

# OA-U Type Ultra low noise Crystal Oscillator

## 3.2 x 2.5 x 0.9 mm SMD package (RMS jitter : 50fs typical)

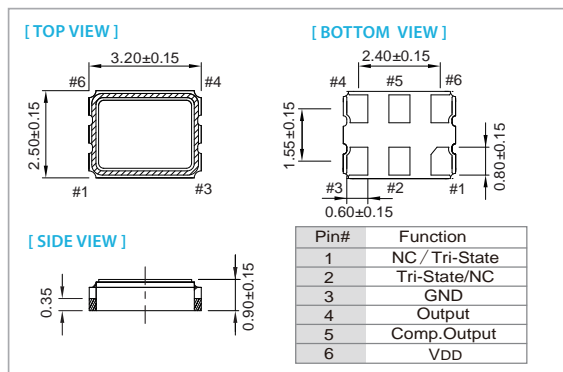
### FEATURE

- Typical 3.2 x 2.5 x 0.9mm ceramic SMD package.
- Ultra low integrated phase jitter < 100fs, 12kHz to 20MHz
- Typical phase jitter 50fs @ 156.25MHz
- Differential output level : LVPECL /LVDS/HCSL
- Operation supply voltage: 1.8V, 2.5V and 3.3V
- Pb-free/RoHS compliant

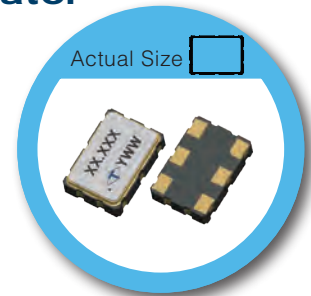
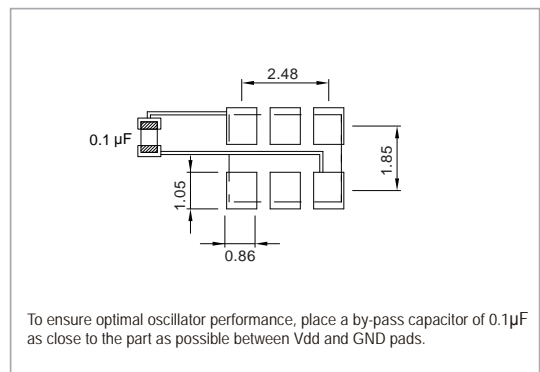
### TYPICAL APPLICATION

- 40Gbit/100Gbit Ethernet, MAN, SONET
- Fiber Channel
- Test Instrumentation

### DIMENSION (mm)



### SOLDER PAD LAYOUT (mm)



RoHS Compliant

### ELECTRICAL SPECIFICATION

Parameter	LVPECL				Unit	
	3.3V		2.5V			
	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V <sub>DD</sub> )	V <sub>DD</sub> -10%	V <sub>DD</sub> +10%	V <sub>DD</sub> -5%	V <sub>DD</sub> +5%	V	
Frequency range	100	220	100	220	MHz	
Standard frequency	100, 125, 156.25				MHz	
Power current consumption:	-	65	-	65	mA	
Output Level	Output High	2.215	2.42	1.415	1.64	V
	Output Low	1.49	1.68	0.69	1.88	V
Transition Time	Rise Time	-	0.4	-	0.4	nSec
	Fall Time	-	0.4	-	0.4	nSec
Duty Cycle	45	55	45	55	%	
Start-up Time	-	5	-	5	mSec	
Tri-State	Output Enable	0.7 x V <sub>DD</sub>	-	0.7 x V <sub>DD</sub>	-	V
	Output Disable	-	0.3 x V <sub>DD</sub>	-	0.3 x V <sub>DD</sub>	
Stand by Current	-	30	-	30	µA	
Output Loading	50Ω, V <sub>DD</sub> -2V					
Phase Noise						
@ V <sub>DD</sub> =3.3V 156.25MHz	offset 10kHz	Typ.: -150		Typ.: -150		dBc/Hz
	offset 100kHz	Typ.: -155		Typ.: -155		dBc/Hz
	offset 1MHz	Typ.: -160		Typ.: -160		dBc/Hz
RMS Phase Jitter Integrated 12KHz to 20MHz @156.25MHz	-	0.1	-	0.1	pSec	
Aging (@ 25°C, First Year)	±3		±3		°C	
Storage Temp. Range	-55	125	-55	125	°C	

Note: not all combination of options are available. Other specifications may be available upon request.

Specifications subject to change without notice.

Parameters		LVDS						Unit
		3.3V		2.5V		1.8V		
		Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation (V <sub>DD</sub> )		V <sub>DD</sub> -10%	V <sub>DD</sub> +10%	V <sub>DD</sub> -5%	V <sub>DD</sub> +5%	V <sub>DD</sub> -5%	V <sub>DD</sub> +5%	V
Frequency range		100	175	100	175	100	175	MHz
Standard frequency		100, 125, 156.25						MHz
Power current consumption:		-	35	-	35	-	25	mA
Output Level								
Differential output (V <sub>OD</sub> , OUT-OUTN)		0.24	0.45	0.24	0.45	0.24	0.45	V
Output High		-	1.6	-	1.6	-	1.6	V
Output Low		0.9	-	0.9	-	0.9	-	V
Transition Time	Rise Time	-	0.3	-	0.3	-	0.4	nSec
	Fall Time	-	0.3	-	0.3	-	0.4	nSec
Duty Cycle		45	55	45	55	45	55	%
Start-up Time		-	5	-	5	-	5	mSec
Tri-State	Output Enable	0.7 x V <sub>DD</sub>	-	0.7 x V <sub>DD</sub>	-	0.7 x V <sub>DD</sub>	-	V
	Output Disable	-	0.3 x V <sub>DD</sub>	-	0.3 x V <sub>DD</sub>	-	0.3 x V <sub>DD</sub>	
Stand by Current		-	30	-	30	-	30	uA
Output Loading		100						Ω
Phase Noise								
@ V <sub>DD</sub> =3.3V 156.25MHz	offset 10kHz	Typ.: -150		Typ.: -150		Typ.: -150		dBc/Hz
	offset 100kHz	Typ.: -155		Typ.: -155		Typ.: -155		dBc/Hz
	offset 1MHz	Typ.: -160		Typ.: -160		Typ.: -160		dBc/Hz
RMS Phase Jitter Integrated 12KHz to 20MHz @156.25MHz		-	0.1	-	0.1	-	0.1	pSec
Aging (@ 25°C, First Year)		±3		±3		±3		ppm
Storage Temp. Range		-55	125	-55	125	-55	125	°C

Parameter		HCSL						Unit
		3.3V		2.5V		1.8V		
		Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation (V <sub>DD</sub> )		V <sub>DD</sub> -10%	V <sub>DD</sub> +10%	V <sub>DD</sub> -5%	V <sub>DD</sub> +5%	V <sub>DD</sub> -5%	V <sub>DD</sub> +5%	V
Frequency range		100	135	100	135	100	135	MHz
Standard frequency		100, 125, 156.25						MHz
Power current consumption:		-	46	-	46	-	46	mA
Output Level								
Output High		0.6	0.9	0.6	0.9	0.5	1.0	V
Output Low		-0.15	0.15	-0.15	0.15	-0.15	0.15	V
Transition Time	Rise Time	-	0.6	-	0.6	-	0.6	nSec
	Fall Time	-	0.6	-	0.6	-	0.6	nSec
Duty Cycle		45	55	45	55	45	55	%
Start-up Time		-	5	-	5	-	5	mSec
Tri-State	Output Enable	0.7 x V <sub>DD</sub>	-	0.7 x V <sub>DD</sub>	-	0.7 x V <sub>DD</sub>	-	V
	Output Disable	-	0.3 x V <sub>DD</sub>	-	0.3 x V <sub>DD</sub>	-	0.3 x V <sub>DD</sub>	
Stand by Current		-	30	-	30	-	30	uA
Output Loading		50 (To GND)						Ω
Phase Noise								
offset 10kHz		Typ.: -150		Typ.: -150		Typ.: -150		dBc/Hz
offset 100kHz		Typ.: -155		Typ.: -155		Typ.: -155		dBc/Hz
offset 1MHz		Typ.: -160		Typ.: -160		Typ.: -160		dBc/Hz
RMS Phase Jitter Integrated 12KHz to 20MHz @156.25MHz		-	0.1	-	0.1	-	0.1	pSec
Aging (@ 25°C, First Year)		±3		±3		±3		ppm
Storage Temp. Range		-55	125	-55	125	-55	125	°C

**Note: not all combination of options are available. Other specifications may be available upon request.**

### FREQ. STABILITY vs. TEMP. RANGE

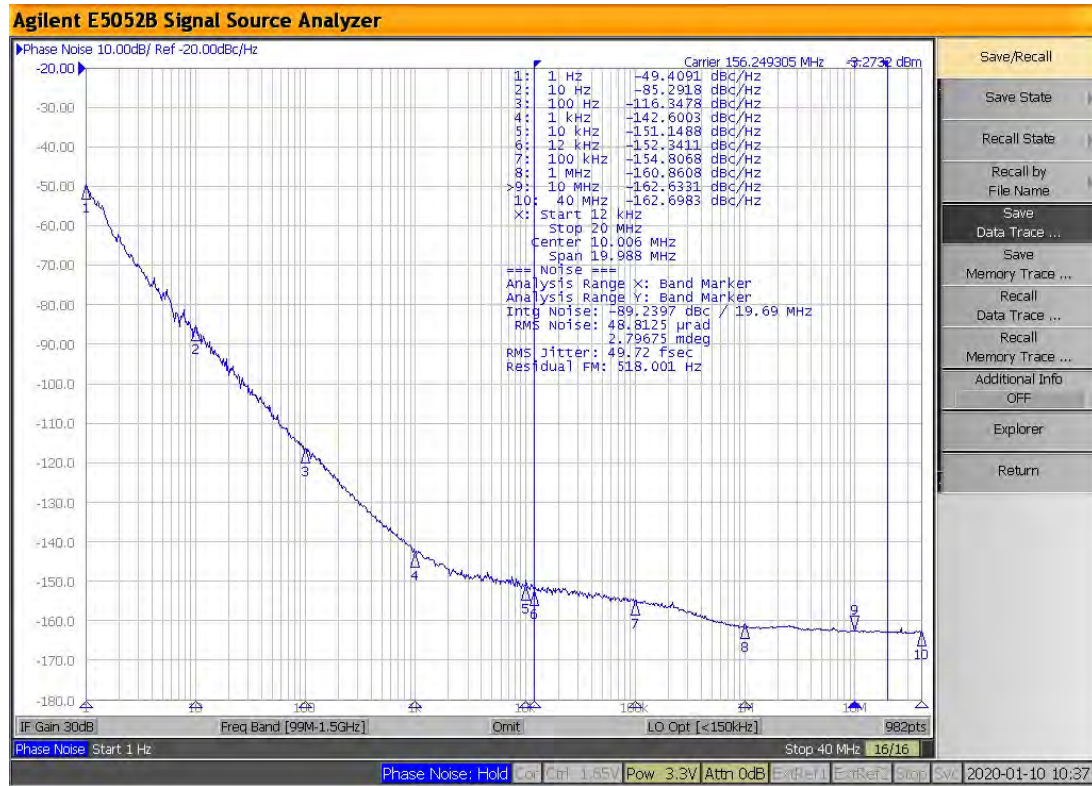
Temp. (°C)	ppm		
	± 20	± 25	± 50
-10 ~ +60	O	O	O
-20 ~ +70	O	O	O
-40 ~ +85	Δ	O	O
-40 ~ +105	X	X	O
-40 ~ +125	X	X	Δ

\* O : Available Δ: Conditional X: Not available

\* Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1<sup>st</sup> year), shock, and vibration

### Phase Noise Test Data

Output level: LVPECL, Fout=156.25MHz, VDD=3.3V, Ta=25°C



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