

U\_B2B-Connectors  
B2B-Connectors.SchDoc

U\_B13  
B13.SchDoc

U\_B14  
B14.SchDoc

U\_B15  
B15.SchDoc

U\_B16  
B16.SchDoc

U\_B34  
B34.SchDoc

U\_FPGA-MGT  
FPGA-MGT.SchDoc

U\_FPGA-CFG  
FPGA-CFG.SchDoc

U\_FPGA-PWR  
FPGA-PWR.SchDoc

U\_Clock  
Clock.SchDoc

U\_DDR3-RAM  
DDR3-RAM.SchDoc

U\_ETHERNET  
ETHERNET.SchDoc

U\_CPLD  
CPLD.SchDoc

U\_PWR1  
PWR1.SchDoc

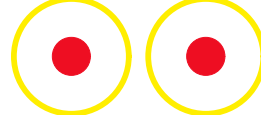
U\_PWR2  
PWR2.SchDoc

Serial  
Serialnumber 6,3 x 6.3mm

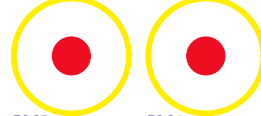
FIDU-DOT - small FIDU-DOT - small



PM1 PM2  
FIDU-DOT - small FIDU-DOT - small

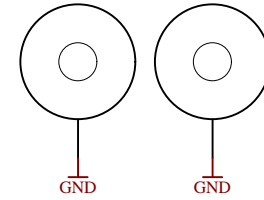


PM3 PM4  
FIDU-DOT - small FIDU-DOT - small

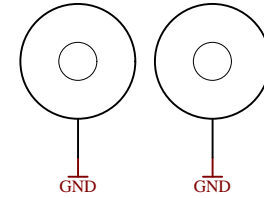


PM5 PM6

Mount.Hole 3.2mm Mount.Hole 3.2mm




Mount.Hole 3.2mm Mount.Hole 3.2mm



Top of Board



		Title: <b>TE0712</b>	
		A4	Number: <b>TE0712 200_21</b>
Date: 2015-12-09		Copyright: Trenz Electronic GmbH	
Page 1		of 16	
Filename: <b>TE0712.SchDoc</b>			

A

B

C

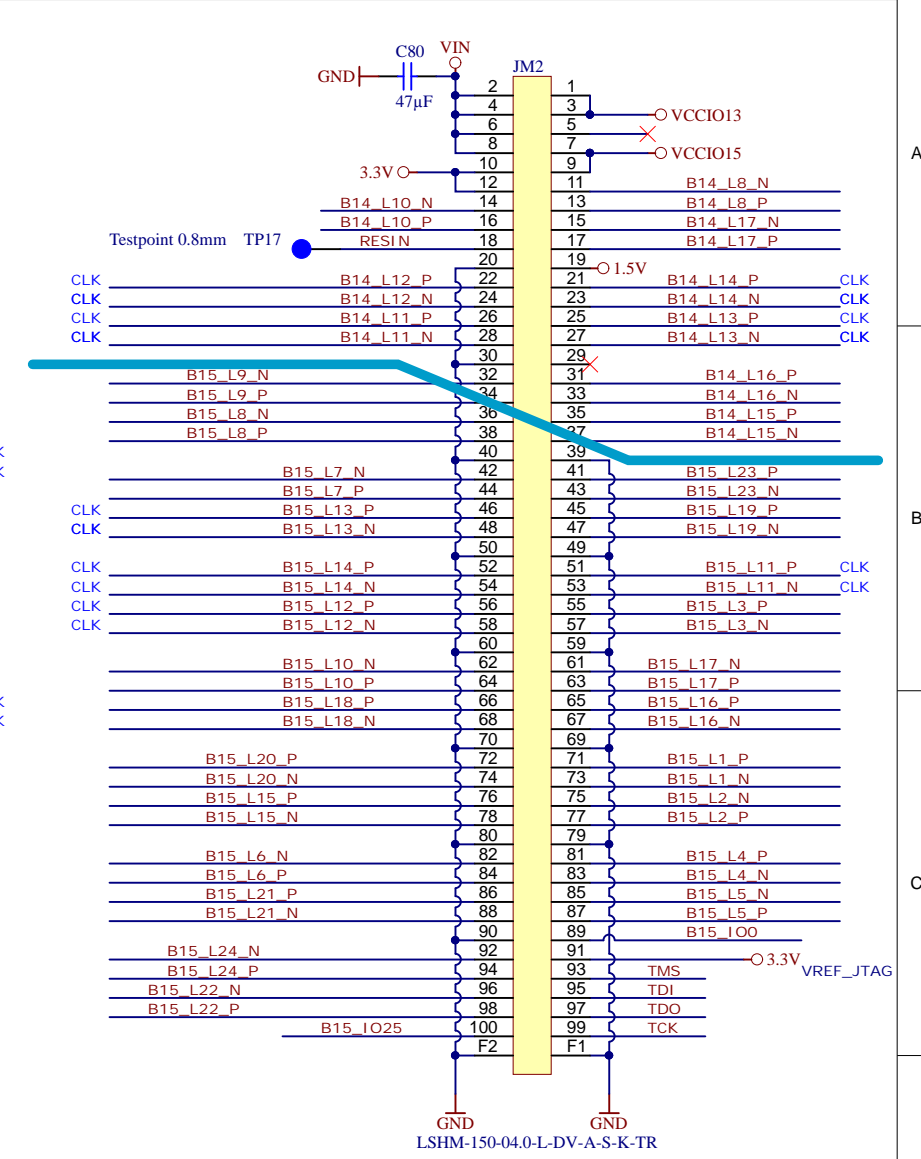
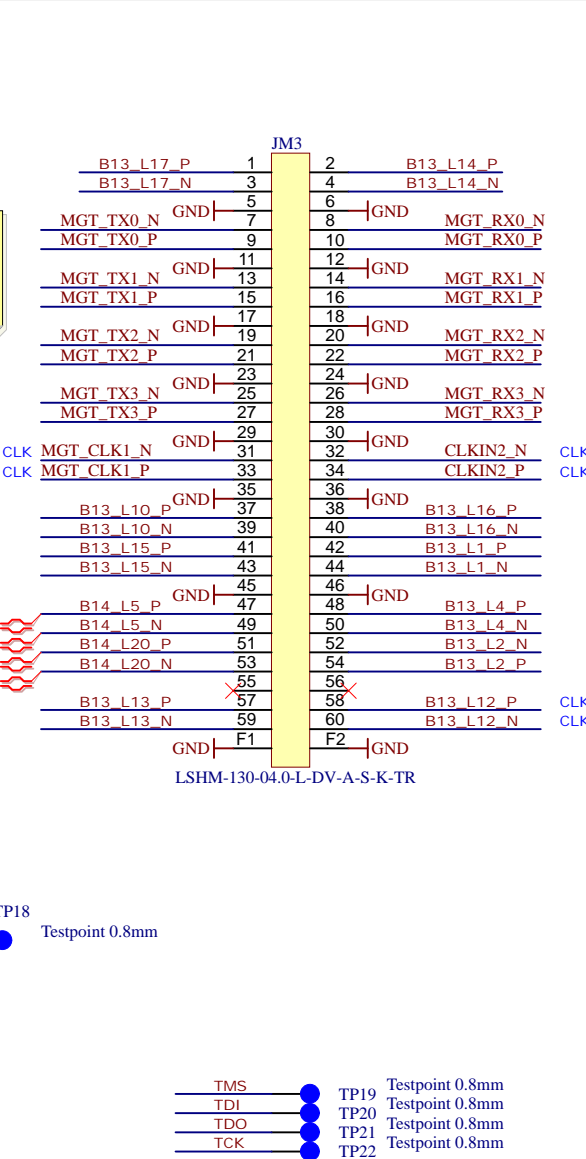
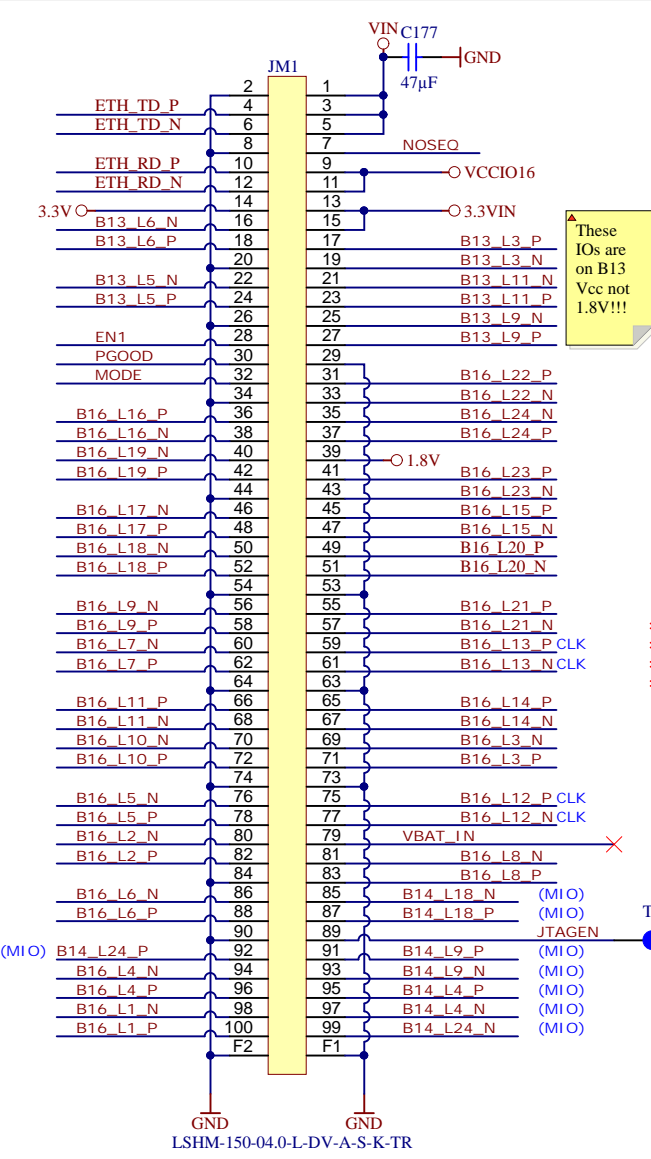
D

A

B

C

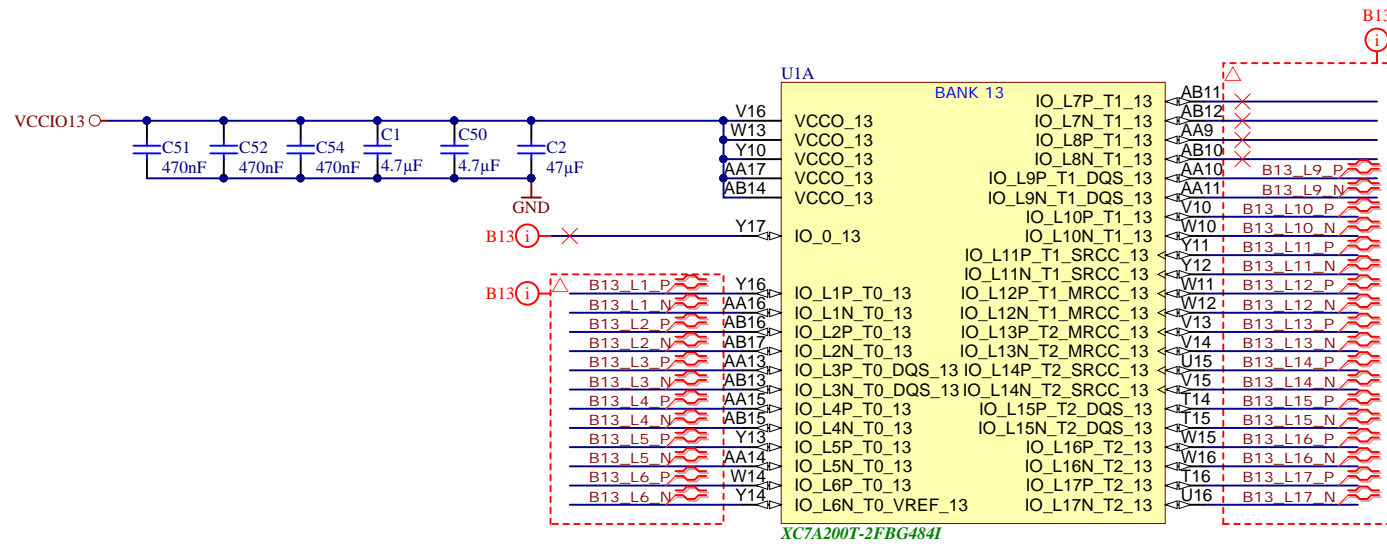
D



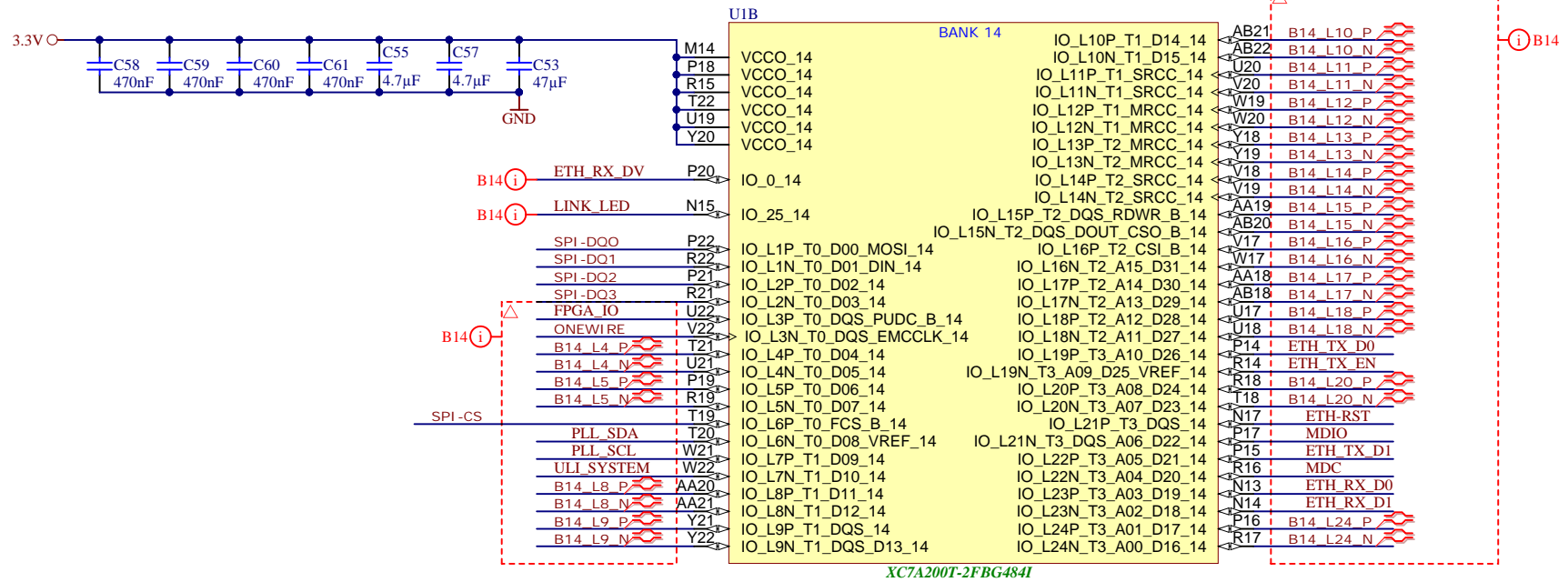
- TMS ● TP19 Testpoint 0.8mm
- TDI ● TP20 Testpoint 0.8mm
- TDO ● TP21 Testpoint 0.8mm
- TCK ● TP22 Testpoint 0.8mm



Title: <b>B2B</b>		
A4	Number: <b>TE0712 200_21</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page2 of 16
Filename: <b>B2B-Connectors.SchDoc</b>		



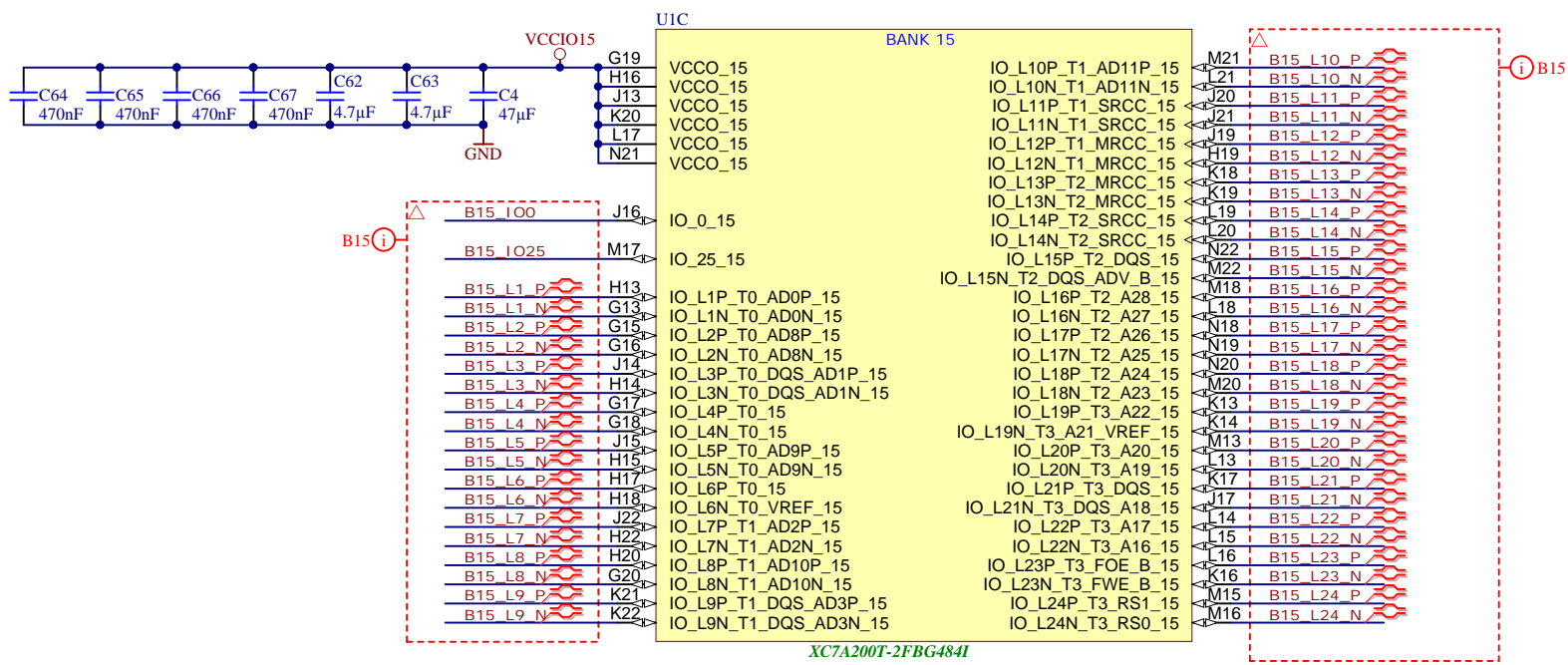
Title: B13		
A4	Number: TE0712 200_21	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 3 of 16
Filename: B13.SchDoc		



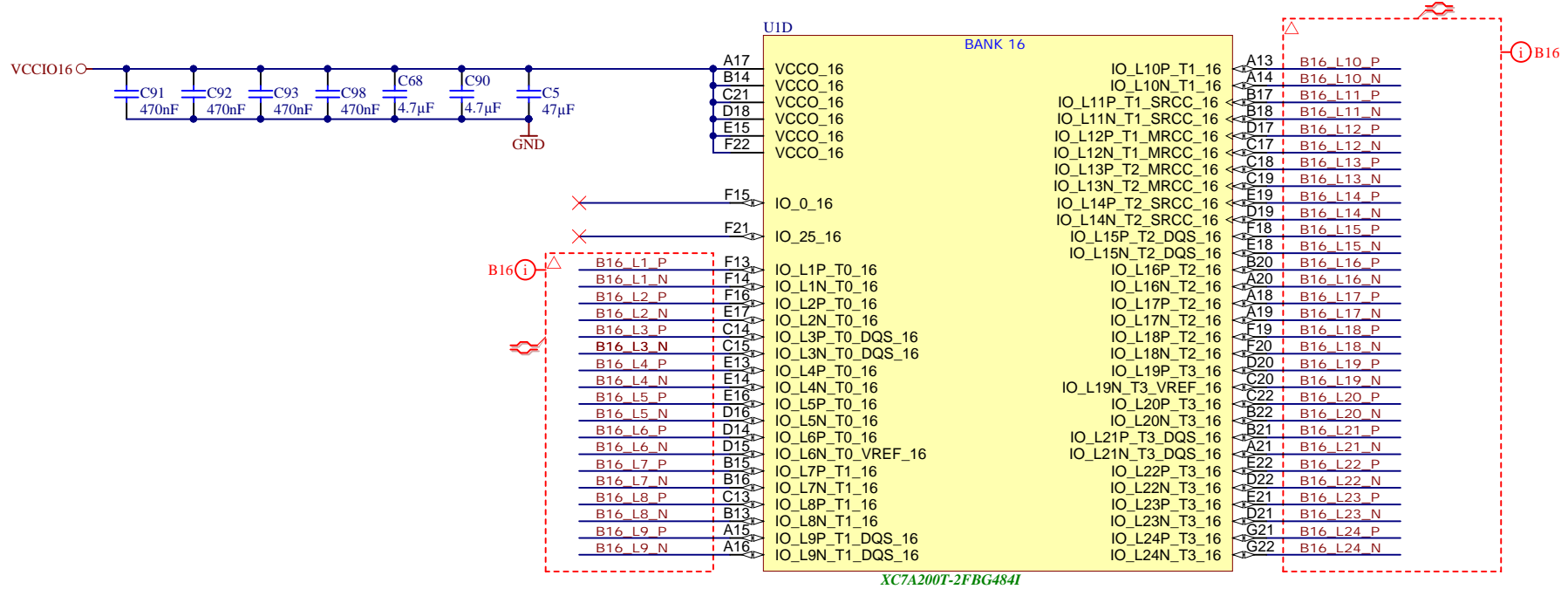
XC7A200T-2FBG484I



Title: <b>B14</b>		
A4	Number: <b>TE0712 200_21</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>4</b> of <b>16</b>
Filename: <b>B14.SchDoc</b>		



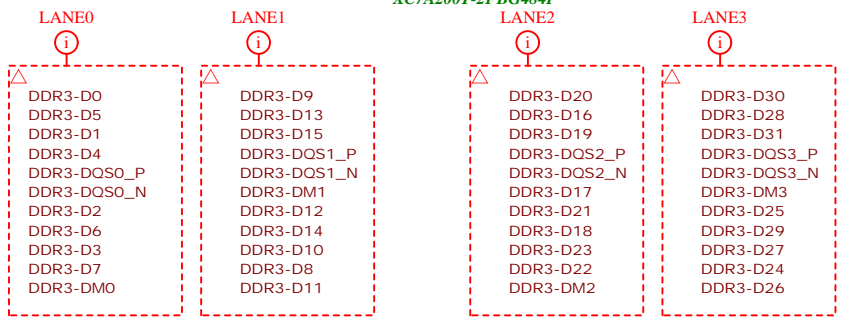
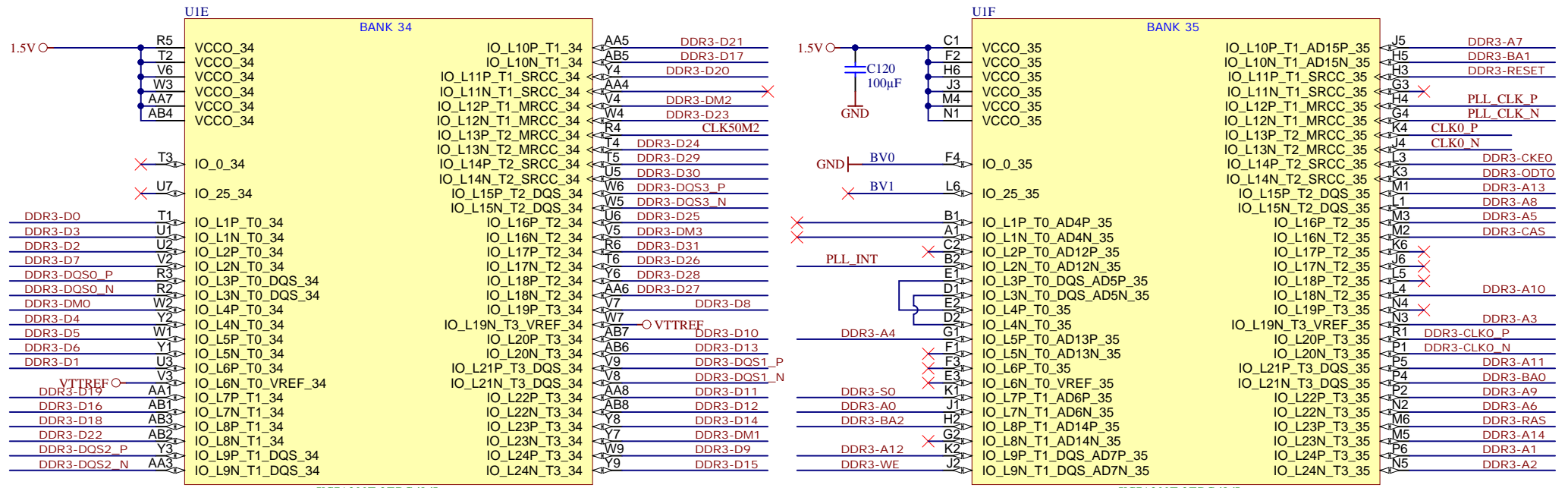
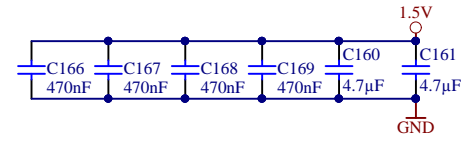
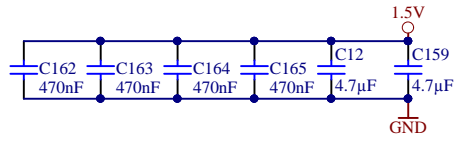
Title: <b>B15</b>		
A4	Number: <b>TE0712 200_21</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>5</b> of <b>16</b>
Filename: <b>B15.SchDoc</b>		



XC7A200T-2FBG484I

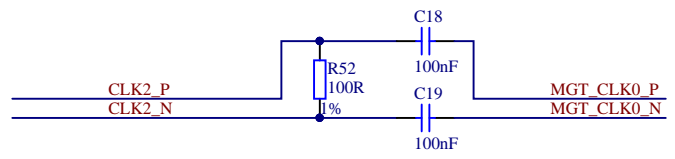
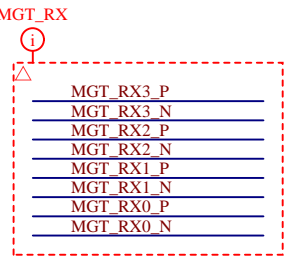
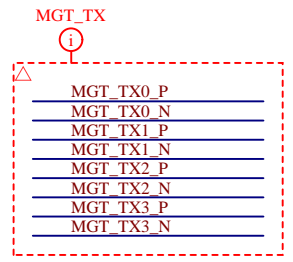
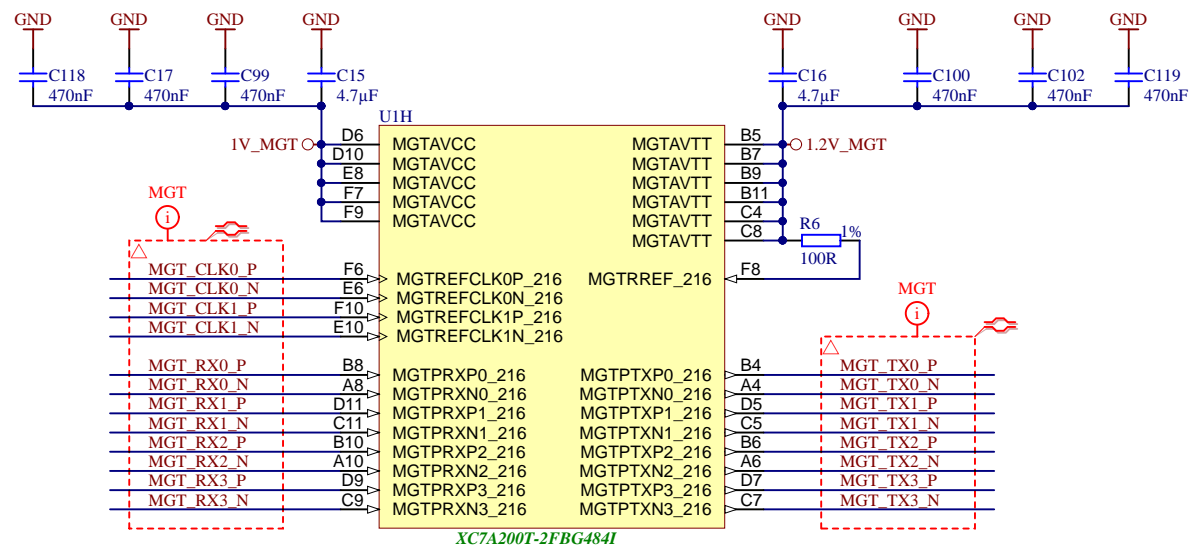


Title: <b>B16</b>		
A4	Number: <b>TE0712 200_2I</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>6</b> of <b>16</b>
Filename: <b>B16.SchDoc</b>		



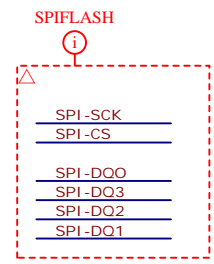
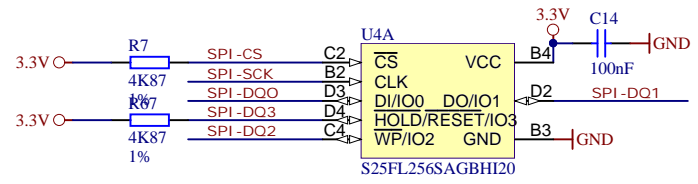
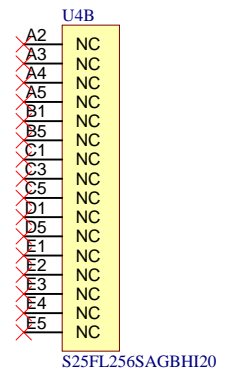
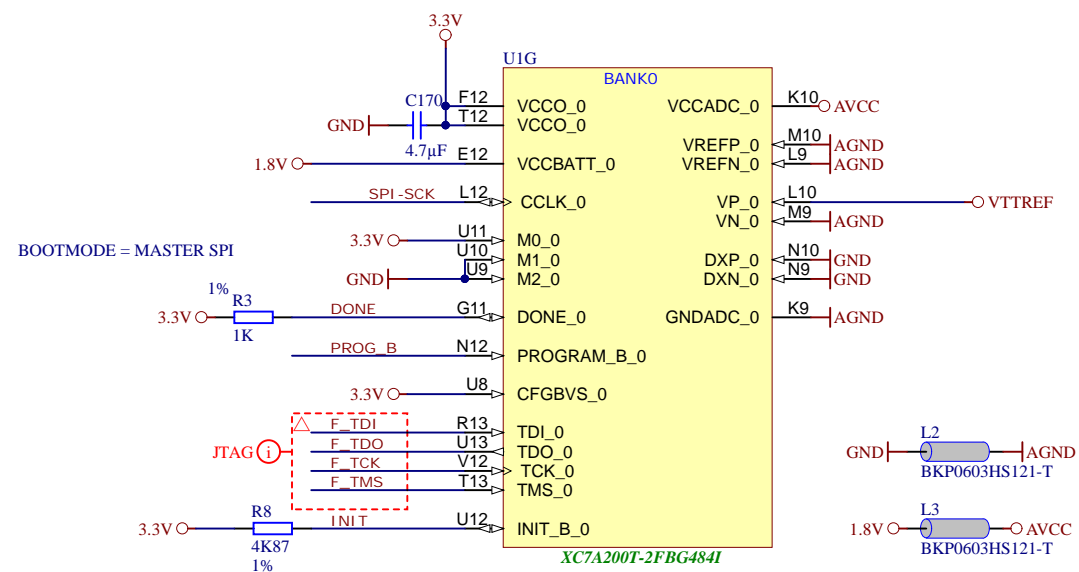
**trenz electronic**

Title: <b>B34</b>		
A4	Number: <b>TE0712 200_21</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: Trenz Electronic GmbH	
Page <b>7</b> of <b>16</b>		Filename: <b>B34.SchDoc</b>

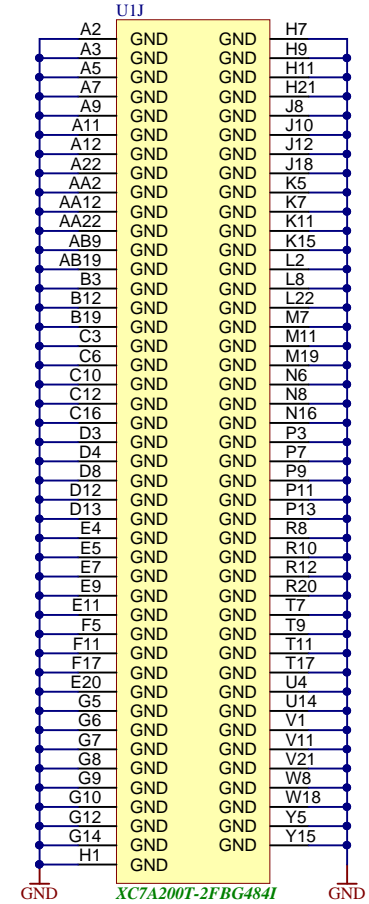
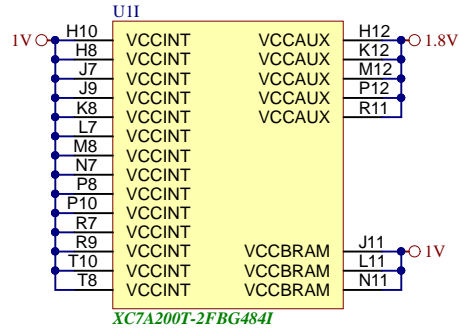
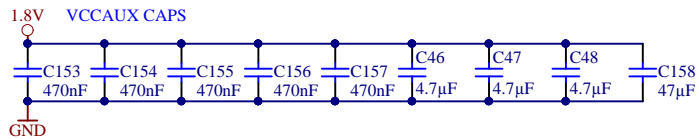
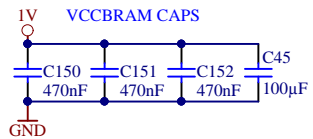
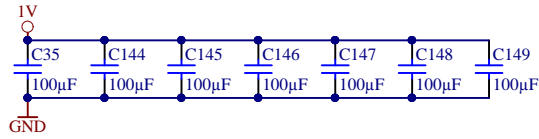
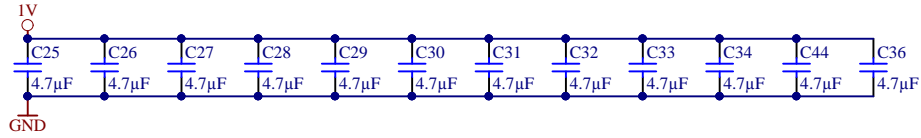
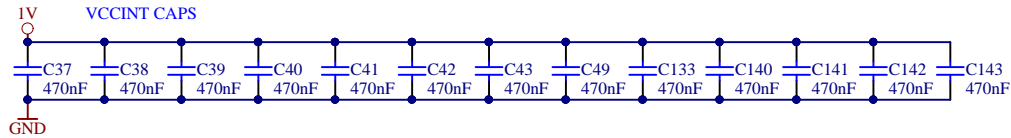


Title: MGT		
A4	Number: TE0712 200_2I	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 8 of 16
Filename: FPGA-MGT.SchDoc		

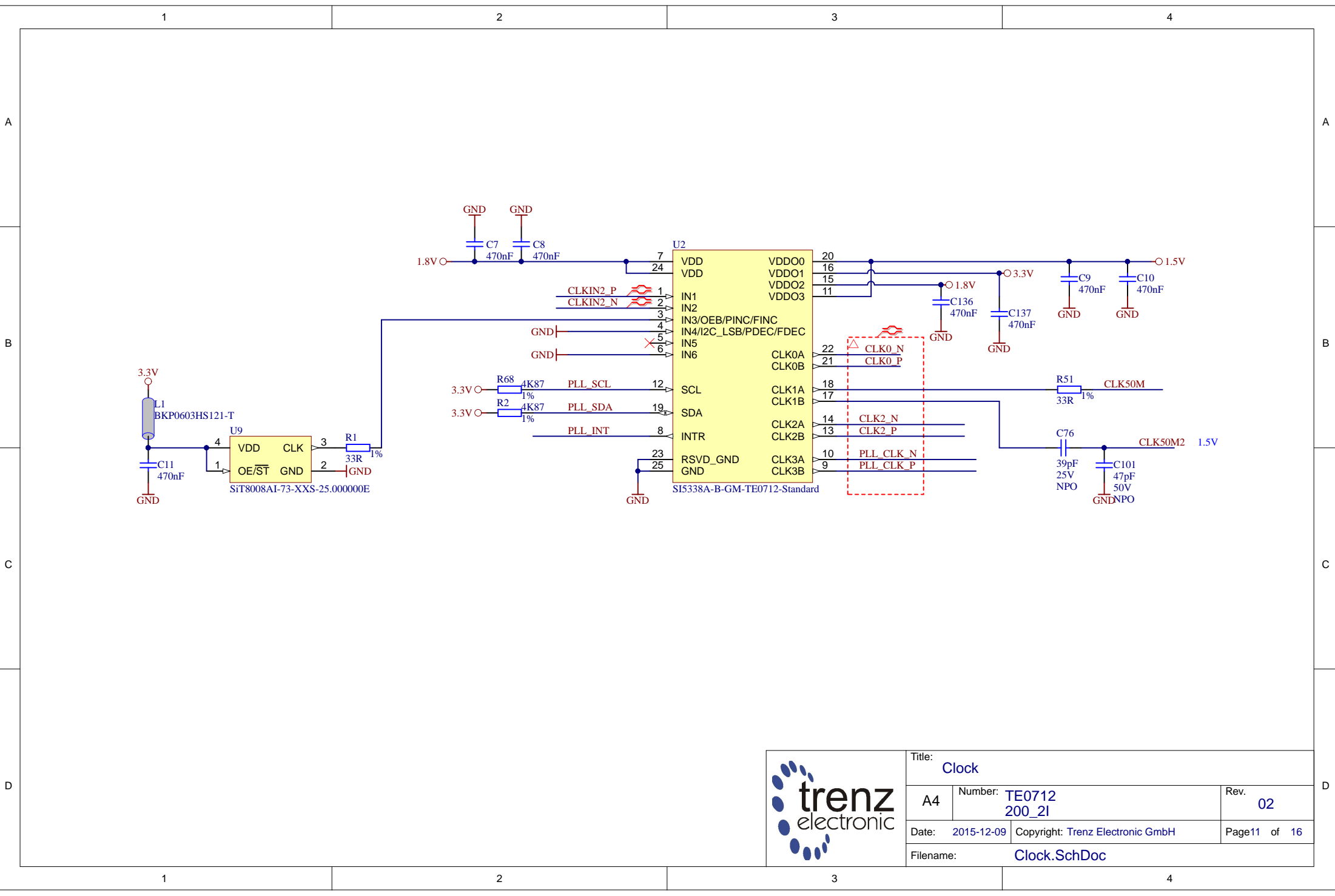





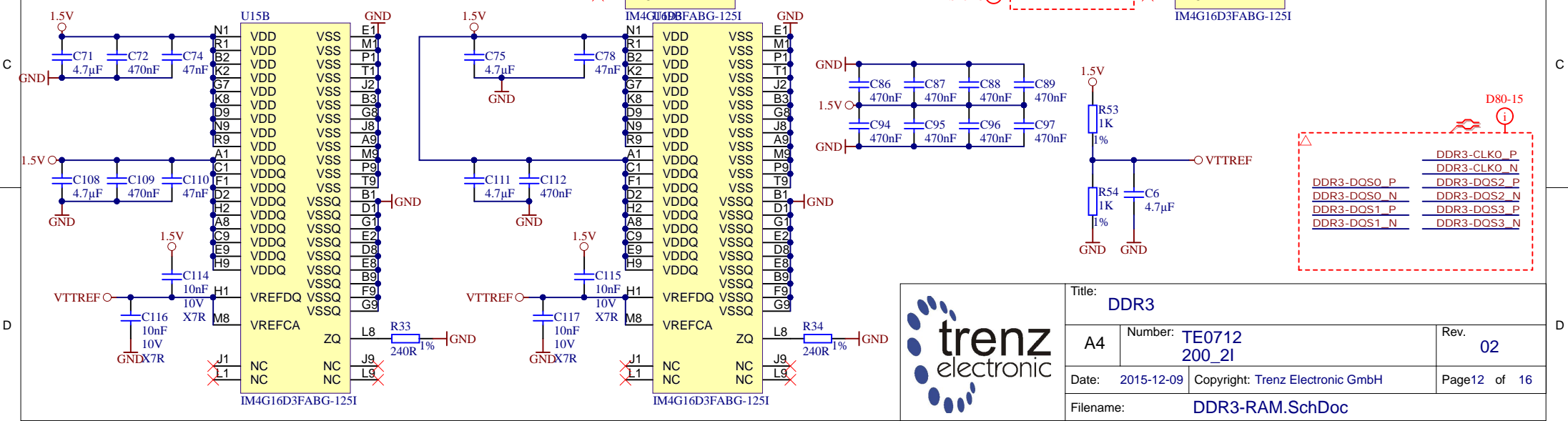
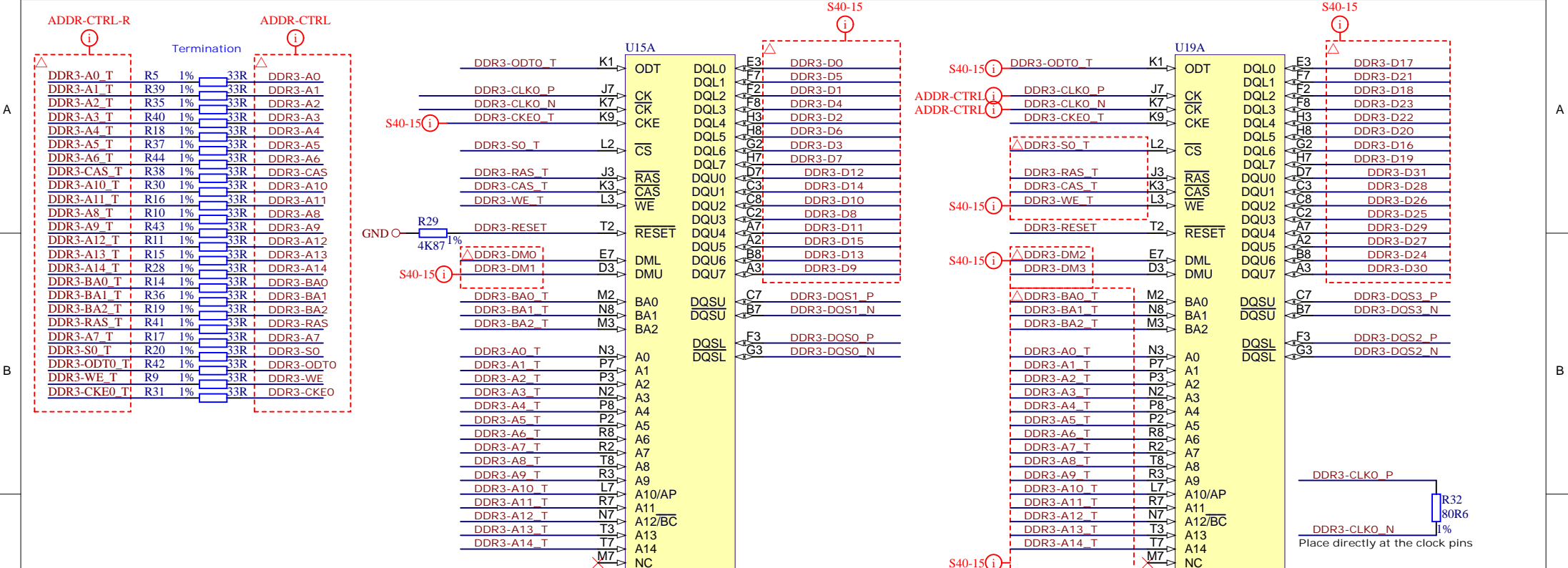
Title: CFG		
A4	Number: TE0712 200_21	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 9 of 16
Filename: FPGA-CFG.SchDoc		



Title: <b>PWR</b>		
A4	Number: <b>TE0712 200_21</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>10</b> of <b>16</b>
Filename: <b>FPGA-PWR.SchDoc</b>		

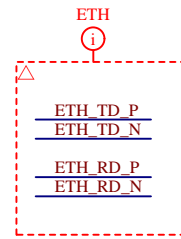
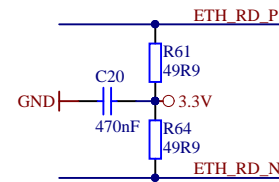
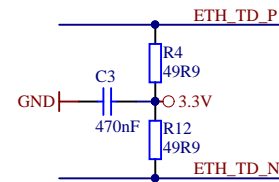
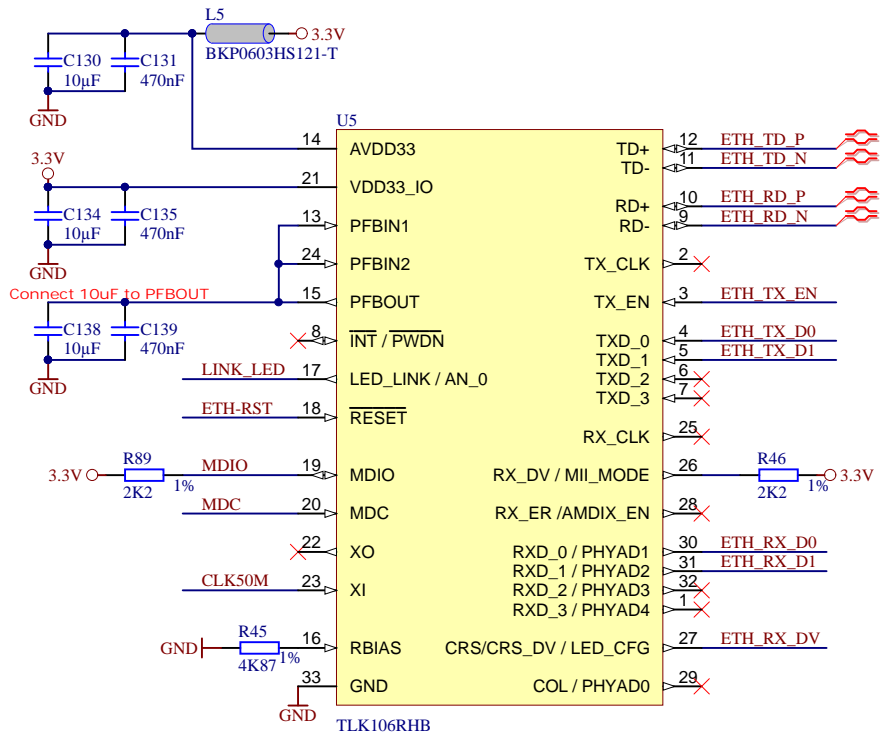



		Title: <b>Clock</b>	
		A4	Number: <b>TE0712 200_21</b> Date: 2015-12-09 Copyright: Trenz Electronic GmbH Filename: <b>Clock.SchDoc</b>

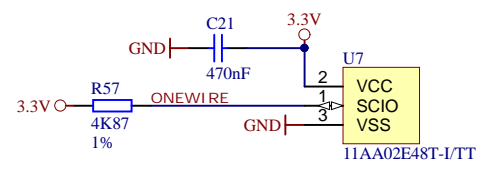
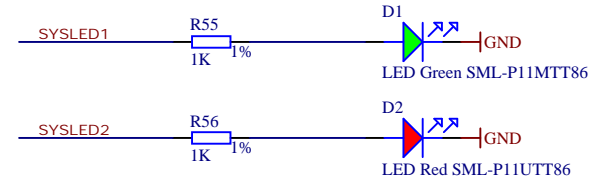
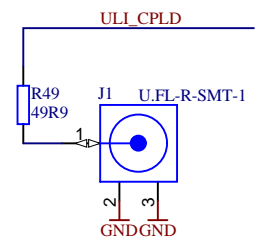
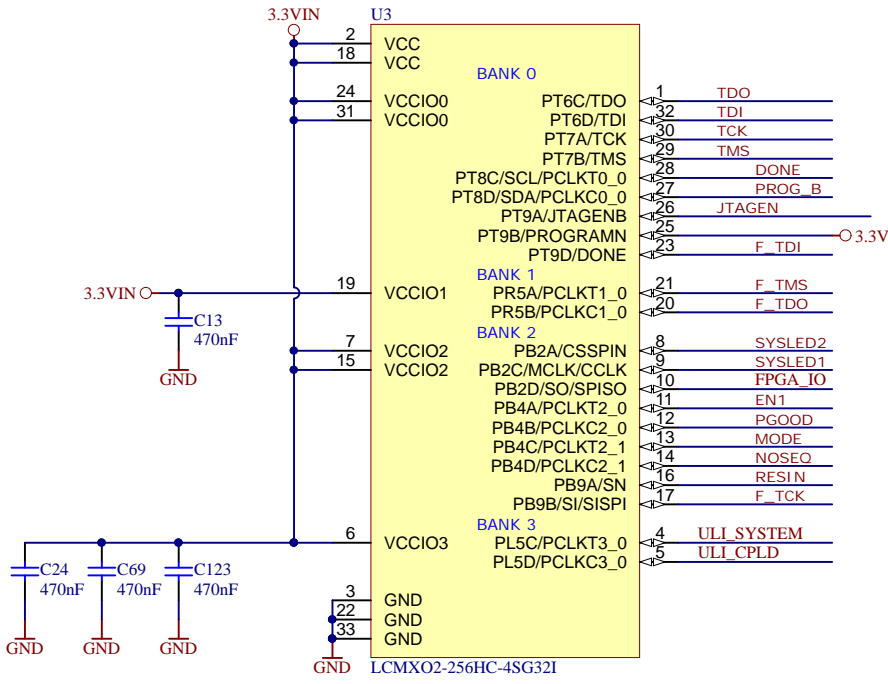


Title: **DDR3**

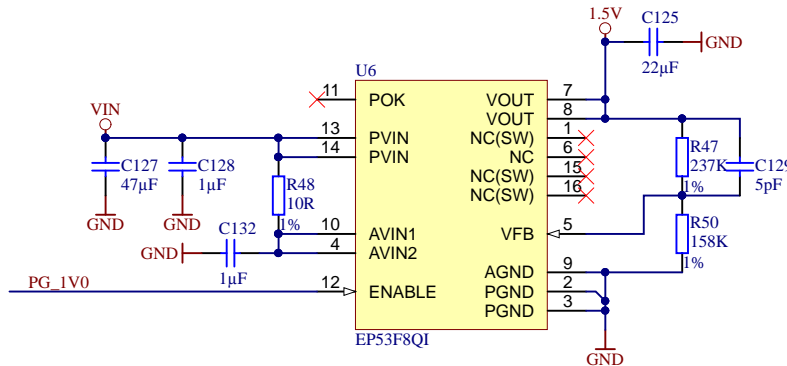
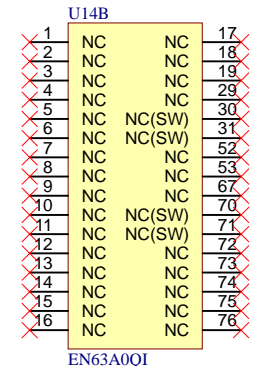
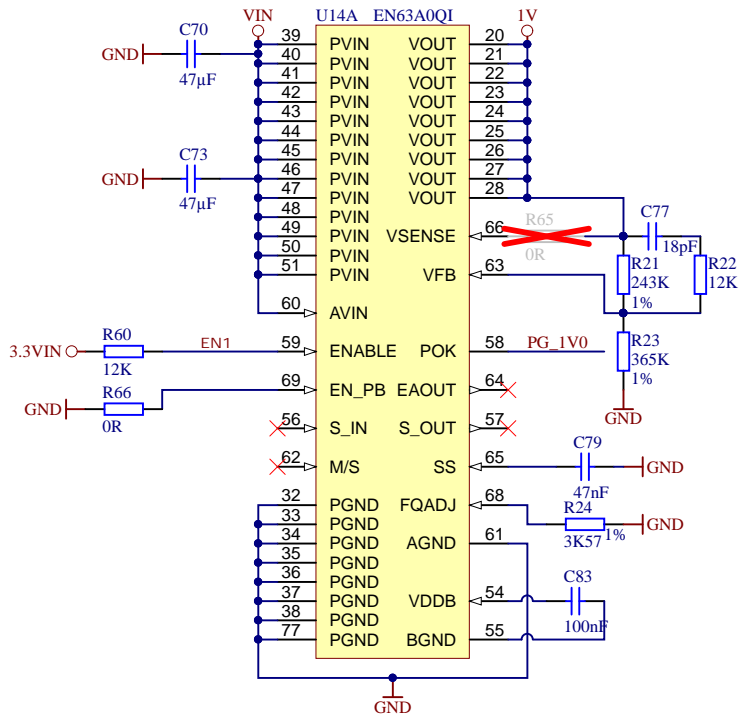
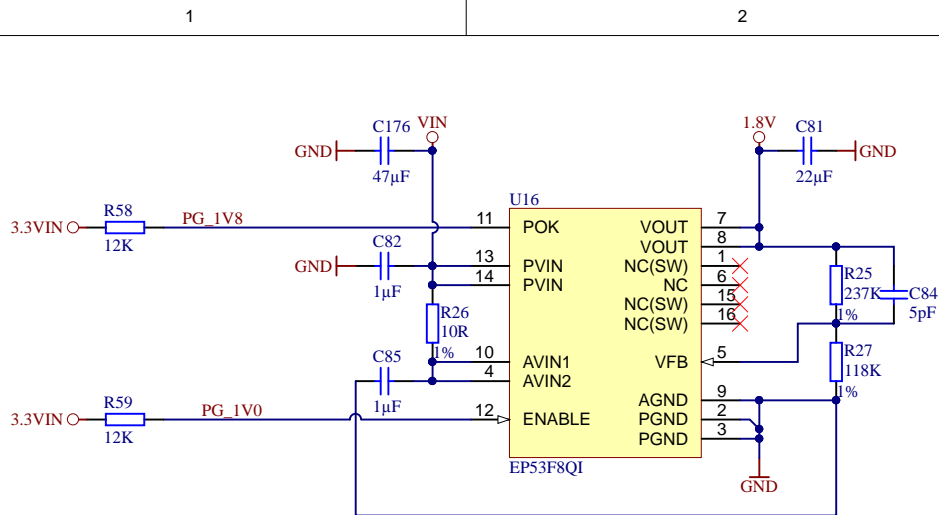
A4	Number: <b>TE0712 200_21</b>	Rev. <b>02</b>
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	
Filename: <b>DDR3-RAM.SchDoc</b>		Page 12 of 16



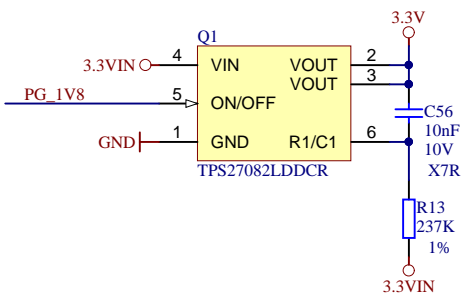
		Title: <b>ETH</b>	
		A4	Number: <b>TE0712 200_21</b>
Date: 2015-12-09		Copyright: Trenz Electronic GmbH	
Filename: <b>ETHERNET.SchDoc</b>		Page13 of 16	



Title: <b>CPLD</b>		
A4	Number: <b>TE0712 200_21</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>14</b> of <b>16</b>
Filename: <b>CPLD.SchDoc</b>		



R65	R66	MODE	EN63A0QI
OK	X		enable pre-bias start-up
X	OK		disable pre-bias start-up



- VIN - TP1 - Testpoint 0.8mm
- 3.3VIN - TP4 - Testpoint 0.8mm
- 3.3V - TP7 - Testpoint 0.8mm
- 1.8V - TP10 - Testpoint 0.8mm
- 1.5V - TP13 - Testpoint 0.8mm
- VTTREF - TP3 - Testpoint 0.8mm
- 1V - TP2 - Testpoint 0.8mm
- 1.2V\_MGT - TP5 - Testpoint 0.8mm
- VCCIO13 - TP8 - Testpoint 0.8mm
- VCCIO15 - TP11 - Testpoint 0.8mm
- VCCIO16 - TP14 - Testpoint 0.8mm
- GND - TP6 - Testpoint 0.8mm
- GND - TP9 - Testpoint 0.8mm
- GND - TP12 - Testpoint 0.8mm
- GND - TP15 - Testpoint 0.8mm



Title: PWR		
A4	Number: TE0712 200_21	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 15 of 16
Filename: PWR1.SchDoc		

1

2

3

4

A

A

B

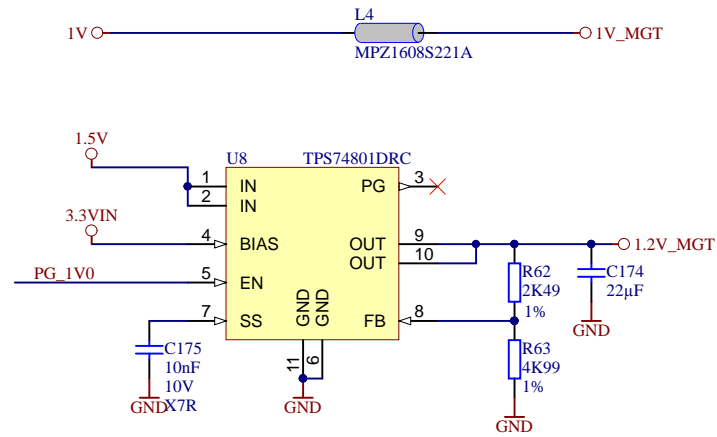
B


C

C

D

D



	Title: PWR		
	A4	Number: TE0712 200_21	Rev. 02
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 16 of 16
	Filename: PWR2.SchDoc		

1

2

3

4