LT3960 I^2C to CAN-Physical Transceiver

DESCRIPTION

Evaluation circuit EVAL-LT3960-AZ features the LT®3960, an I^2C to CAN-Physical transceiver in a 10-lead plastic MSOP package. EVAL-LT3960-AZ consists of two ICs configured in the master and slave mode using selectable jumpers, JP1 and JP3. The board is designed to be easily snapped apart at the center, separating two circuitries.

The LT3960 I^2C to CAN-Physical transceiver is used to send and receive I^2C data through harsh or noisy environments at up to 400kb/s using the CAN-Physical layer for differential signaling over twisted pair connections. The SDA and SCL data lines are converted to differential signals and are shared between devices connected to the bus. This allows for the physical separation of the I^2C source and I^2C receiver.

The first LT3960 is connected to the I^2C master (I^2C-compatible microcontroller). The second LT3960 should be connected to the first LT3960 by two twisted pairs. It regenerates the I^2C bus locally for one or more I^2C slave devices. The LT3960 devices transmit the clock signal in only one direction, from master to slave. Bidirectional communication of the data signal is always permitted.

The LT3960 data sheet gives a complete description of the parts, their operation, and application information. The data sheet must be read in conjunction with this user guide for the evaluation circuit EVAL-LT3960-AZ. The LT3960EMSE is assembled in a 10-lead MSOP package.

Design files for this circuit board are available.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage	V_{IN} Tied to V_{CC}, 3.3V Range	(Jumper JP2, JP4: $V_{IN} = V_{CC}$)	3	3.3	3.6	V
		V_{IN} Tied to V_{CC}, 5V Range	(Jumper JP2, JP4: $V_{IN} = V_{CC}$)	4.5	5	5.5	V
		V_{CC} Regulated Internally from V_{IN}	(Jumper JP2, JP4: $V_{IN} \neq V_{CC}$)	4		60	V
V_{MSTR}, V_{SLV}, V_{SHDN}	EN/MODE Voltage	Master Mode	(Jumper JP1, JP3: MASTER)	2		5	V
		Slave Mode	(Jumper JP1, JP3: SLAVE)	0.7		2	V
		Low Power Shutdown Mode	(Jumper JP1, JP3: OFF)	0		0.7	V
f_{CLK}	Clock Frequency					400	kHz
V_{CM}	Bus Common Mode Voltage	V_{CC} = 3.3V				±25	V
		V_{CC} = 5V				±36	V

QUICK START PROCEDURE

EVAL-LT3960-AZ can be powered by a voltage source between 4V and 60V due to the integrated LDO in the LT3960. The LDO regulates the input from the V_{IN} pin between 4V and 60V to 3.3V on the V_{CC} pin from which the transceivers and bus lines are powered. Alternatively, the EVAL-LT3960-AZ can be powered from a supply voltage of 3.3V or 5V on VIN, bypassing the LDO by shorting VCC to VIN using jumpers JP2 and JP4.

One procedure for using the EVAL-LT3960-AZ is described as follows:

1. Launch Arduino IDE.
2. Connect two Linduinos to the computer via USB.
3. Download the Linduino code from the EVAL-LT3960-AZ webpage.
4. Upload the code to the master and slave Linduinos accordingly.
5. Break the EVAL-LT3960-AZ into two separate boards by applying force to the horizontal scoring line.
6. Use 2 twisted pairs of small wires to connect CANSCLx1 and CANSCLx2; CANSDAx1 and CANS-DAx2.
7. Connect GND1 and GND2 pins on two boards using a small wire (optional).
8. Connect SLC, SDA, GND pins from the master (slave) Linduino to SLC1, SDA1, GND1 (SLC2, SDA2, GND2) of the EVAL-LT3960-AZ, respectively.
9. With input power off, connect the first (second) input power supply to VIN1 and GND1 (VIN2 and GND2) of the EVAL-LT3960-AZ.
10. Turn on input power supplies.
11. Open the serial monitor associated with the slave Linduino and check the received message.

QUICK START PROCEDURE

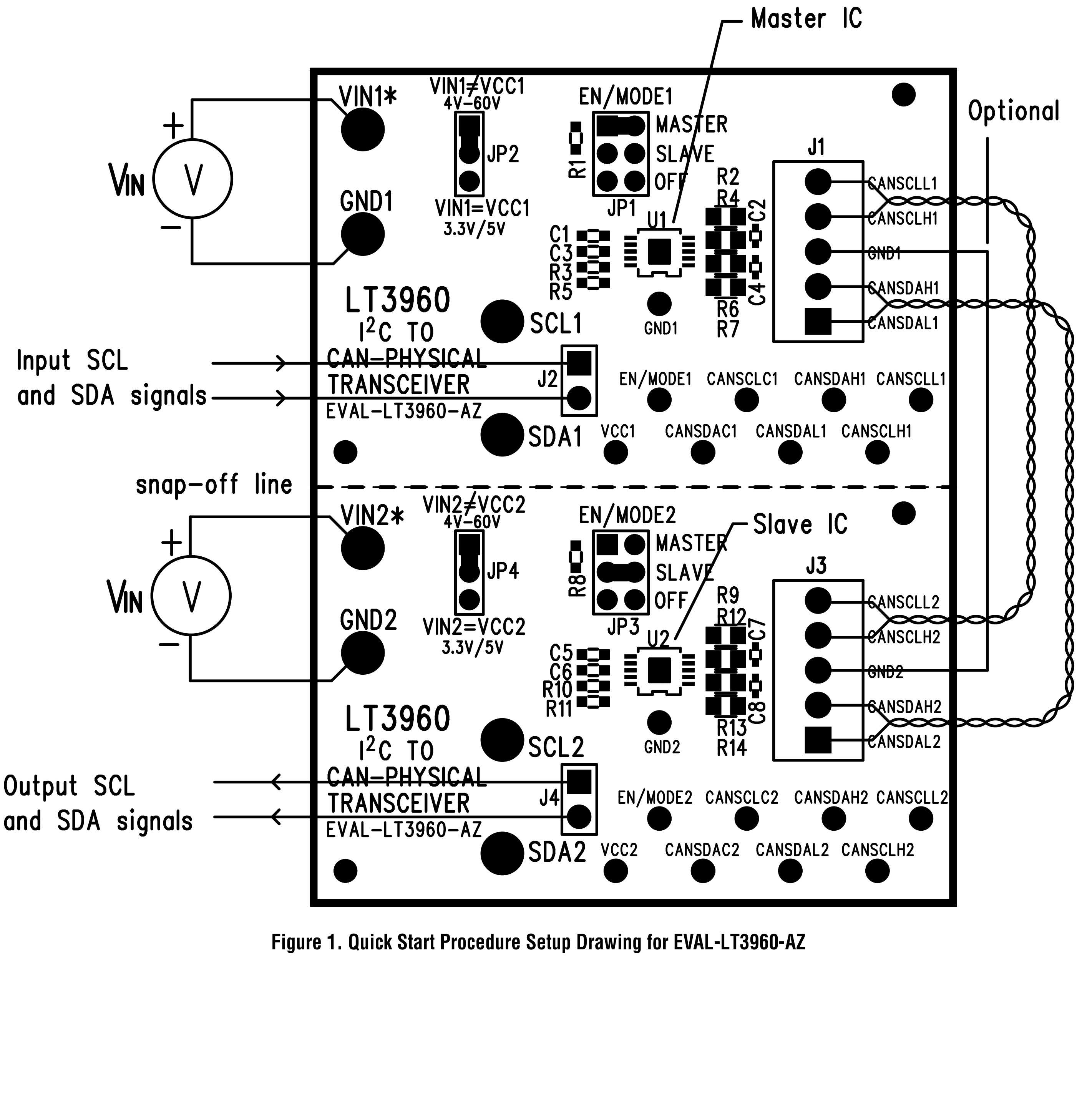


Figure 1. Quick Start Procedure Setup Drawing for EVAL-LT3960-AZ

TEST RESULTS

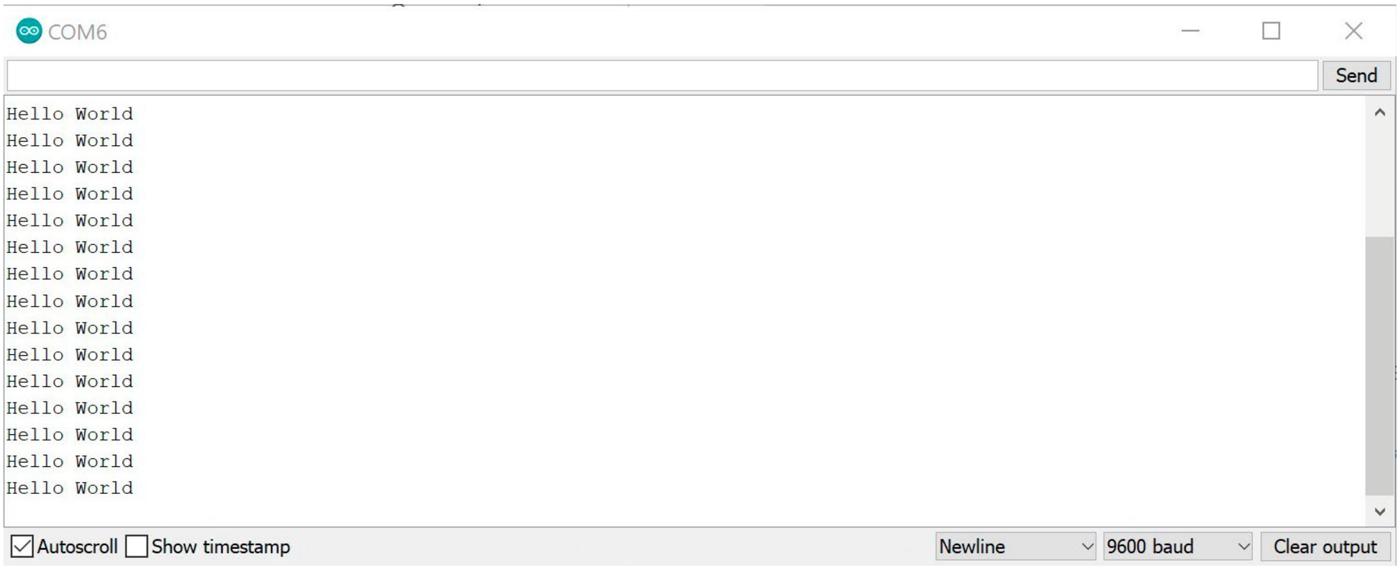
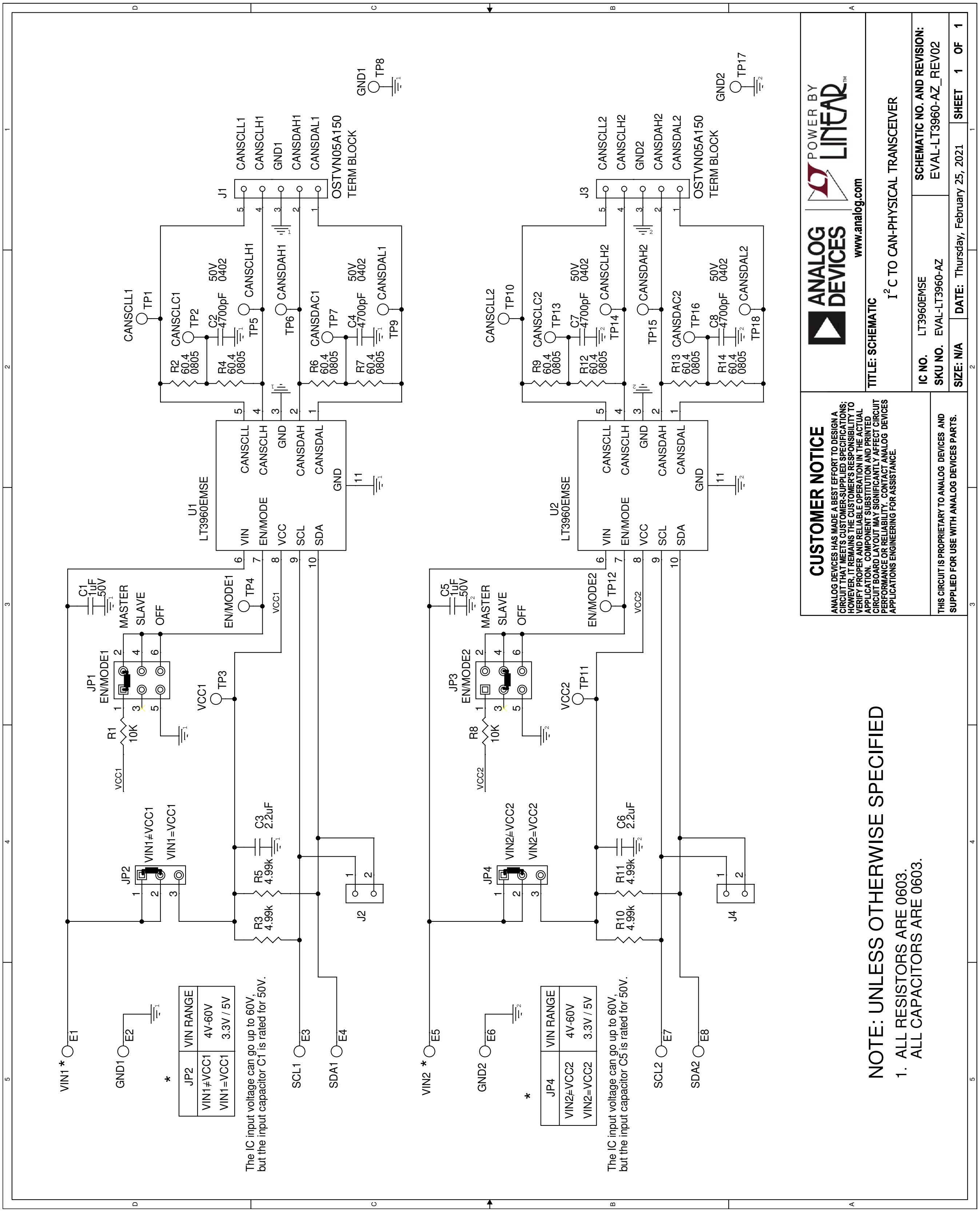


Figure 2. Linduino COM Terminal Window of the Slave Device

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	2	C1, C5	CAP., 1µF, X7R, 50V, 10%, 0603	YAGEO, CC0603KRX7R9BB105
2	4	C2, C4, C7, C8	CAP., 4700pF, X7R, 50V, 10%, 0402	MURATA, GRM155R71H472KA01D
3	2	C3, C6	CAP., 2.2µF, X7S, 10V, 10%, 0603, AEC-Q200	TDK, CGA3E3X7S1A225K080AB
4	2	R1, R8	RES., 10k, 1%, 1/10W, 0603, AEC-Q200	VISHAY, CRCW060310K0FKEA
5	8	R2, R4, R6, R7, R9, R12, R13, R14	RES., 60.4Ω, 1%, 1/8W, 0805, AEC-Q200	PANASONIC, ERJ6ENF60R4V
6	4	R3, R5, R10, R11	RES., 4.99k, 1%, 1/10W, 0603, AEC-Q200	PANASONIC, ERJ3EKF4991V
7	2	U1, U2	IC, 12C TO DUAL CAN TRANSCEIVER, MSOP-10	ANALOG DEVICES, LT3960EMSE#PBF
Hardware: For Demo Board Only				
1	8	E1-E8	TEST POINT, TURRET, 0.064" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2308-2-00-80-00-00-07-0
2	2	J1, J3	CONN., TERM BLOCK, 5 POS, 2.54mm, ST, THT, SIDE ENTRY, GREEN	ON-SHORE TECHNOLOGY, OSTVN05A150
3	2	J2, J4	CONN., HDR, MALE, 1x2, 2.54mm, VERT, ST, THT	WURTH ELEKTRONIK, 61300211121
4	2	JP1, JP3	CONN., HDR, MALE, 2x3, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000621121
5	2	JP2, JP4	CONN., HDR, MALE, 1x3, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000311121
6	18	TP1-TP18	TEST POINT, 1POS, 0.040" MTG. HOLE, 2.54mm DIA x 4.57mm L, THT, BLACK	KEYSTONE, 5001
7	4	XJP1, XJP2, XJP3, XJP4	CONN., SHUNT, FEMALE, 2 POS, 2mm	WURTH ELEKTRONIK, 60800213421

SCHEMATIC DIAGRAM



Rev. 0

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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