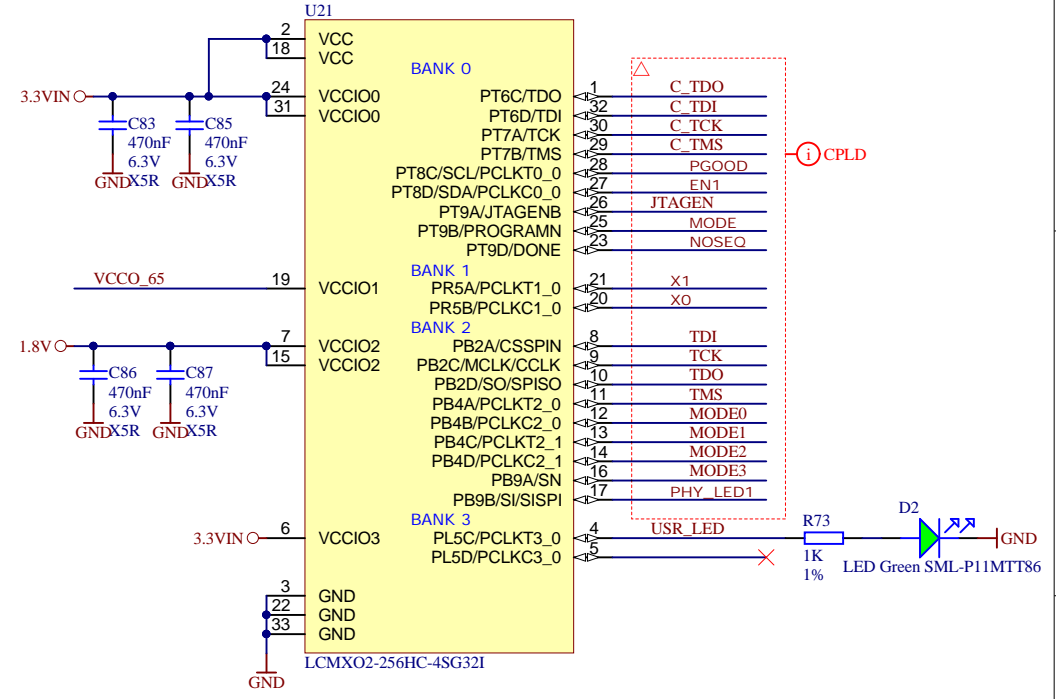
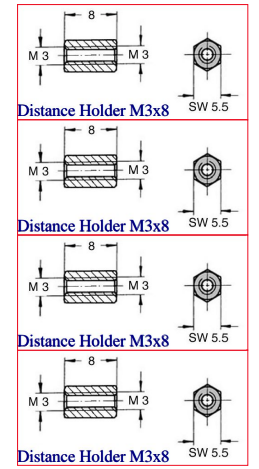
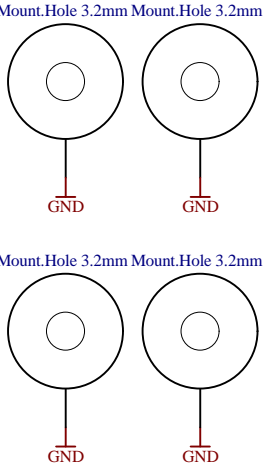
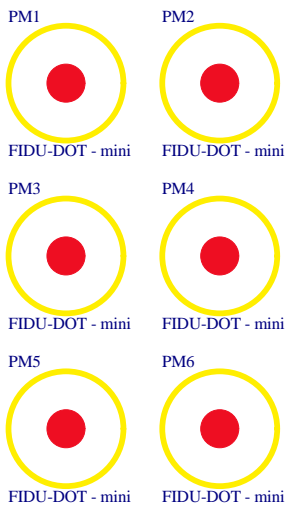
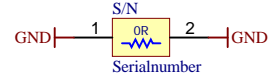


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U_ETH-PHY	ETH-PHY.SchDoc
U_B_HD	B_HD.SchDoc
U_B64	B64.SchDoc
U_B65	B65.SchDoc
U_B66	B66.SchDoc
U_CONFIG	CONFIG.SchDoc
U_B_MIO	B_MIO.SchDoc
U_B_PS_GT	B_PS_GT.SchDoc
U_CLK	CLK.SchDoc

U_B2B-Connectors	B2B-Connectors.SchDoc
U_eMMC	eMMC.SchDoc
U_PS_DDR	PS_DDR.SchDoc
U_ZU_POWER	ZU_POWER.SchDoc
U_ZU_PS_POWER	ZU_PS_POWER.SchDoc
U_DDR4-RAM_2	DDR4-RAM_2.SchDoc
U_DDR4-RAM	DDR4-RAM.SchDoc
U_POWER	POWER.SchDoc
U_POWER_1	POWER_1.SchDoc

Serial
Serialnumber 6,3 x 6.3mm



Assembly variant	04CG-1ED
Created by	VariantCreatedBy
Modified by	VariantModifiedBy
Modified at	VariantDateModification
SVN Revision	8646



Title: TE0820		
A4	Number: TE0820 04CG-1ED	Rev. 03
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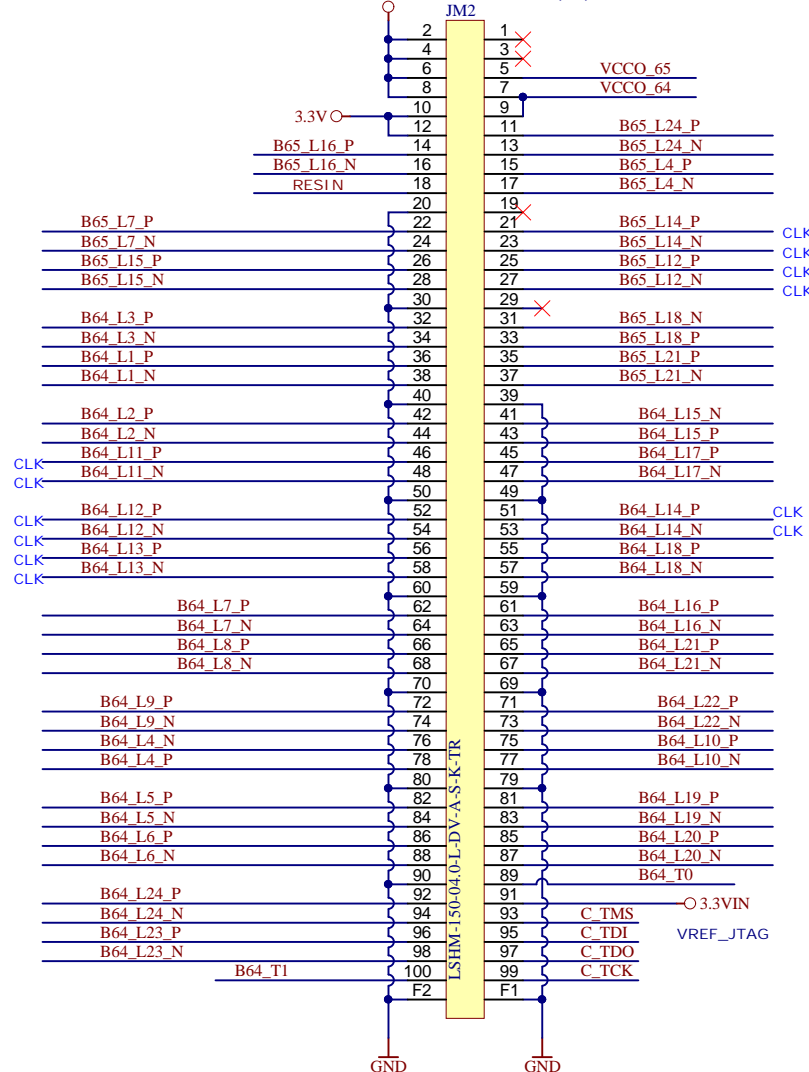
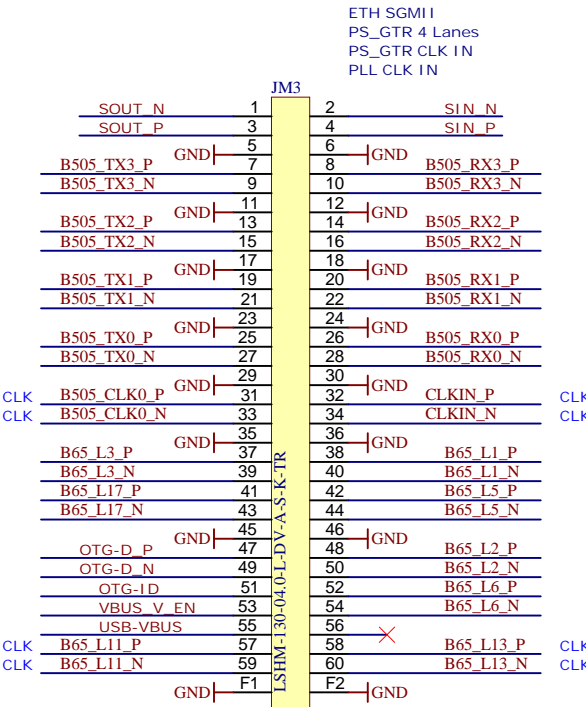
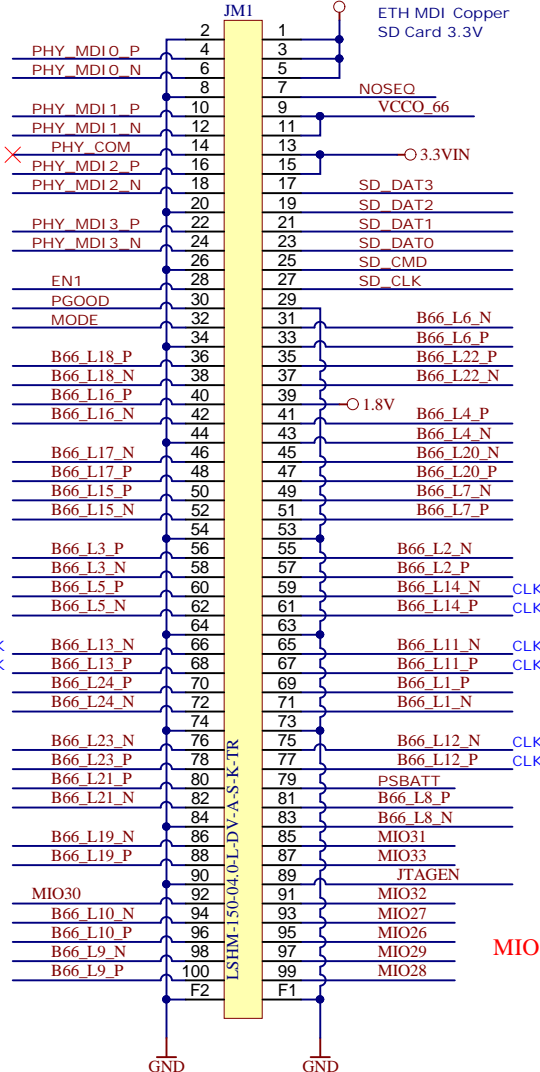
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D

B66(HP) 48 IO, 24 LVDS Pairs
 MIO501 8 IO, 3.3V
 ETH MDI Copper
 SD Card 3.3V

B65(HP) 16 IO, 8 LVDS Pairs
 USB OTG
 ETH SGMII
 PS_GTR 4 Lanes
 PS_GTR CLK IN
 PLL CLK IN

B65(HP) 18 IO, 9 LVDS Pairs
 B64(HP) 50 IO, 24 LVDS Pairs



VCCO64, VCCO65, VCCO66 ->>> max. 1.8V (HP bank's)

MIO[29..26] ->PJTAG1



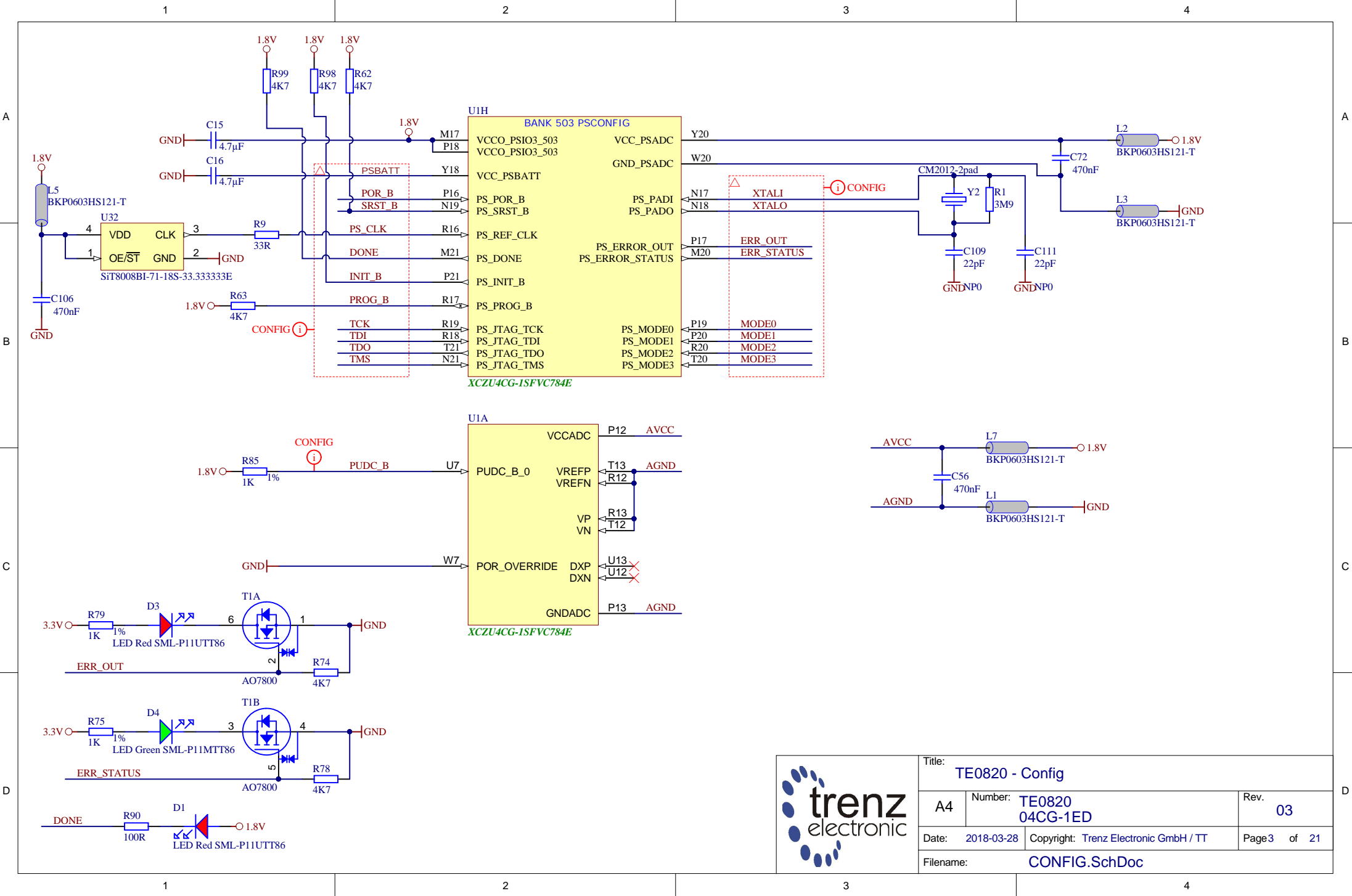
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Date: 2018-03-28	Copyright: 2015 Trenz Electronic GmbH	Page 2 of 21
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Title: TE0820 - Config		
A4	Number: TE0820 04CG-1ED	Rev. 03
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Filename: CONFIG.SchDoc		

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UIC

BANK 46 HD (ZU2/3 BANK 26 HD)

F14	VCCO_46	IO_L1P_AD11P_46	IO_L7P_HDGC_AD5P_46
C15	VCCO_46	IO_L1N_AD11N_46	IO_L7N_HDGC_AD5N_46
B15	IO_L1P_AD11P_46	IO_L2P_AD10P_46	IO_L8P_HDGC_AD4P_46
A15	IO_L1N_AD11N_46	IO_L2N_AD10N_46	IO_L8N_HDGC_AD4N_46
B14	IO_L2P_AD10P_46	IO_L3P_AD9P_46	IO_L9P_AD3P_46
A14	IO_L2N_AD10N_46	IO_L3N_AD9N_46	IO_L9N_AD3N_46
B13	IO_L3P_AD9P_46	IO_L4P_AD8P_46	IO_L10P_AD2P_46
A13	IO_L3N_AD9N_46	IO_L4N_AD8N_46	IO_L10N_AD2N_46
C14	IO_L4P_AD8P_46	IO_L5P_HDGC_AD7P_46	IO_L11P_AD1P_46
C13	IO_L4N_AD8N_46	IO_L5N_HDGC_AD7N_46	IO_L11N_AD1N_46
D15	IO_L5P_HDGC_AD7P_46	IO_L6P_HDGC_AD6P_46	IO_L12P_AD0P_46
D14	IO_L5N_HDGC_AD7N_46	IO_L6N_HDGC_AD6N_46	IO_L12N_AD0N_46
E14	IO_L6P_HDGC_AD6P_46		
E13	IO_L6N_HDGC_AD6N_46		

B26

B26

BANK 43 HD (ZU2/3 BANK 44 HD)

AC10	VCCO_43	IO_L1P_AD11P_43	IO_L7P_HDGC_AD5P_43
AG12	VCCO_43	IO_L1N_AD11N_43	IO_L7N_HDGC_AD5N_43
AG10	IO_L1P_AD11P_43	IO_L2P_AD10P_43	IO_L8P_HDGC_AD4P_43
AH10	IO_L1N_AD11N_43	IO_L2N_AD10N_43	IO_L8N_HDGC_AD4N_43
AF11	IO_L2P_AD10P_43	IO_L3P_AD9P_43	IO_L9P_AD3P_43
AG11	IO_L2N_AD10N_43	IO_L3N_AD9N_43	IO_L9N_AD3N_43
AH12	IO_L3P_AD9P_43	IO_L4P_AD8P_43	IO_L10P_AD2P_43
AH11	IO_L3N_AD9N_43	IO_L4N_AD8N_43	IO_L10N_AD2N_43
AE13	IO_L4P_AD8P_43	IO_L5P_HDGC_AD7P_43	IO_L11P_AD1P_43
AF10	IO_L4N_AD8N_43	IO_L5N_HDGC_AD7N_43	IO_L11N_AD1N_43
AE12	IO_L5P_HDGC_AD7P_43	IO_L6P_HDGC_AD6P_43	IO_L12P_AD0P_43
AF12	IO_L5N_HDGC_AD7N_43	IO_L6N_HDGC_AD6N_43	IO_L12N_AD0N_43
AC13	IO_L6P_HDGC_AD6P_43		
AD13	IO_L6N_HDGC_AD6N_43		

B44

B44

UIB

XCZU4CG-1SFVC784E

BANK 44 HD (ZU2/3 BANK 24 HD)

AA14	VCCO_44	IO_L1P_AD15P_44	IO_L7P_HDGC_44
AD13	VCCO_44	IO_L1N_AD15N_44	IO_L7N_HDGC_44
AE15	IO_L1P_AD15P_44	IO_L2P_AD14P_44	IO_L8P_HDGC_44
AE14	IO_L1N_AD15N_44	IO_L2N_AD14N_44	IO_L8N_HDGC_44
AG14	IO_L2P_AD14P_44	IO_L3P_AD13P_44	IO_L9P_AD11P_44
AH14	IO_L2N_AD14N_44	IO_L3N_AD13N_44	IO_L9N_AD11N_44
AG13	IO_L3P_AD13P_44	IO_L4P_AD12P_44	IO_L10P_AD10P_44
AH13	IO_L3N_AD13N_44	IO_L4N_AD12N_44	IO_L10N_AD10N_44
AF13	IO_L4P_AD12P_44	IO_L5P_HDGC_44	IO_L11P_AD9P_44
AD13	IO_L4N_AD12N_44	IO_L5N_HDGC_44	IO_L11N_AD9N_44
AC14	IO_L5P_HDGC_44	IO_L6P_HDGC_44	IO_L12P_AD8P_44
AC13	IO_L5N_HDGC_44	IO_L6N_HDGC_44	IO_L12N_AD8N_44

B24

B24

BANK 45 HD (ZU2/3 BANK 25 HD)

B12	VCCO_45	IO_L1P_AD15P_45	IO_L7P_HDGC_45
E11	VCCO_45	IO_L1N_AD15N_45	IO_L7N_HDGC_45
J11	IO_L1P_AD15P_45	IO_L2P_AD14P_45	IO_L8P_HDGC_45
J10	IO_L1N_AD15N_45	IO_L2N_AD14N_45	IO_L8N_HDGC_45
K13	IO_L2P_AD14P_45	IO_L3P_AD13P_45	IO_L9P_AD11P_45
K12	IO_L2N_AD14N_45	IO_L3N_AD13N_45	IO_L9N_AD11N_45
H13	IO_L3P_AD13P_45	IO_L4P_AD12P_45	IO_L10P_AD10P_45
G10	IO_L3N_AD13N_45	IO_L4N_AD12N_45	IO_L10N_AD10N_45
J12	IO_L4P_AD12P_45	IO_L5P_HDGC_45	IO_L11P_AD9P_45
H12	IO_L4N_AD12N_45	IO_L5N_HDGC_45	IO_L11N_AD9N_45
G11	IO_L5P_HDGC_45	IO_L6P_HDGC_45	IO_L12P_AD8P_45
F12	IO_L5N_HDGC_45	IO_L6N_HDGC_45	IO_L12N_AD8N_45
F11	IO_L6P_HDGC_45		
F10	IO_L6N_HDGC_45		

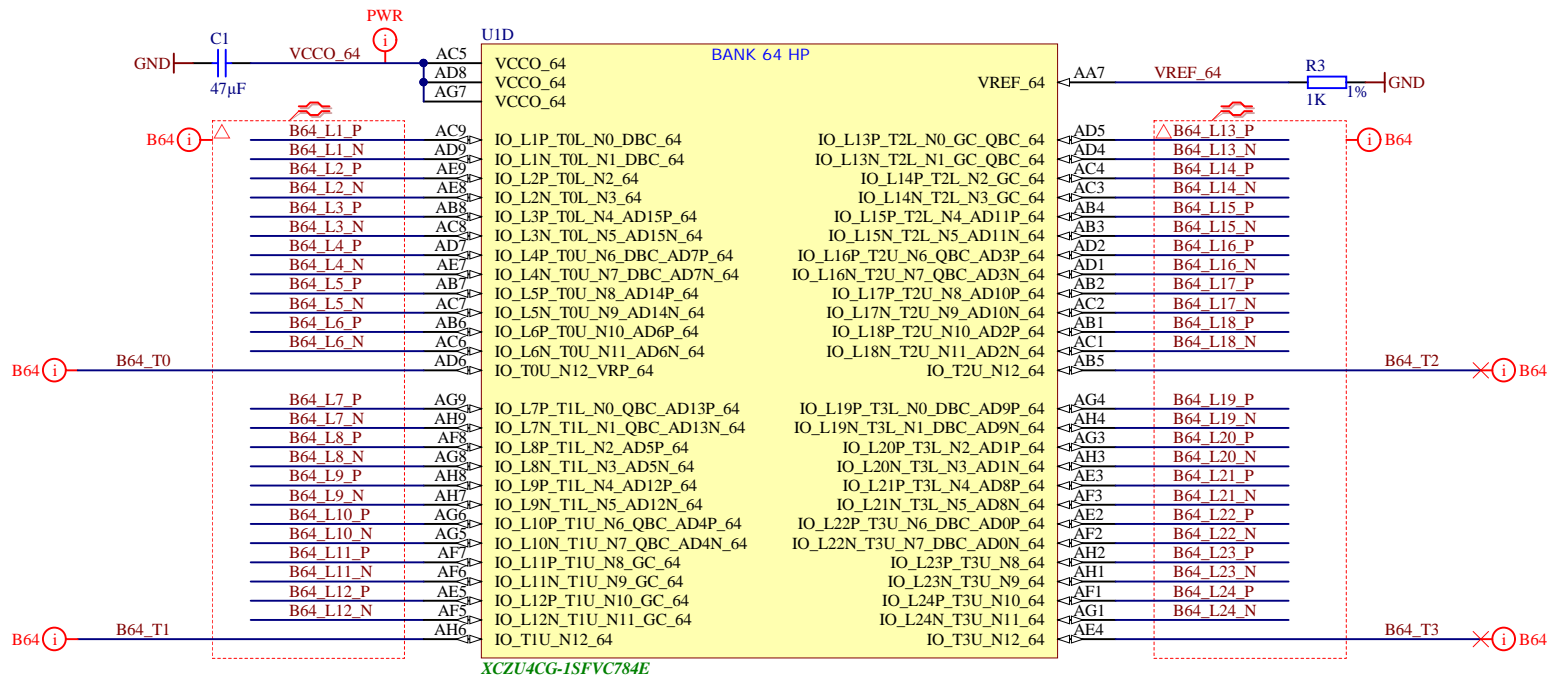
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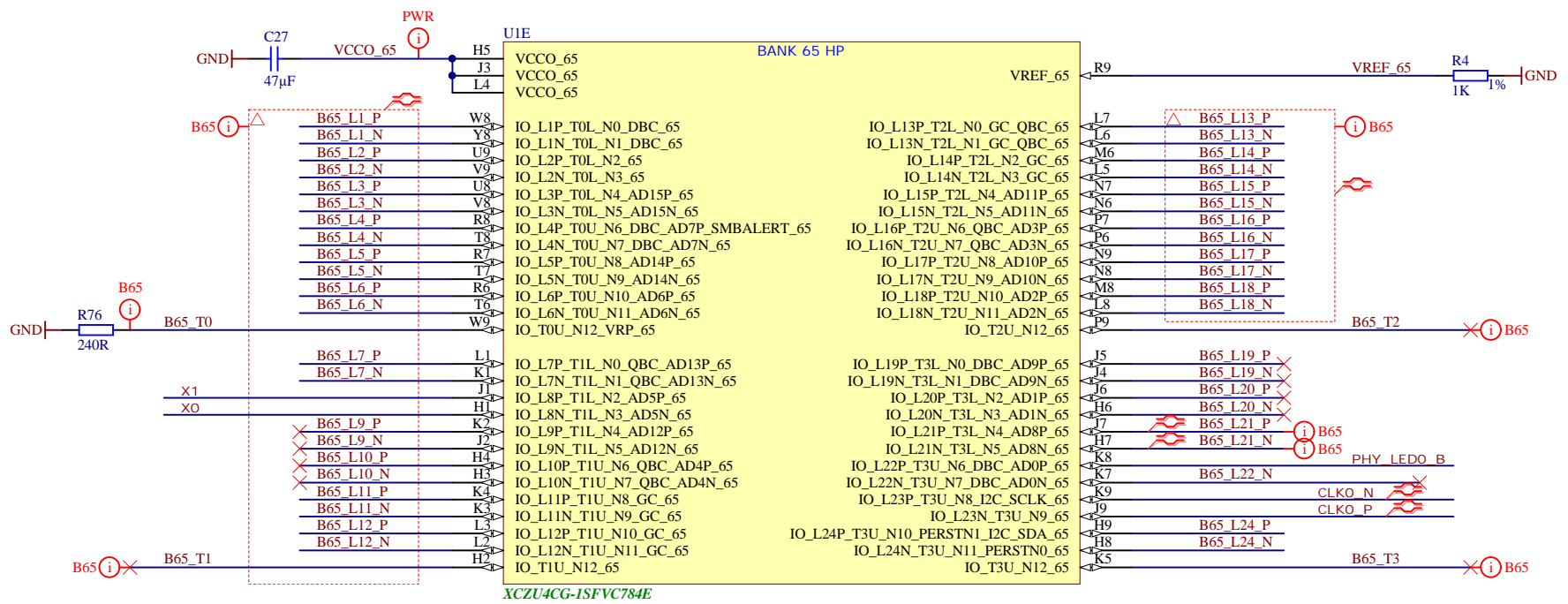
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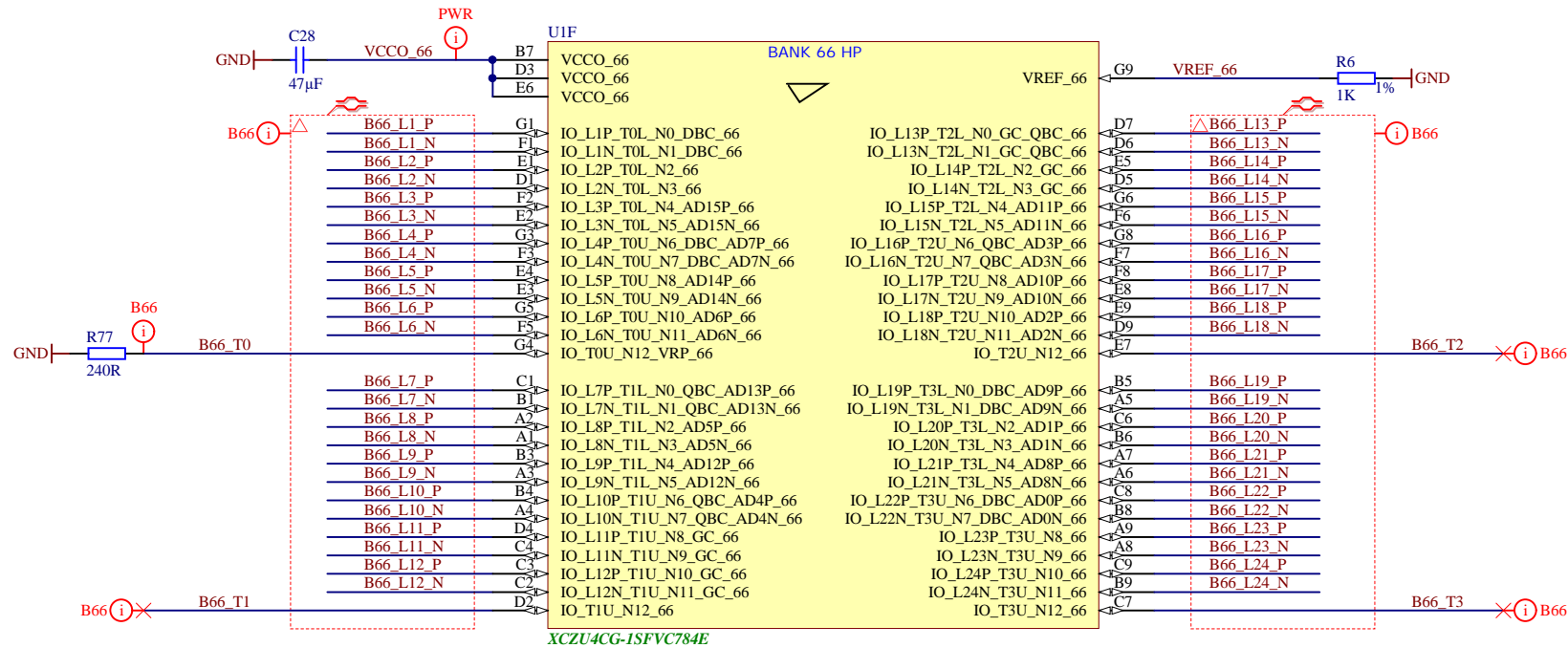
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Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 4 of 21
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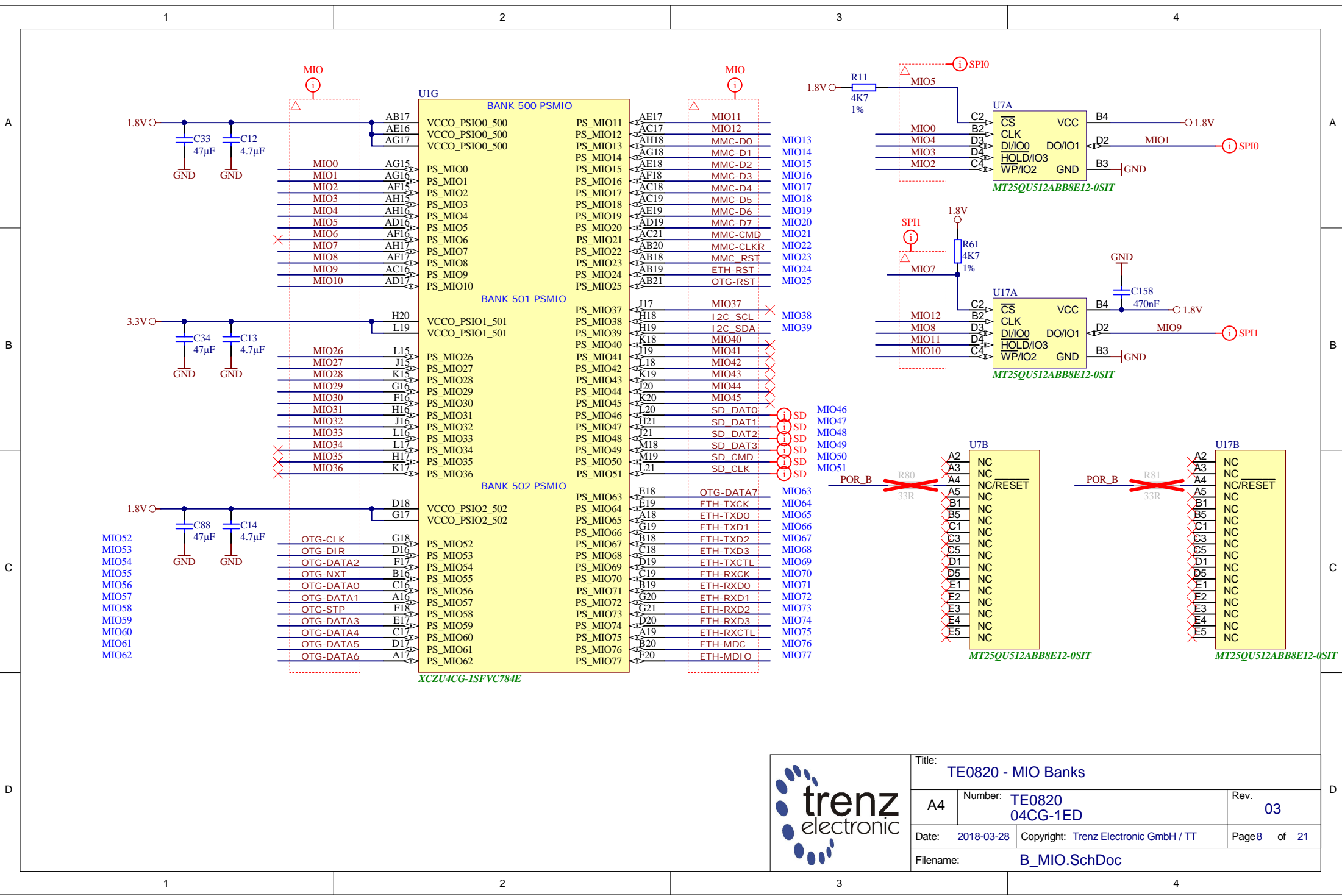
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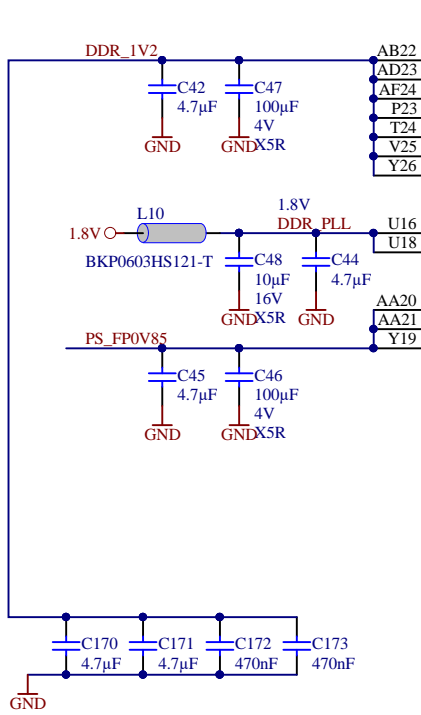
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Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 7 of 21
Filename: B66.SchDoc		



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			A4	Number: TE0820 04CG-1ED
Date: 2018-03-28		Copyright: Trenz Electronic GmbH / TT		Page 8 of 21
Filename: B_MIO.SchDoc				



U11

BANK 504 PSDDR

VCCO_PSDDR_504	PS_DDR_CK0	W25	DDR4-CLK0_P
VCCO_PSDDR_504	PS_DDR_CK0_N0	W26	DDR4-CLK0_N
VCCO_PSDDR_504	PS_DDR_CKE0	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1	V27	
VCC_PSDDR_PLL	PS_DDR_A0	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2	AB28	DDR4-A2
VCC_PSINTFP_DDR	PS_DDR_A3	AA28	DDR4-A3
VCC_PSINTFP_DDR	PS_DDR_A4	Y27	DDR4-A4
VCC_PSINTFP_DDR	PS_DDR_A5	AA27	DDR4-A5
VCC_PSINTFP_DDR	PS_DDR_A6	Y22	DDR4-A6
VCC_PSINTFP_DDR	PS_DDR_A7	AA23	DDR4-A7
VCC_PSINTFP_DDR	PS_DDR_A8	AA22	DDR4-A8
VCC_PSINTFP_DDR	PS_DDR_A9	AB23	DDR4-A9
VCC_PSINTFP_DDR	PS_DDR_A10	AA25	DDR4-A10
VCC_PSINTFP_DDR	PS_DDR_A11	AA26	DDR4-A11
VCC_PSINTFP_DDR	PS_DDR_A12	AB25	DDR4-A12
VCC_PSINTFP_DDR	PS_DDR_A13	AB26	DDR4-A13
VCC_PSINTFP_DDR	PS_DDR_A14	AB24	DDR4-A14
VCC_PSINTFP_DDR	PS_DDR_A15	AC24	DDR4-A15
VCC_PSINTFP_DDR	PS_DDR_A16	AC23	DDR4-A16
VCC_PSINTFP_DDR	PS_DDR_A17	AC22	DDR4-A17
PS_DDR_CS_N0	PS_DDR_CS_N1	W27	DDR4-CS
PS_DDR_CS_N0	PS_DDR_CS_N1	V26	
PS_DDR_BA0	PS_DDR_BA1	V23	DDR4-BA0
PS_DDR_BA0	PS_DDR_BA1	W22	DDR4-BA1
PS_DDR_BG0	PS_DDR_BG1	W24	DDR4-BG0
PS_DDR_BG0	PS_DDR_BG1	V22	
PS_DDR_PARITY	PS_DDR_RAM_RST_N	Y24	DDR4-PAR
PS_DDR_RAM_RST_N	PS_DDR_ACT_N	U23	DDR4-RESET
PS_DDR_ACT_N	PS_DDR_ALERT_N	Y23	DDR4-ACT
PS_DDR_ALERT_N		U25	DDR4-ALERT
PS_DDR_ZQ		U24	
PS_DDR_ODT0	PS_DDR_ODT1	U28	DDR4-ODT0
PS_DDR_ODT0	PS_DDR_ODT1	U26	

XCZU4CG-1SFVC784E



U1J

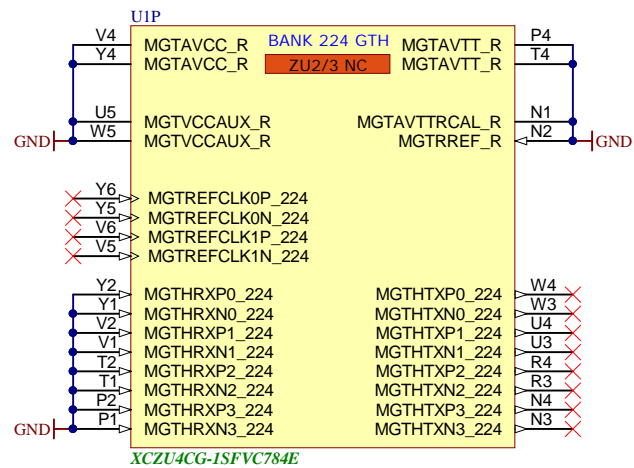
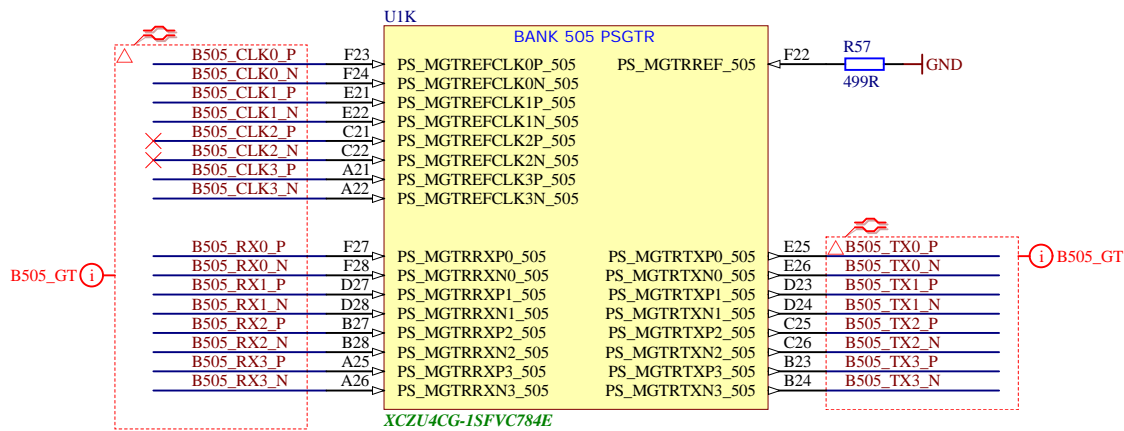
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DQ1	AE20	PS_DDR_DQ1	PS_DDR_DQ33	R22
DQ2	AD20	PS_DDR_DQ2	PS_DDR_DQ34	P22
DQ3	AF20	PS_DDR_DQ3	PS_DDR_DQ35	N22
DQ4	AH21	PS_DDR_DQ4	PS_DDR_DQ36	T23
DQ5	AH20	PS_DDR_DQ5	PS_DDR_DQ37	P24
DQ6	AH19	PS_DDR_DQ6	PS_DDR_DQ38	R24
DQ7	AG19	PS_DDR_DQ7	PS_DDR_DQ39	N24
DQ8	AF22	PS_DDR_DQ8	PS_DDR_DQ40	H24
DQ9	AH22	PS_DDR_DQ9	PS_DDR_DQ41	J24
DQ10	AE22	PS_DDR_DQ10	PS_DDR_DQ42	M24
DQ11	AD22	PS_DDR_DQ11	PS_DDR_DQ43	K24
DQ12	AH23	PS_DDR_DQ12	PS_DDR_DQ44	J22
DQ13	AH24	PS_DDR_DQ13	PS_DDR_DQ45	H22
DQ14	AE24	PS_DDR_DQ14	PS_DDR_DQ46	K22
DQ15	AG24	PS_DDR_DQ15	PS_DDR_DQ47	L22
DQ16	AC26	PS_DDR_DQ16	PS_DDR_DQ48	M25
DQ17	AD26	PS_DDR_DQ17	PS_DDR_DQ49	M26
DQ18	AD25	PS_DDR_DQ18	PS_DDR_DQ50	L25
DQ19	AD24	PS_DDR_DQ19	PS_DDR_DQ51	L26
DQ20	AG26	PS_DDR_DQ20	PS_DDR_DQ52	K28
DQ21	AH25	PS_DDR_DQ21	PS_DDR_DQ53	L28
DQ22	AH26	PS_DDR_DQ22	PS_DDR_DQ54	M28
DQ23	AG25	PS_DDR_DQ23	PS_DDR_DQ55	N28
DQ24	AH27	PS_DDR_DQ24	PS_DDR_DQ56	J28
DQ25	AH28	PS_DDR_DQ25	PS_DDR_DQ57	K27
DQ26	AF28	PS_DDR_DQ26	PS_DDR_DQ58	H28
DQ27	AG28	PS_DDR_DQ27	PS_DDR_DQ59	H27
DQ28	AC27	PS_DDR_DQ28	PS_DDR_DQ60	G26
DQ29	AD27	PS_DDR_DQ29	PS_DDR_DQ61	G25
DQ30	AD28	PS_DDR_DQ30	PS_DDR_DQ62	K25
DQ31	AC28	PS_DDR_DQ31	PS_DDR_DQ63	J25
DDR4-DQS0_P	AF21	PS_DDR_DQS_P0	PS_DDR_DQ64	T28
DDR4-DQS0_N	AG21	PS_DDR_DQS_N0	PS_DDR_DQ65	R28
DDR4-DQS1_P	AF23	PS_DDR_DQS_P1	PS_DDR_DQ66	P28
DDR4-DQS1_N	AG23	PS_DDR_DQS_N1	PS_DDR_DQ67	P27
DDR4-DQS2_P	AF25	PS_DDR_DQS_P2	PS_DDR_DQ68	P26
DDR4-DQS2_N	AF26	PS_DDR_DQS_N2	PS_DDR_DQ69	R25
DDR4-DQS3_P	AE27	PS_DDR_DQS_P3	PS_DDR_DQ70	P25
DDR4-DQS3_N	AE27	PS_DDR_DQS_N3	PS_DDR_DQ71	T25
PS_DDR_DQS_P4	N23	PS_DDR_DM0	AG20	DDR4-DM0
PS_DDR_DQS_N4	M23	PS_DDR_DM1	AE23	DDR4-DM1
PS_DDR_DQS_P5	L23	PS_DDR_DM2	AE25	DDR4-DM2
PS_DDR_DQS_N5	K23	PS_DDR_DM3	AE28	DDR4-DM3
PS_DDR_DQS_P6	N26	PS_DDR_DM4	R23	
PS_DDR_DQS_N6	N27	PS_DDR_DM5	R23	
PS_DDR_DQS_P7	J26	PS_DDR_DM6	H23	
PS_DDR_DQS_N7	J27	PS_DDR_DM7	L27	
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PS_DDR_DQS_N8	T27		T26	

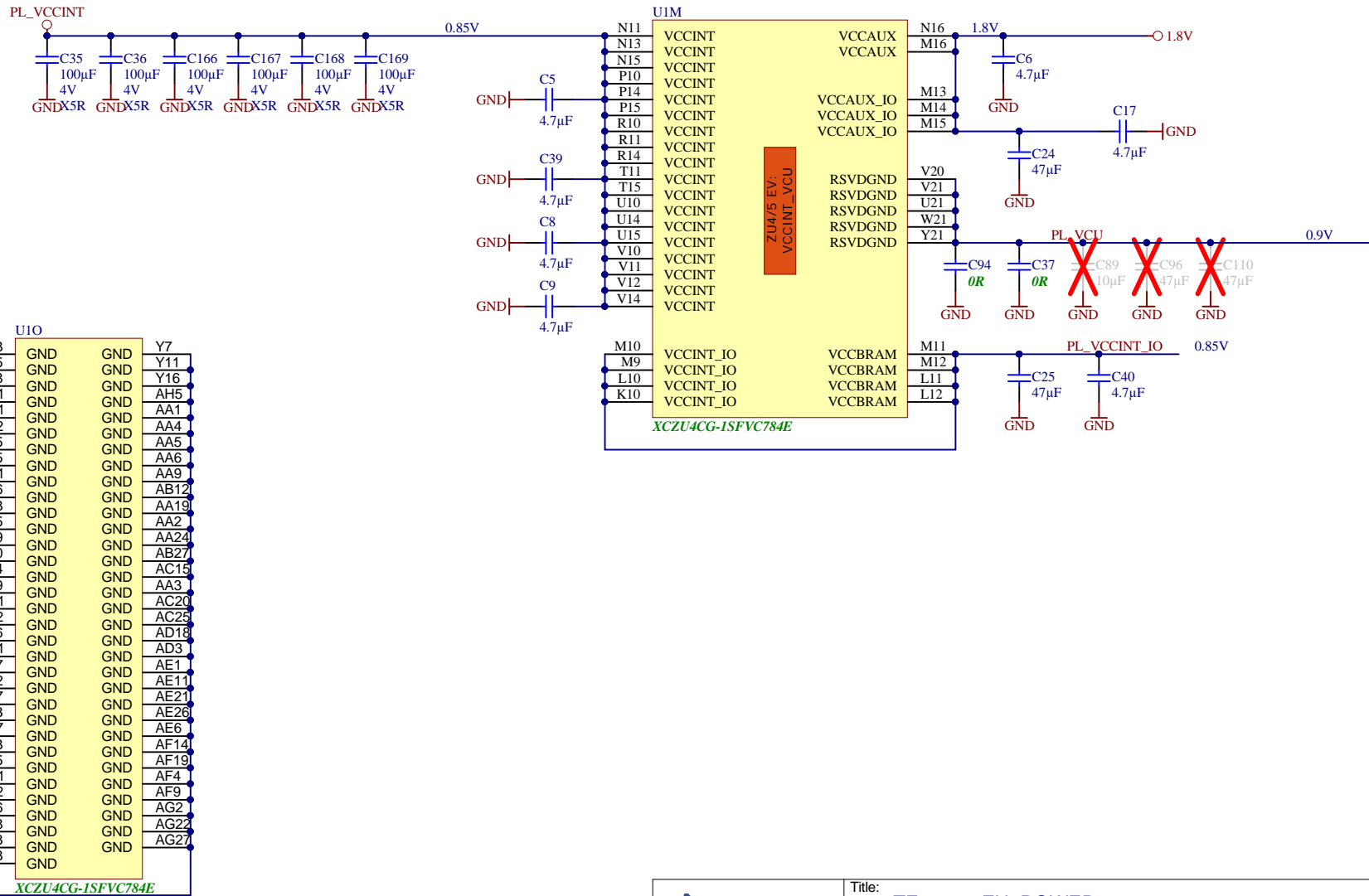
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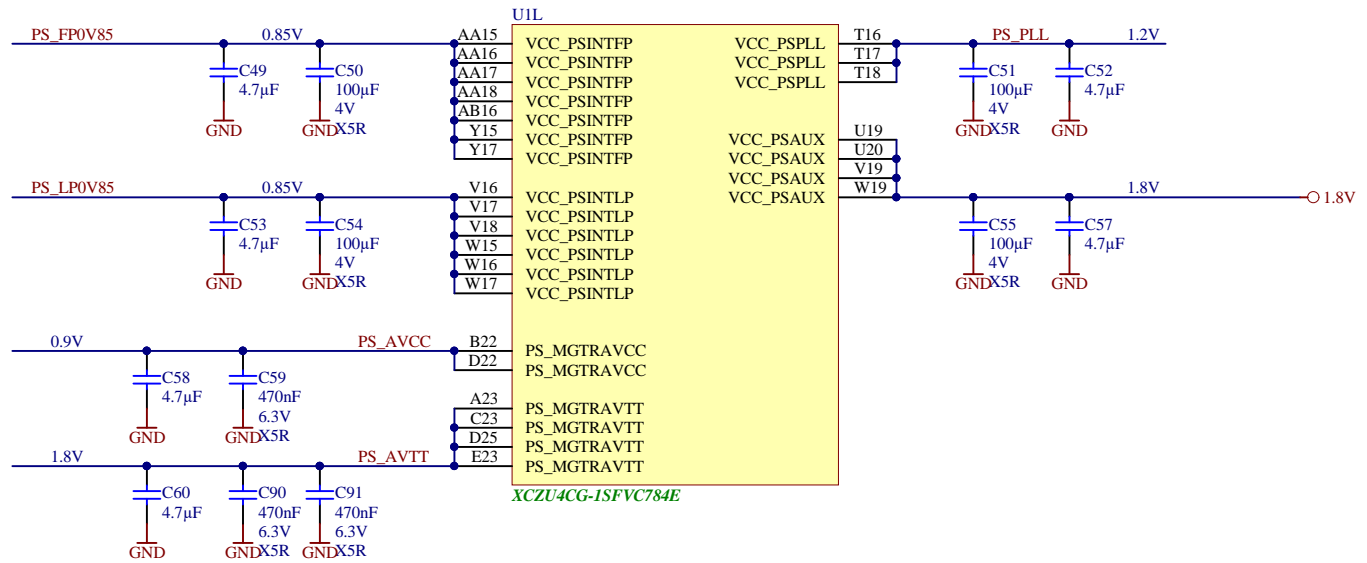
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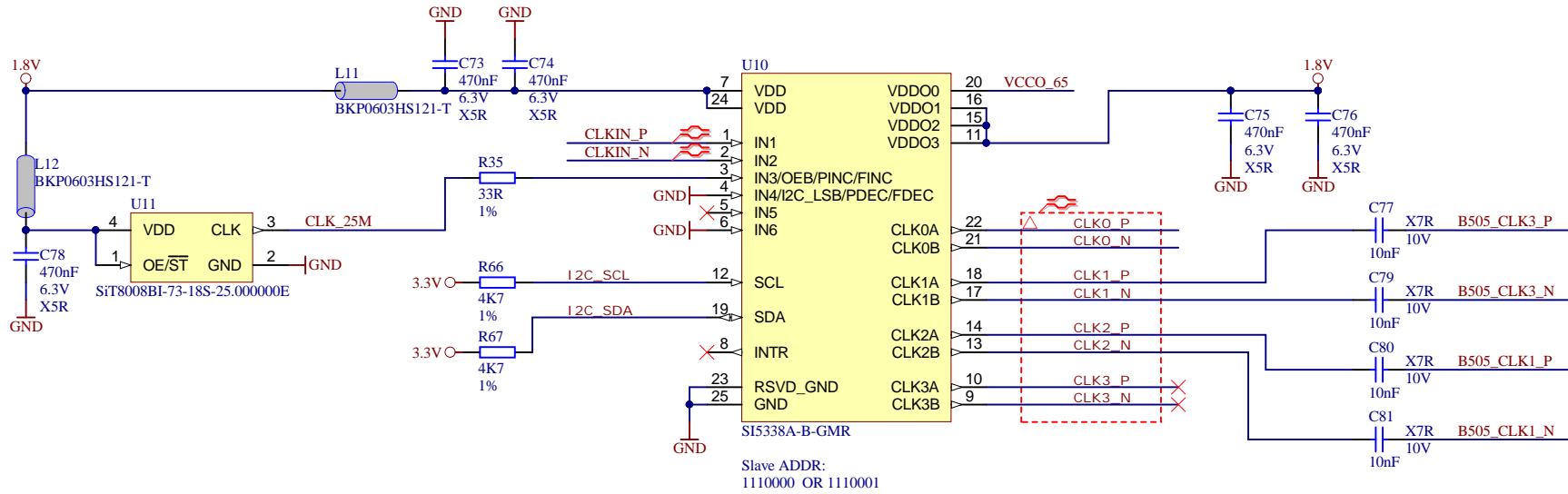
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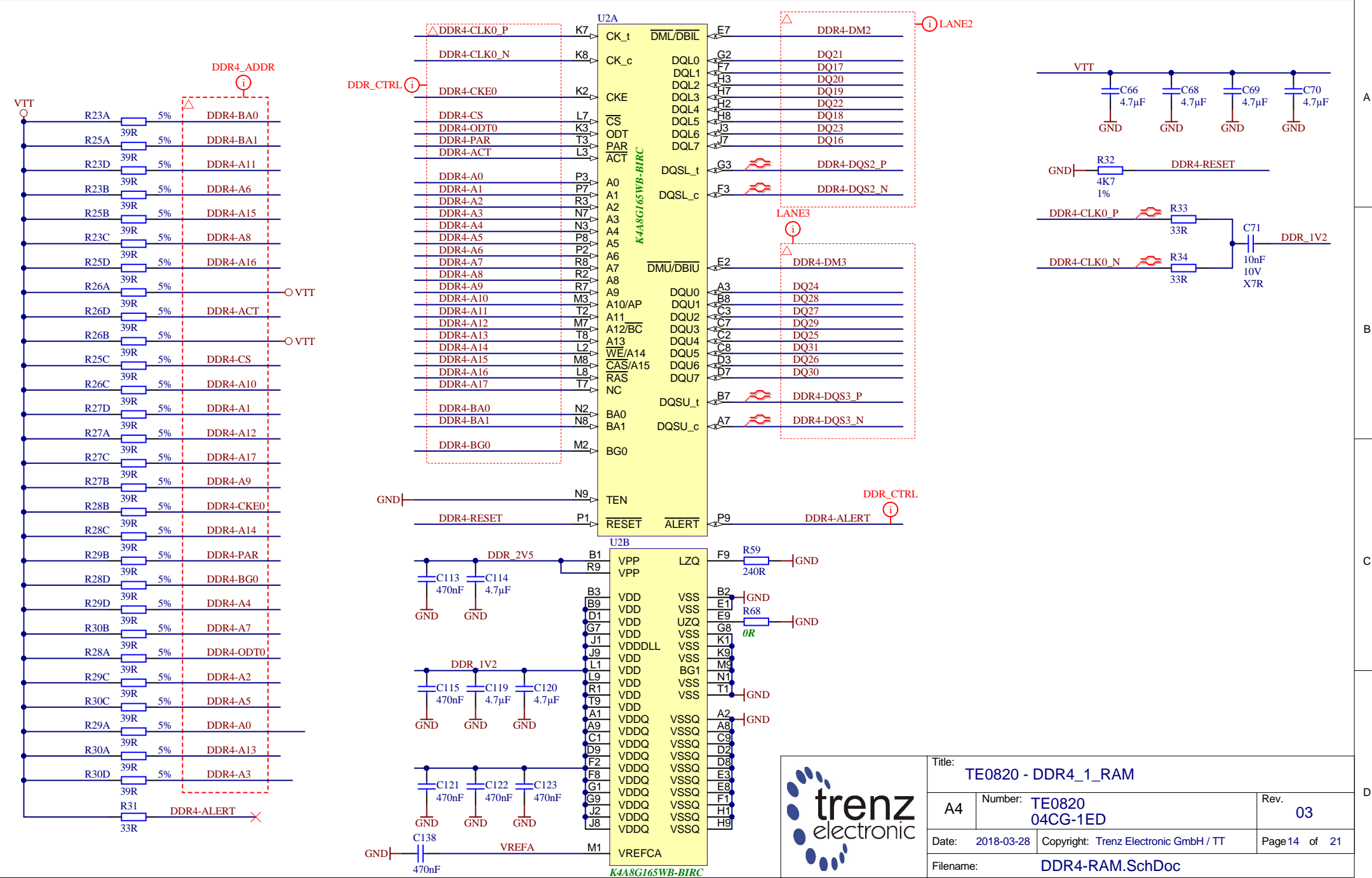
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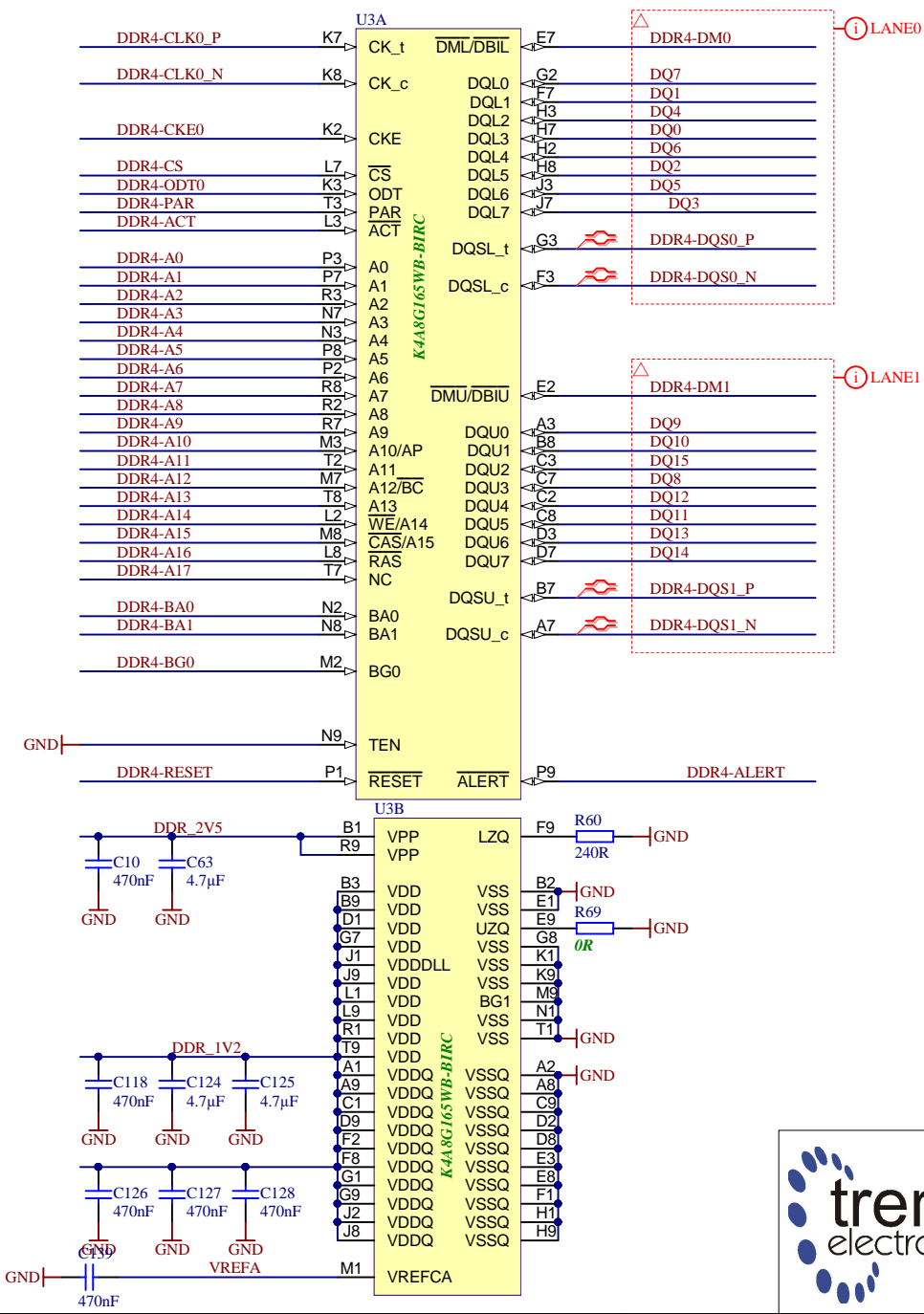

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Date: 2018-03-28		Page 12 of 21	
Filename: ZU_PS_POWER.SchDoc			



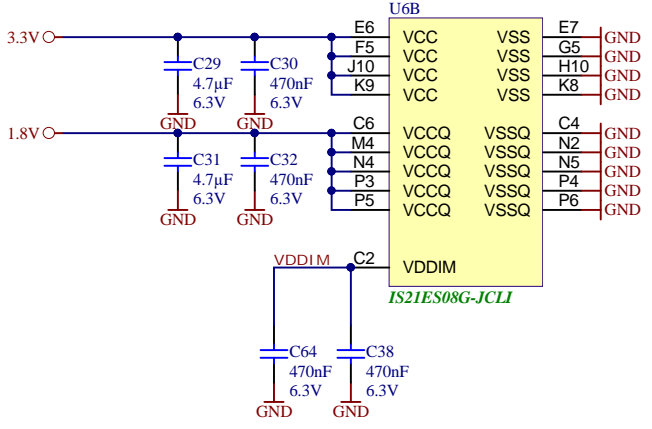
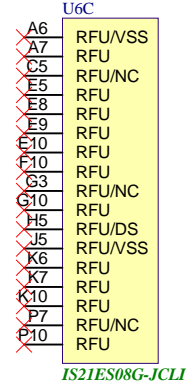
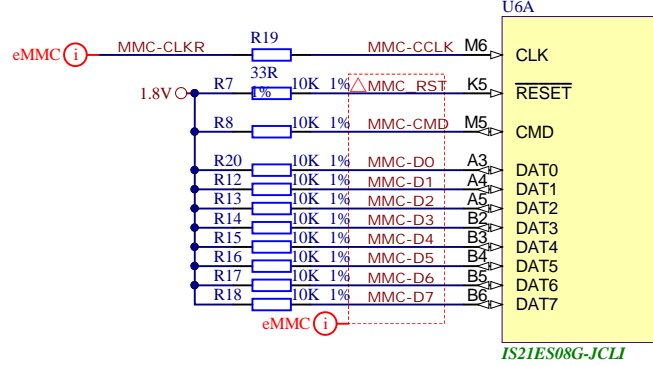
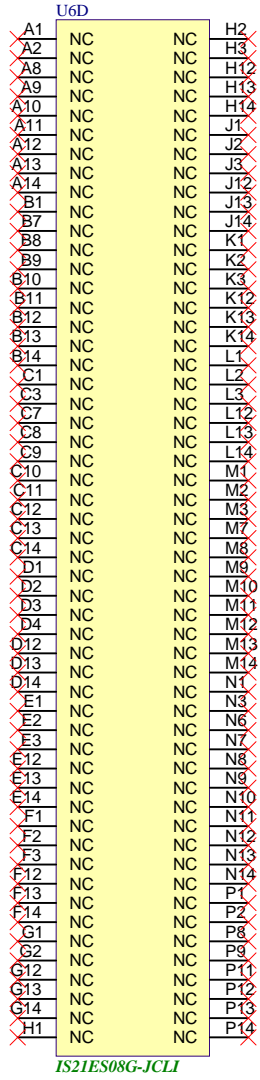
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		A4	Number: TE0820 04CG-1ED
Date: 2018-03-28		Copyright: 2015 Trenz Electronic GmbH	
Filename: CLK.SchDoc		Page 13 of 21	



Title: TE0820 - DDR4_1_RAM		
A4	Number: TE0820 04CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 14 of 21
Filename: DDR4-RAM.SchDoc		

Title: TE0820 - DDR4_2_RAM		
A4	Number: TE0820 04CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 15 of 21
Filename: DDR4-RAM_2.SchDoc		



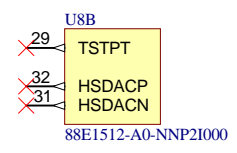
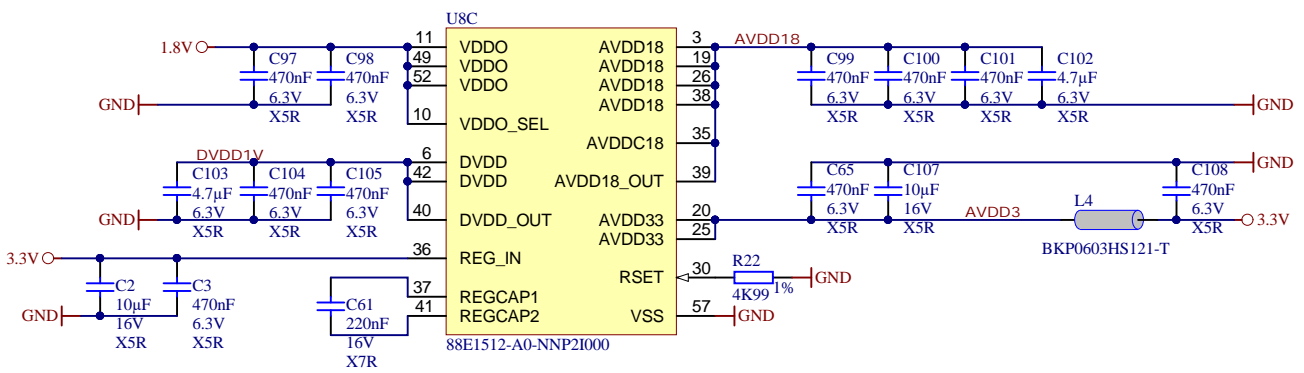
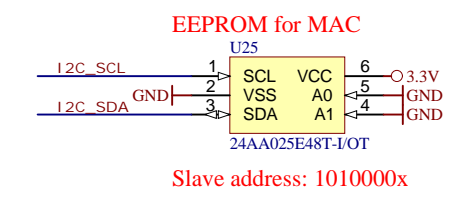
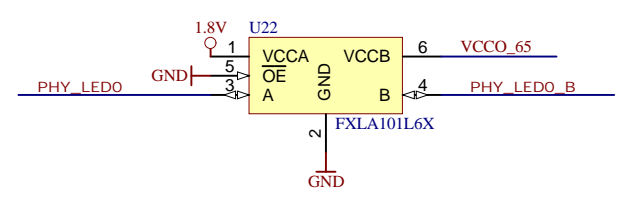
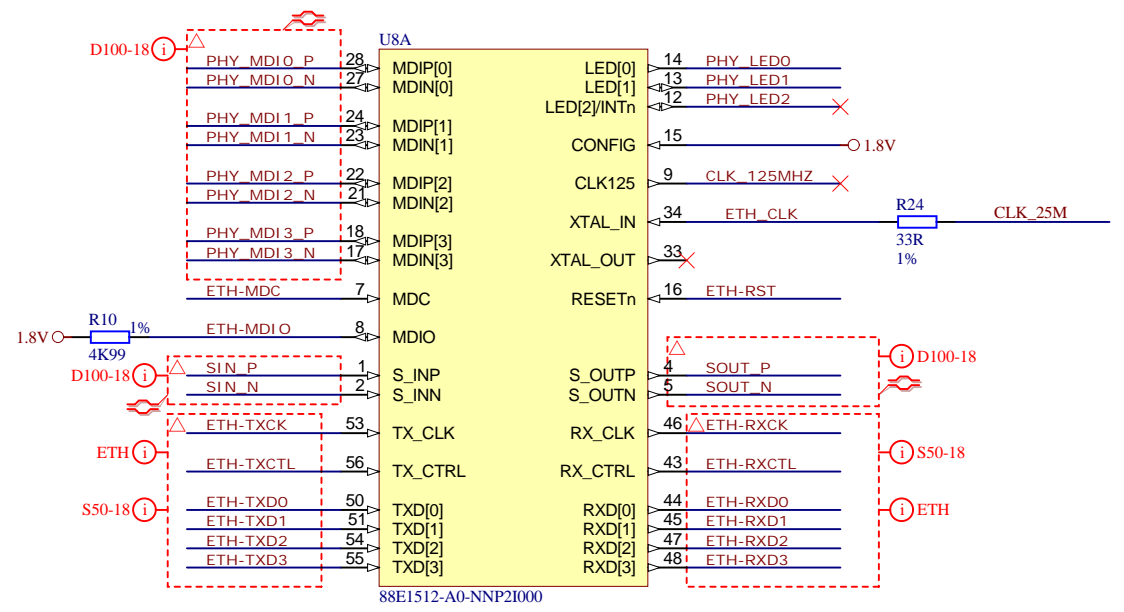
Title: TE0820 - eMMC		
A4	Number: TE0820 04CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 16 of 21
Filename: eMMC.SchDoc		

A

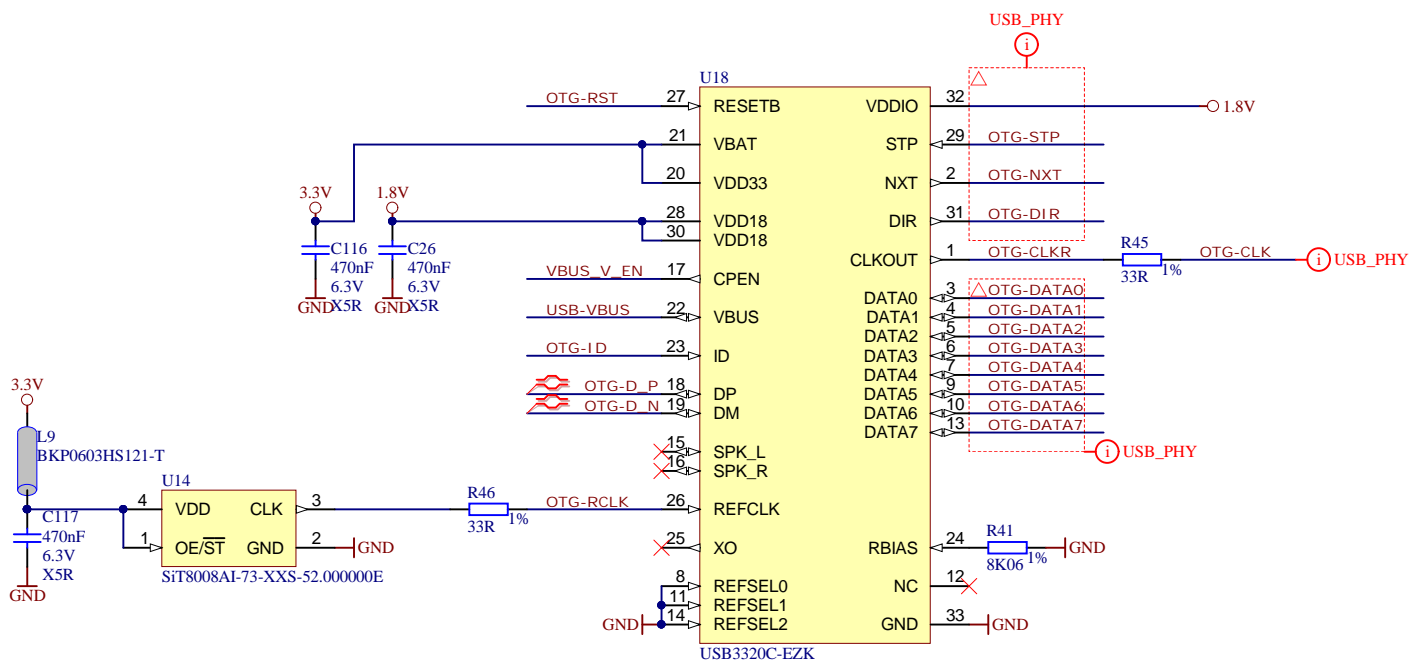
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C

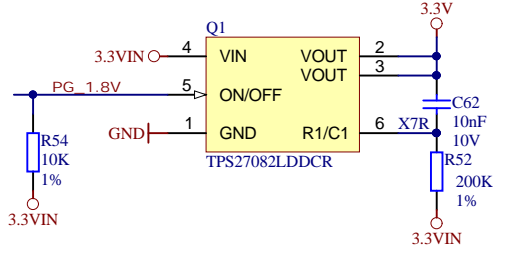
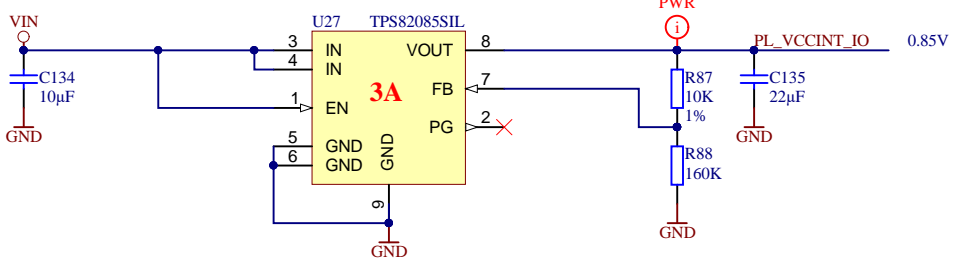
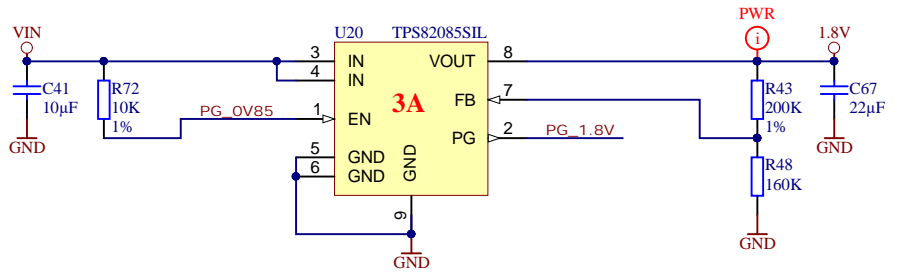
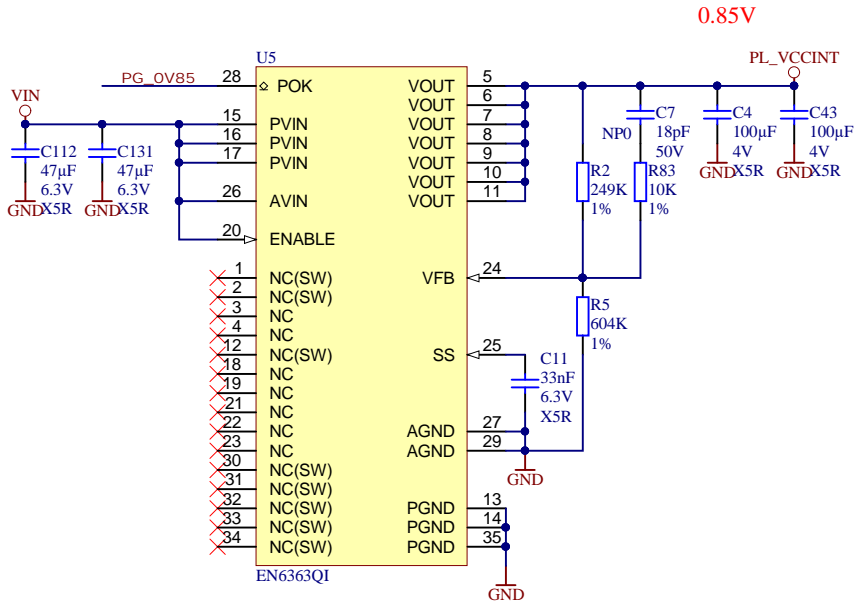
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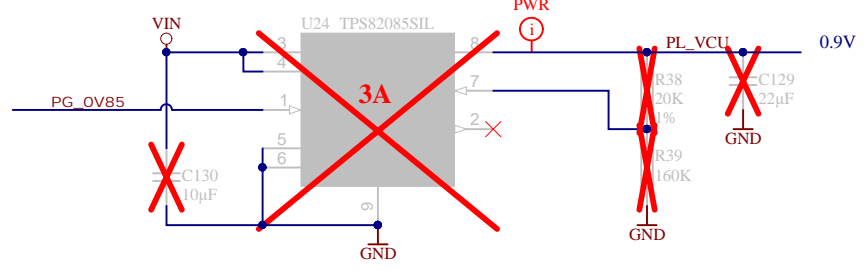
Title: TE0820 - Eth_PHY		
A4	Number: TE0820 04CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: 2015 Trenz Electronic GmbH	Page 17 of 21
Filename: ETH-PHY.SchDoc		



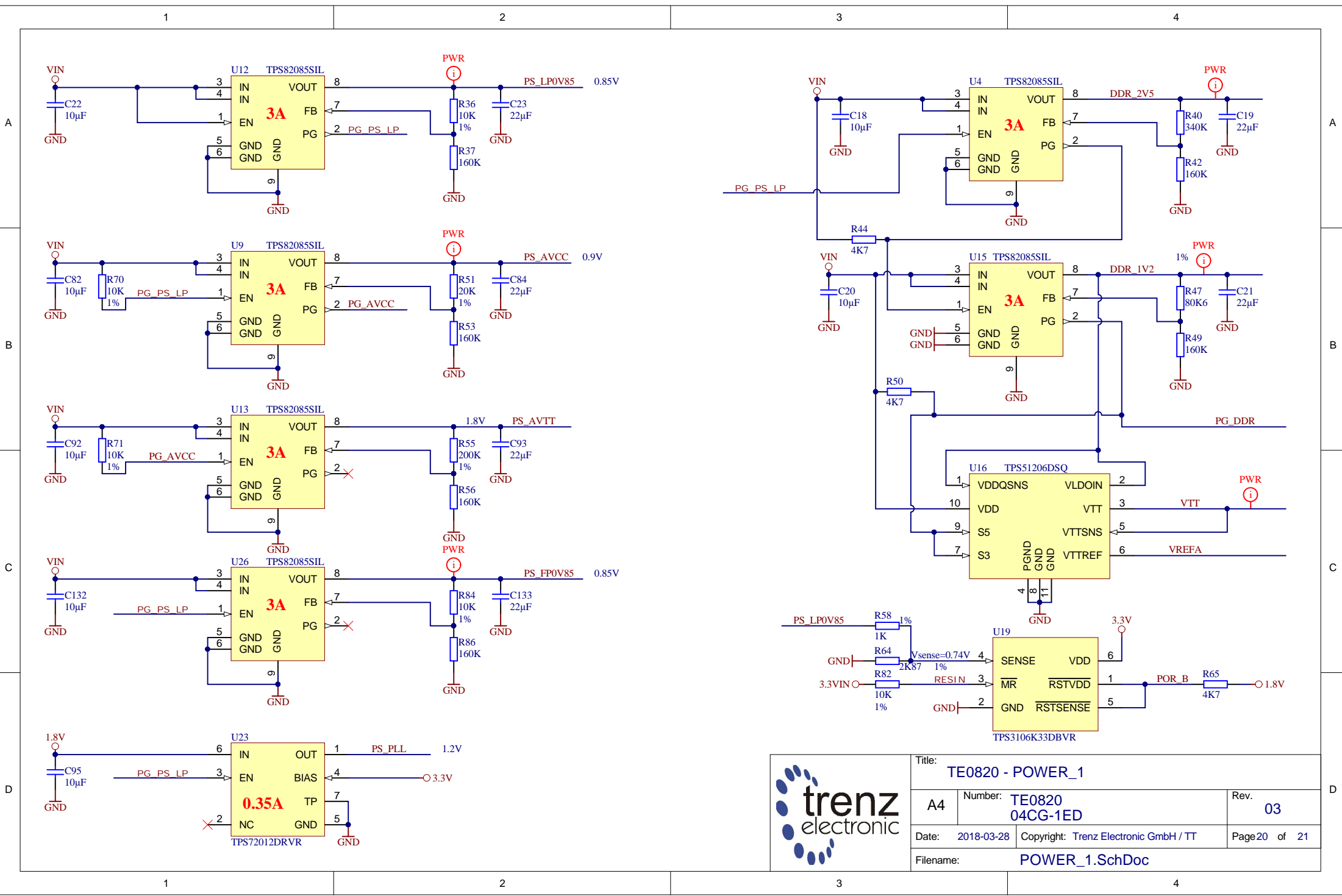
		Title: TE0820 - USB_PHY	
		A4	Number: TE0820 04CG-1ED
Date: 2018-03-28		Copyright: 2015 Trenz Electronic GmbH	
Filename: USB-PHY.SchDoc		Page 18 of 21	




NOTE: in variants with VCU R38 was 40.2K, this has been corrected to 20K (Xilinx documentation DS925) for further details just see Design Note Number: DN-20200904 <https://wiki.trenz-electronic.de/display/PD/Design+Note+TE0820-03+with+Video+Codec++++EV>



Title: TE0820 - POWER		
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			Title: TE0820 - POWER_1	
			A4	Number: TE0820 04CG-1ED
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Filename: POWER_1.SchDoc				


CHANGES REV01 to REV02

- 1) Added MAC EEPROM (slave address:)
- 2) LIB components update
- 3) Fixed SD Card connection
- 4) Fixed sense connection from DCDC
- 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
- 6) Added resistors for variants (ZU+ with/without VCU)
- 7) Added termination resistors (240R) to VRP pins fro all HP-banks

CHANGES REV02 to REV03

- 1) Fixed VCU connection: add additional DCDC (0.9V)
- 2) LIB components update
- 3) Change package 1K resistors (0402 -> 0201)
- 4) Added LEDs (1x user LED, 1x LED for ERR_STATUS, 1xLED for ERR_OUT)
- 5) Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit)
- 6) Added additional DCDCs (PL_VCCINT_IO, PS_FP0V85)
- 7) Changed DCDC (U5) 6A (optional 4A)

Design Note Number: DN-20200904 (<https://wiki.trenz-electronic.de/display/PD/Design+Note+TE0820-03+with+Video+Codec+++EV>)
 The internal supply voltage for the video codec unit (VCU) is set via Resistors R38 and R39. For the above mentioned affected SoMs R38 is set to 40.2 kOhm resulting in a PL_VCU voltage of 1.0V. This is above the recommended operation specification.
 Up to the issue date of this design note no adverse effects have been reported. For all serial numbers not mentioned under affected products R38 is 20 kOhm resulting in xilinx recommended 0.9V internal VCU voltage.
 If your product is affected and revision is required please contact sales@trenz-electronic.de (subject = DN-20200904) for further instructions.

		Title: TE0820 - Revision Changes		
		A4	Number: TE0820 04CG-1ED	Rev. 03
		Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 21 of 21
		Filename: Revision Changes.SchDoc		