TPS61197 Single-String White-LED Driver for LCD TV

1 Features

- 8-V to 30-V Input Voltage
- 50-kHz to 800-kHz Programmable Switching Frequency
- Adaptive Boost Output to White-LED Voltage
- High-Precision PWM Dimming Resolution up to 5000:1
- Programmable Overvoltage Protection Threshold at Output
- Programmable Undervoltage Threshold at Input with Adjustable Hysteresis
- Adjustable Soft-Start Time Independent of Dimming Duty Cycle
- Built-in LED Open and IFB Short Protections
- Built-in Schottky Diode Open/Short Protection
- Thermal Shutdown

2 Applications

- LCD TV Backlight
- Large LCD TV Displays
- Monitors

3 Description

The TPS61197 provides highly integrated solutions for LCD TV backlighting. This device is a current-mode boost controller driving one WLED string with multiple LEDs in series. The TPS61197 adjusts the output voltage of the boost controller automatically to provide only the minimum voltage required by the LED string to generate the setting LED current, thereby optimizing the efficiency of the driver.

The device supports direct PWM brightness dimming method. During the pulse-width modulation (PWM) dimming, the white LED current is turned on and off at the duty cycle and frequency, which are determined by an external PWM signal. The PWM dimming frequency ranges from 90 Hz to 22 kHz.

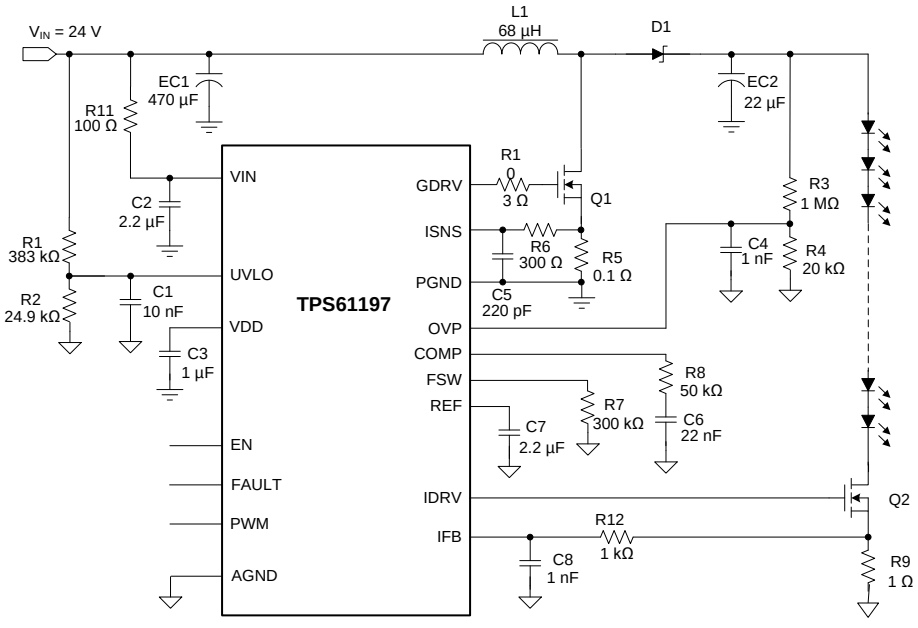
The TPS61197 integrates overcurrent protection, output short-circuit protection, Schottky diode open and short protection, LED open protection, LED-string short protection, and overtemperature shutdown circuit. The device also provides programmable input undervoltage lockout (UVLO) threshold and output overvoltage protection (OVP) threshold. The device is available in a 16-pin SOIC package, which is ideal for a single-layer PCB board.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61197	SOIC (16)	17.90 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2016) to Revision B **Page**

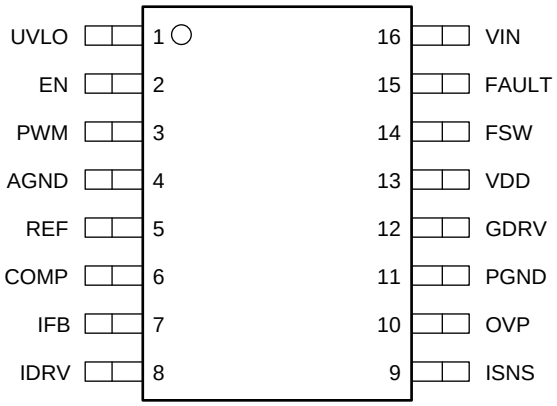
- Changed R5 value from 0.1 kohm to 0.1 ohm and R6 value from 300 kohm to 300 ohm in Figure 21 ... 21
- Changed R5 value from 0.05 kohm to 0.05 ohm in Figure 22 ... 22

Changes from Original (July 2013) to Revision A **Page**

- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1

5 Pin Configuration and Functions

D Package
16-Pin SOIC
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	UVLO	I	Low input undervoltage lockout. Use a resister divider from VIN to this pin to set the UVLO threshold.
2	EN	I	Device enable and disable control input. EN pin high voltage enables the device. EN pin low voltage disables the device.
3	PWM	I	PWM dimming signal input. The frequency of the PWM signal is in the range of 90 Hz to 22 kHz.
4	AGND	G	Analog ground
5	REF	O	Internal reference voltage for the boost converter. Use a capacitor at this pin to adjust the soft-start time.
6	COMP	O	Loop compensation for the boost converter. Connect a RC network to make loop stable
7	IFB	I	Regulated current sink input pin. A resistor on this pin is used to set a desired string current.
8	IDRV	O	PWM dimming output control pin to drive the external MOSFET or bipolar transistor
9	ISNS	I	External switch MOSFET current sense positive input
10	OVP	I	Overvoltage protection detection input. Connect a resistor divider from output to this pin to program the OVP threshold. In addition, this pin is also the feedback of the output voltage of the boost converter.
11	PGND	G	External MOSFET current sense ground input
12	GDRV	O	Gate driver output for the external switch MOSFET
13	VDD	O	Internal regulator output for device power supply. Connect a ceramic capacitor of more than 1 µF to this pin.
14	FSW	O	Boost switching frequency setting pin. Use a resistor to set the frequency from 50 kHz to 800 kHz.
15	FAULT	O	Fault indicator. Open-drain output. Output high impedance when fault conditions happen.
16	VIN	I	Power supply input pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range(2)	Pin VIN	–0.3	33	V
	Pin FAULT	–0.3	VIN	
	Pin ISNS, IFB	–0.3	3.3	
	Pin EN, PWM, VDD, GDRV, IDRV	–0.3	20	
	Pin GDRV 10-ns transient	–2	20	
	All other pins	–0.3	7	
Continuous power dissipation		See *Thermal Information*		
Operating junction temperature range		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model	200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	8	30	V
V_{OUT}	Output voltage range	V_{IN}	300	V
L_1	Inductor	4.7	470	µH
C_{IN}	Input capacitor	10		µF
C_{OUT}	Output capacitor	1	220	µF
f_{SW}	Boost regulator switching frequency	50	800	kHz
f_{DIM}	PWM dimming frequency	0.09	22	kHz
T_A	Operating ambient temperature	–40	85	°C
T_J	Operating junction temperature	–40	125	°C

(1) Customers need to verify the component value in their application if the values are different from the recommended values.

6.4 Thermal Information

THERMAL METRIC(1)		TPS61197 D (SOIC) 16 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.8	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	44.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.3	°C/W
$R_{\psi JT}$	Junction-to-top characterization parameter	13.5	°C/W
$R_{\psi JB}$	Junction-to-board characterization parameter	42.9	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

V_{IN} = 24 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C, EC1 = 470 µF, EC2 = 22 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		8		30	V
V_{VIN_UVLO}	Undervoltage lockout threshold	V_{IN} falling		6.5	7	V
V_{VIN_HYS}	VIN UVLO hysteresis			300		mV
I_{Q_VIN}	Operating quiescent current into VIN	Device enabled, no switching, V_{IN} = 30 V			2	mA
I_{SD}	Shutdown current	V_{IN} = 12 V V_{IN} = 30 V			25 50	µA
V_{DD}	Regulation voltage for internal circuit	0 mA < I_{DD} < 15 mA	6.6	7	7.4	V
EN and PWM						
V_H	Logic high input on EN, PWM	V_{IN} = 8 V to 30 V	1.6			V
V_L	Logic low input on EN, PWM	V_{IN} = 8 V to 30 V			0.75	V
R_{PD}	Pulldown resistance on EN, PWM		400	800	1600	kΩ
UVLO						
V_{UVLOTH}	Threshold voltage at UVLO pin		1.204	1.229	1.253	V
I_{UVLO}	UVLO input bias current	V_{UVLO} = V_{UVLOTH} – 50 mV	–0.1		0.1	µA
		V_{UVLO} = V_{UVLOTH} + 50 mV	–4.4	-3.9	–3.3	
SOFT START						
I_{SS}	Soft start charging current	PWM dimming on, V_{REF}< 2 V		200		µA
CURRENT REGULATION						
V_{IFB_REG}	IFB pin regulation voltage	T_J = 25°C to 85°C	293	300	307	mV
V_{IFB_SCP}	IFB short to ground protection threshold			200		mV
V_{IFB_OVP}	IFB over voltage protection threshold		1	1.1	1.2	V
I_{IFB_LEAK}	IFB pin leakage current	V_{IFB} = 300 mV	–100		100	nA

Electrical Characteristics (continued)

V_{IN} = 24 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C, EC1 = 470 µF, EC2 = 22 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST REFERENCE VOLTAGE						
V_{REF}	Reference voltage range for boost controller		0		3.5	V
I_{REF_LEAK}	Leakage current at REF	T_J = –40°C to 85°C	–25		25	nA
OSCILLATOR						
V_{FSW}	FSW pin reference voltage			1.8		V
ERROR AMPLIFIER						
I_{SINK}	Comp pin sink current	V_{OVP} = V_{REF} + 200 mV, V_{COMP} = 1V		20		µA
I_{SOURCE}	Comp pin source current	V_{OVP} = V_{REF} – 200 mV, V_{COMP} = 1V		20		µA
Gm_{EA}	Error amplifier transconductance		90	120	150	µS
R_{EA}	Error amplifier output resistance			20		MΩ
GATE DRIVER						
R_{GDRV_SRC}	Gate driver impedance when sourcing	V_{GDRV} = 7 V, I_{GDRV} = –20 mA		5	10	Ω
R_{GDRV_SNK}	Gate driver impedance when sinking	V_{DD} = 7 V, I_{GDRV} = 20 mA		2	5	Ω
I_{GDRV_SRC}	Gate driver source current	V_{DD} = 7 V, V_{GDRV} = 5 V	200			mA
I_{GDRV_SNK}	Gate driver sink current	V_{DD} = 7 V, V_{GDRV} = 2 V	400			mA
V_{PWM_OCP}	Overcurrent detection threshold during PWM	V_{IN} = 8 V to 30 V, T_J = 25°C to 125°C	376	400	424	mV
V_{PFM_OCP}	Overcurrent detection threshold during PFM			180		mV
OVP						
V_{OVPTH}	Overvoltage protection threshold		2.98	3.04	3.1	V
I_{OVP_LEAK}	Leakage current at OVP pin		–100	0	100	nA
FAULT INDICATOR						
I_{FLT_H}	Leakage current at high impedance	V_{FLT} = 24 V		1		nA
I_{FLT_L}	Sink current at low output	V_{FLT} = 1 V	2	5		mA
THERMAL SHUTDOWN						
T_{STDN}	Thermal shutdown threshold			150		°C
T_{HYS}	Thermal shutdown threshold hysteresis			15		°C

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}	Switching frequency	R = 200 kΩ	187	200	213	kHz
$D_{(max)}$	Maximum duty cycle	f_{SW} = 200 kHz	90%	94%	98%	
$t_{on(min)}$	Minimum pulse width			300		ns
f_{EA}	Error amplifier crossover frequency			1000		kHz

6.7 Typical Characteristics

Table 1. Table Of Graphs

See Figure 18		
TITLE	**TEST CONDITIONS**	**FIGURE**
Dimming Linearity	24 LEDs (V_{OUT} = 80 V), V_{IN} = 24 V	Figure 1
Dimming Linearity at Small Dimming Duty Cycle	24 LEDs (V_{OUT} = 80 V), V_{IN} = 24 V	Figure 2
DC Load Efficiency	f_{SW} = 130 kHz	Figure 3
Switching Frequency Setting	V_{IN} = 24 V	Figure 4
Boost Switching Waveform	V_{IN} = 24 V, V_{OUT} = 80 V, I_{OUT} = 300 mA	Figure 5
Dimming Waveform (2% Dimming)	V_{IN} = 24 V, V_{OUT} = 80 V, I_{OUT} = 300 mA, 100-Hz dimming frequency	Figure 6
Startup Waveform (1% Dimming)	100-Hz dimming frequency, 1% dimming duty cycle	Figure 7
Startup Waveform (100% Dimming)	100-Hz dimming frequency, 100% dimming duty cycle	Figure 8
Shutdown Waveform (1% Dimming)	100-Hz dimming frequency, 1% dimming duty cycle	Figure 9
Shutdown Waveform (100% Dimming)	100-Hz dimming frequenc, 100% dimming duty cycle	Figure 10
LED Open Protection (1% Dimming)	100-Hz dimming frequenc, 1% dimming duty cycle	Figure 11
LED Open Protection (100% Dimming)	100-Hz dimming frequenc, 100% Dimming Duty Cycle	Figure 12
LED String Short Protection (1% Dimming)	100-Hz dimming frequency, 1% dimming duty cycle	Figure 13
LED String Short Protection (100% Dimming)	100-Hz dimming frequency, 1% dimming duty cycle	Figure 14

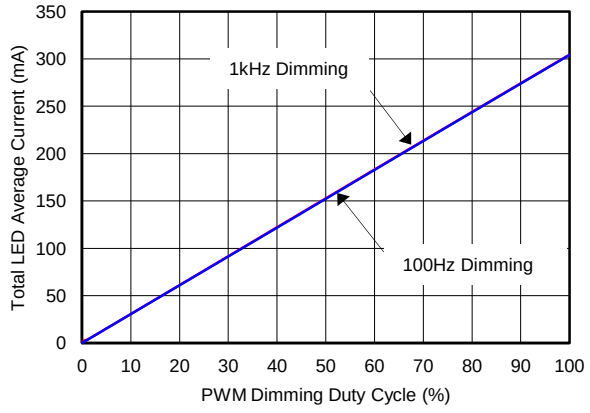


Figure 1. Dimming Linearity

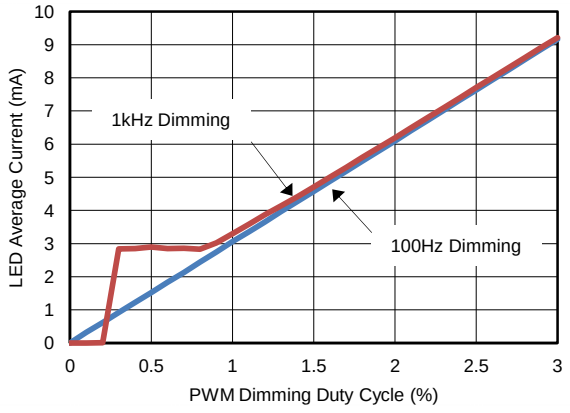


Figure 2. Dimming Linearity at Low Dimming Duty Cycle

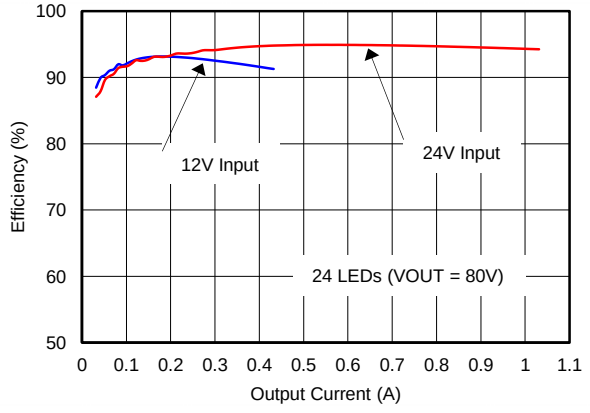


Figure 3. DC Load Efficiency

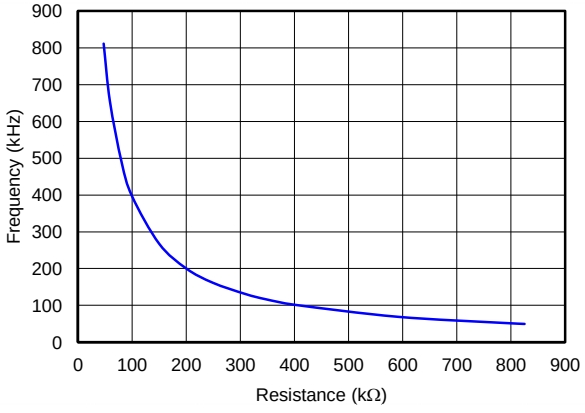


Figure 4. Switching Frequency Setting

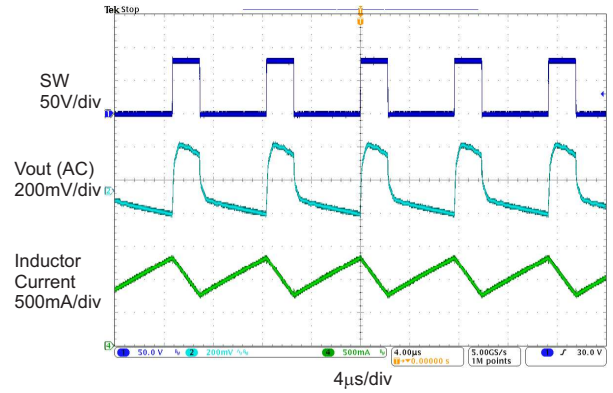


Figure 5. Boost Switching Waveform

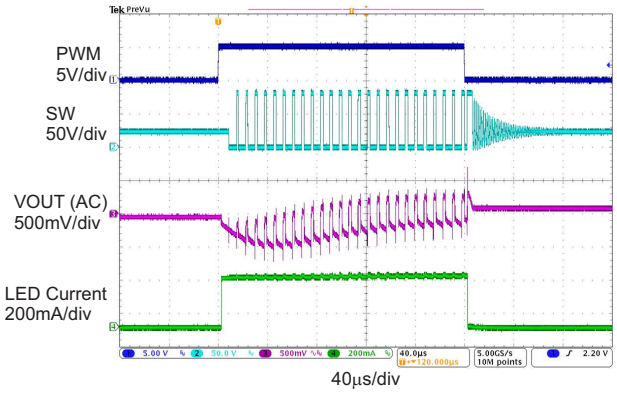


Figure 6. Dimming Waveform (1% Dimming)

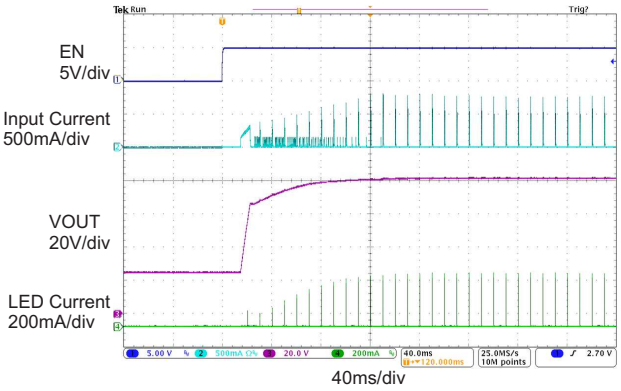


Figure 7. Start-up Waveform (1% Dimming)

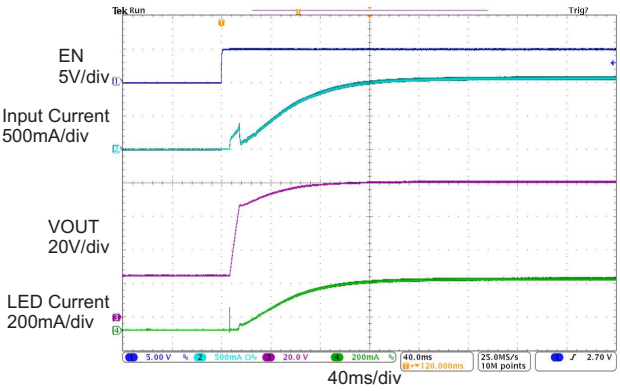


Figure 8. Start-up Waveform (100% Dimming)

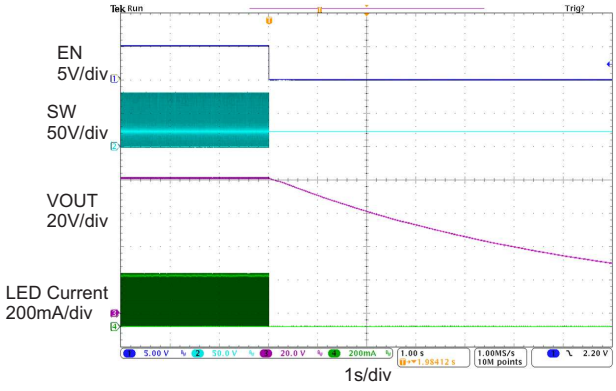


Figure 9. Shutdown Waveform (1% Dimming)

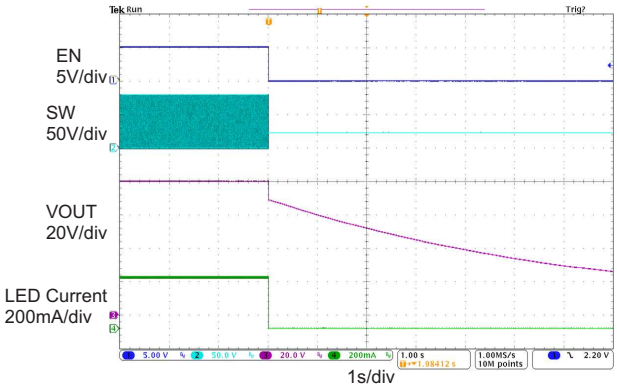


Figure 10. Shutdown Waveform (100% Dimming)

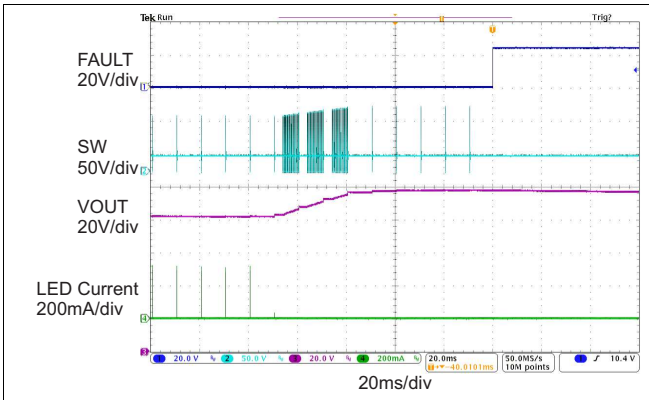


Figure 11. LED Open Protection (1% Dimming)

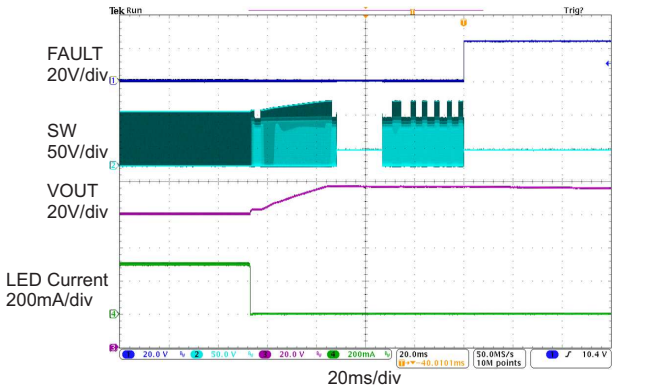


Figure 12. LED Open Protection (100% Dimming)

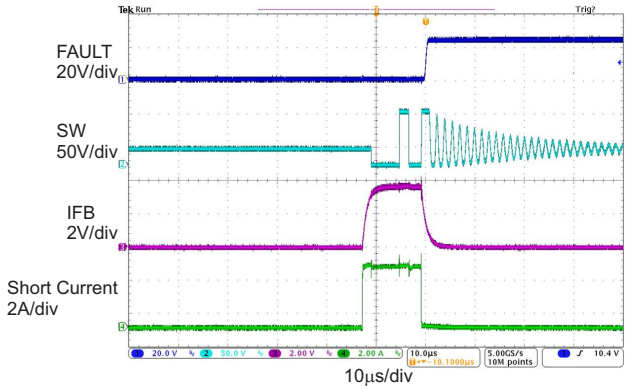


Figure 13. LED String Short Protection (1% Dimming)

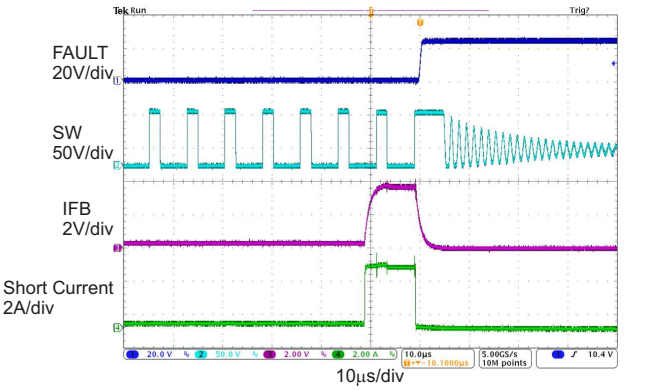


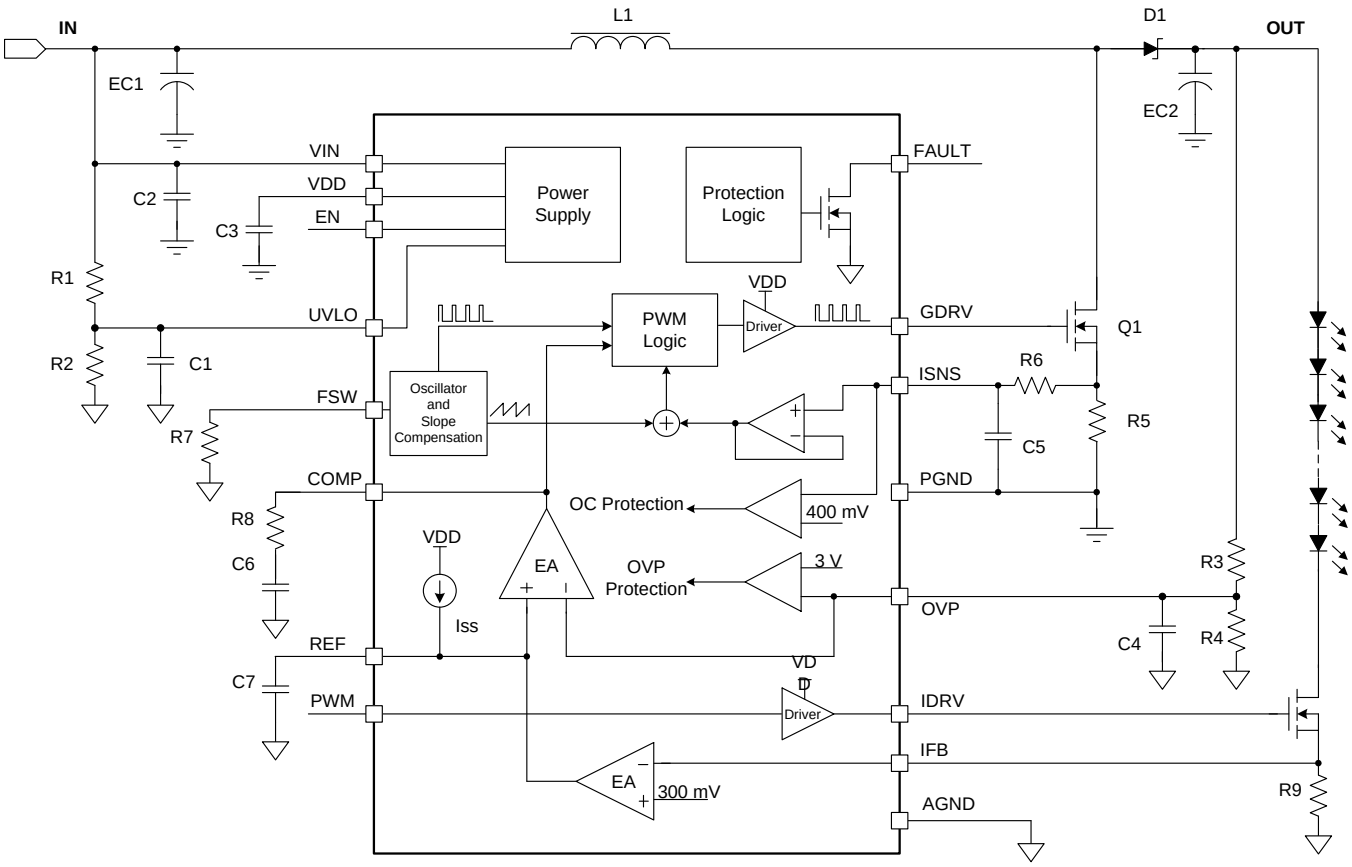
Figure 14. LED String Short Protection (100% Dimming)

7 Detailed Description

7.1 Overview

The TPS61197 provides a highly integrated solution for LCD TV backlight with high precision pulse width modulation (PWM) dimming resolution up to 5000:1. This device is a current-mode boost controller driving one WLED string with multiple LEDs in series. The input voltage range for the device is from 8 V to 30 V.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Supply Voltage

The TPS61197 has a built-in linear regulator to supply the device analog and logic circuits. The VDD pin (output of the regulator) must be connected to a bypass capacitor with more than 1-µF capacitance. VDD only has a current sourcing capability of 15 mA. VDD voltage is ready after the EN pin is pulled high.

7.3.2 Boost Controller

The TPS61197 regulates the output voltage with peak current mode PWM control. The control circuitry turns on an external switch FET at the beginning of each switching cycle. The input voltage is applied across the inductor and stores the energy as the inductor current ramps up. During this portion of the switching cycle, the load current is provided by the output capacitor. When the inductor current rises to the threshold set by the error amplifier (EA) output, the switch FET is turned off and the external Schottky diode is forward biased. The inductor transfers stored energy to replenish the output capacitor and supply the load current. This operation repeats each switching cycle. The switching frequency is programmed by an external resistor.

Feature Description (continued)

A ramp signal from the oscillator is added to the current ramp to provide slope compensation, shown in the *Functional Block Diagram*. The duty cycle of the converter is then determined by the PWM logic block which compares the EA output and the slope compensated current ramp. The feedback loop regulates the OVP pin to a reference voltage generated by the current regulation control circuit which senses the LED current at the IFB pin. The output of the EA is connected to the COMP pin. An external RC compensation network must be connected to the COMP pin to optimize the feedback loop for stability and transient response.

The TPS61197 consistently adjusts the boost output voltage to account for any changes in LED forward voltages. In the event that the boost controller is not able to regulate the output voltage due to the minimum pulse width ($t_{on(min)}$, in the *Electrical Characteristics* table), the TPS61197 enters pulse skip mode. In this mode, the device keeps the power switch off for several switching cycles to prevent the output voltage from rising above the regulated voltage. This operation typically occurs in light load condition or when the input voltage is higher than the output voltage.

7.3.3 Switching Frequency

The switching frequency is programmed from 50 kHz to 800 kHz by an external resistor (R7 in Figure 18). To determine the resistance by a given frequency, use the curve in Figure 4 or calculate the resistance value by Equation 1. Table 2 shows the recommended resistance values for some switching frequencies.

$$f_{SW} = \frac{40000}{R7\ (k\Omega)}(kHz) \quad (1)$$

Table 2. Recommended Resistance Values For Switching Frequencies

R7 (kΩ)	f_{SW} (kHz)
800	50
400	100
200	200
100	400
80	500

7.3.4 Enable and Undervoltage Lockout

The TPS61197 is enabled with soft start-up when the EN pin voltage is higher than 1.6 V. A voltage of less than 0.75 V disables the TPS61197. An undervoltage lockout (UVLO) protection feature is provided in the TPS61197. When the voltage at the VIN pin is less than 6.5 V, the TPS61197 is powered off. The TPS61197 resumes the operation once the voltage at the VIN pin recovers above the hysteresis (V_{VIN_HYS}) more than the UVLO falling threshold of input voltage. If a higher UVLO voltage is required, use the UVLO pin as shown in Figure 15 to adjust the input UVLO threshold by using an external resistor divider. Once the voltage at the UVLO pin exceeds the 1.229-V threshold, the TPS61197 is powered on and a hysteresis current source of 3.9 µA is added. When the voltage at the UVLO pin drops lower than 1.229 V, the current source is removed and the TPS61197 is powered off. The resistors of R1, R2 can be calculated by Equation 2 from required turnon voltage (V_{START}) and turn-off voltage (V_{STOP}). To avoid noise coupling, the resistor divider R1 and R2 must be close to the UVLO pin. Placing a filter capacitor of more than 10nF as shown in Figure 15 can eliminate the impact of the switching ripple of the input voltage and improve the noise immunity.

If the UVLO function is not used, pull up the UVLO pin to the VDD pin.

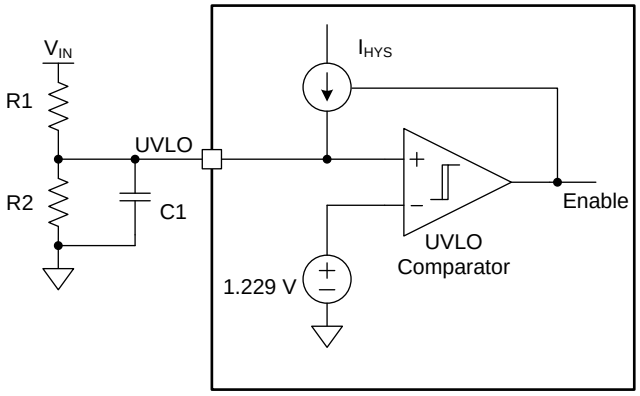


Figure 15. UVLO Circuit

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS}}$$

where

- I_{HYS} is 3.9 µA sourcing current from the UVLO pin (2)

$$R2 = R1 \frac{1.229V}{V_{START} - 1.229V} \quad (3)$$

When the UVLO condition happens, the FAULT pin outputs high impedance. As long as the UVLO condition is removed, the FAULT pin outputs low impedance.

7.3.5 Power-Up Sequencing and Soft Start-up

The input voltage, UVLO pin voltage, EN input signal, and the input dimming PWM signal control the power up of the TPS61197. After the input voltage is above the required minimal input voltage of 7.5 V, the internal circuit is ready to be powered up. After the UVLO pin voltage is above the threshold of 1.229 V and the EN signal is high, the internal LDO and logic circuit are activated. When the PWM dimming signal is high, the soft start-up begins.

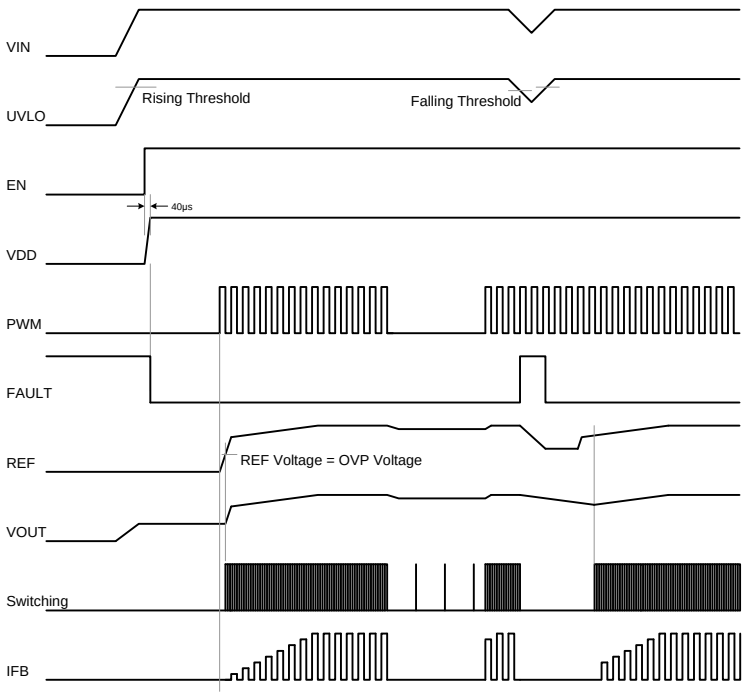


Figure 16. Power-Up Sequencing

The TPS61197 has integrated the soft-start circuitry working with an external capacitor at the REF pin to avoid inrush current during start-up. During the start-up period, the capacitor at the REF pin is charged with a soft-start current source. When the REF pin voltage is higher than the output feedback voltage at the OVP pin, the boost controller starts switching, and the output voltage starts to ramp up. At the same time, the LED current regulation circuit starts to drive the LED string. At the beginning of the soft start, the charge current is 200 µA. Once the voltage of the REF pin exceeds 2 V, the charge current stops. The output voltage continues to ramp up until the IFB voltage is in regulation of 300 mV. The total soft-start time is determined by the external capacitance at the REF pin. The capacitance must be within 470 nF to 4.7 µF for different start-up time.

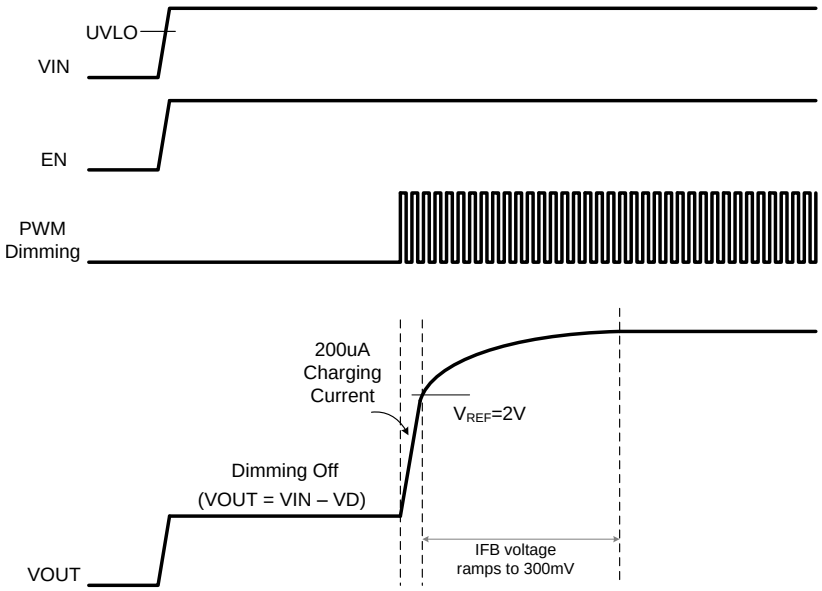


Figure 17. Soft-Start Waveforms

7.3.6 Current Regulation

The TPS61197 regulates the IFB voltage to 300 mV. Applying a current sense resistor (R9 in the *Figure 18*) at the IFB pin to set the required LED current.

$$I_{LED} = \frac{V_{IFB\_REG}}{R9} \quad (4)$$

where

- V_{IFB_REG} is the IFB pin regulation voltage of 300 mV

7.3.7 PWM Dimming

LED brightness dimming is set by applying an external PWM signal of 90 Hz to 22 kHz to the PWM pin. Varying the PWM duty cycle from 0% to 100% adjusts the LED from minimum to maximum brightness, respectively. The recommended minimum on-time of the LED string is 10 µs. Thus, the TPS61197 has a minimum dimming ratio of 5000:1 at 200 Hz.

When the PWM voltage is pulled low during dimming off, the TPS61197 turns off the LED string and keeps the boost converter running in pulse frequency modulation (PFM) mode. In PFM mode, the output voltage is kept at a level which is a little bit lower than that when the PWM voltage is high. Thus, the TPS61197 limits the output ripple due to the load transient that occurs during PWM dimming.

When the PWM voltages are pulled low for more than 20 ms, to avoid the REF pin voltage dropping due to the leakage current, the voltage of the REF pin is held by an internal reference voltage, which is a little bit lower than the REF pin voltage in normal dimming operation. Thus, the output voltage is kept unchanged during the long dimming off time.

Because the output voltage in long-time dimming off status is almost the same as the normal voltage for turning the LED on, the TPS61197 turns on the LED very fast without any flicker when recovering from long-time dimming off to normal dimming operation.

7.3.8 Indication for Fault Conditions

The TPS61197 has an open-drain fault indicator pin to indicate abnormal conditions. When the TPS61197 is operating normally, the voltage at the FAULT pin is low. When any fault condition happens, the FAULT pin is in high impedance, which can be pulled up to a high voltage level through an external resistor.

7.4 Device Functional Modes

7.4.1 Protections

The TPS61197 has full set of protections making the system safe to any abnormal conditions. Some protections latch the TPS61197 in off state until its power supply is recycled or it is disabled and then enabled again. In the latch-off state, the REF pin voltage is discharged to 0 V.

7.4.1.1 Switch Current Limit Protection Using the ISNS Pin

The TPS61197 monitors the inductor current through the voltage across a sense resistor (R5 in Figure 18) in order to provide current-limit protection. During the switch FET on period, when the voltage at the ISNS pin rises above the overcurrent protection threshold (V_{PWM_OCP} or V_{PFM_OCP} in *Electrical Characteristics*), the device turns off the FET immediately and does not turn it back on until the next switching cycle. The switch current limit is equal to V_{PWM_OCP} / R5 (or V_{PFM_OCP} / R5). The current limit is different for PWM mode and PFM mode. In the PWM mode, the current limit threshold voltage is 400 mV typically. In the PFM mode, it is 180 mV typically.

7.4.1.2 LED Open Protection

When the LED string is open, the IFB pin voltage drops to zero volt during dimming on-time. The TPS61197 keeps increasing the output voltage until it touches the output over-voltage protection threshold. The TPS61197 is then latched off.

Device Functional Modes (continued)

7.4.1.3 Schottky Diode Open Protection

When the TPS61197 is enabled, it checks the topology connection first. The TPS61197 detects the voltage at the OVP pin to check if the Schottky diode is not connected or the boost output is hard-shorted to ground. If the voltage at the OVP pin is lower than 70 mV for 80 ms, the TPS61197 is locked in off state until the input power is recycled or the TPS61197 is enabled again.

7.4.1.4 Schottky Diode Short Protection

If the rectifier Schottky diode is shorted, the reverse current from output capacitor to ground is very large when the switch MOSFET is turned on. The TPS61197 uses a secondary current limit threshold of 800 mV across the current sense resistor to permanently disable the switching if the threshold is touched.

7.4.1.5 IFB Overvoltage Protection

When the IFB pin reaches the threshold (V_{IFB_OVP} in the *Electrical Characteristics* table) of 1.1V during startup or normal operation, the device stops switching and stays in the latch-off state immediately to protect from damage. This function protects the external dimming MOSFET from damage when the LED string is shorted from the anode (connecting to output of the boost converter) to its cathode.

7.4.1.6 Output Overvoltage Protection Using the OVP Pin

Use a resistor divider to program the maximum output voltage of the boost converter. To ensure the LED string can be turned on with setting current, the maximum output voltage must be higher than the forward voltage drop of the LED string. The maximum required voltage can be calculated by multiplying the maximum LED forward voltage ($V_{FWD(max)}$) and number (n) of series LEDs , and adding extra 2 V to account for regulation and resistor tolerances and load transients.

The recommended bottom feedback resistor of the resistor divider (R4 in Figure 18) is 20 kΩ. Calculate the top feedback resistor (R3 in the *Figure 18*) using Equation 5, where V_{OUT_OVP} is the output overvoltage protection threshold of the boost converter.

$$R3 = \left(\frac{V_{OUT\_OVP}}{3.04} - 1 \right) \times R4 \tag{5}$$

When the device detects that the OVP pin voltage exceeds the overvoltage protection threshold of 3.04 V, indicating that the output voltage has exceeded the over-voltage proteciton threshold, the TPS61197 clamps the output voltage to prevent it going up any more. If the OVP pin voltage does not drop below the OVP threshold for more than 640 ms, the TPS61197 is latched off until the input power or the EN pin is re-cycled.

7.4.1.7 IFB Short-to-Ground Protection

The TPS61197 monitors the IFB pin voltage when the device is enabled. If the IFB pin voltage is less than 200 mV, the TPS61197 keeps increasing the output voltage until the over-voltage protection or the switch overcurrent protection happens. If the IFB pin voltage is still under 200 mV for 60 ms in these protection conditions, the TPS61197 is latched off.

Device Functional Modes (continued)

7.4.1.8 Thermal Shutdown

When the internal junction temperature of the TPS61197 is over 150°C, the thermal protection circuit is triggered and shuts down the device immediately. The device automatically restarts when the junction temperature falls back to less than 150°C, with approximate 15°C hysteresis.

Table 3. Protection List

PROTECTION ITEM	FAULT CONDITIONS	FAULT	RESULT
Diode open	V_{OVP} < 70 mV for more than 80 ms	Y	Latch off
Diode short	V_{ISNS} > 800 mV for three switching cycles	Y	Latch off
Output overvoltage	V_{OVP} > 3.04 V for more than 640 ms	Y	Latch off
LED string open	(V_{IFB} < 200 mV and V_{OVP} > 3.04 V) for more than 60 ms	Y	Latch off
LED string short	V_{IFB} > 1.1 V	Y	Latch off
IFB short to ground	(V_{IFB} < 200 mV and V_{OVP} > 3.04 V) or (V_{IFB} < 200 mV and V_{ISNS} > 400 mV) for more than 60 ms	Y	Latch off
Input voltage under UVLO threshold	V_{UVLO} < 1.229 V	Y	Retry
Thermal shutdown	T_J > 150°C	Y	Retry

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61197 is designed for LCD TV backlighting. It is a current-mode boost controller driving one white-LED string with multiple LEDs in series. The input voltage range for the device is from 8 V to 30 V. Its switching frequency is programmed by an external resistor from 50 kHz to 800 kHz.

The TPS61197 has a built-in linear regulator, which steps down the input voltage to the VDD voltage for powering the internal circuitry. An internal soft start circuit is implemented to work with an external capacitor to adjust the soft start-up time to minimize the in-rush current during boost converter start-up.

8.2 Typical Applications

8.2.1 Simple Boost Converter

The TPS61197 is configured as a simple boost converter to drive the single string with the LEDs when the boost ratio of the output voltage to the input voltage is less than 6.

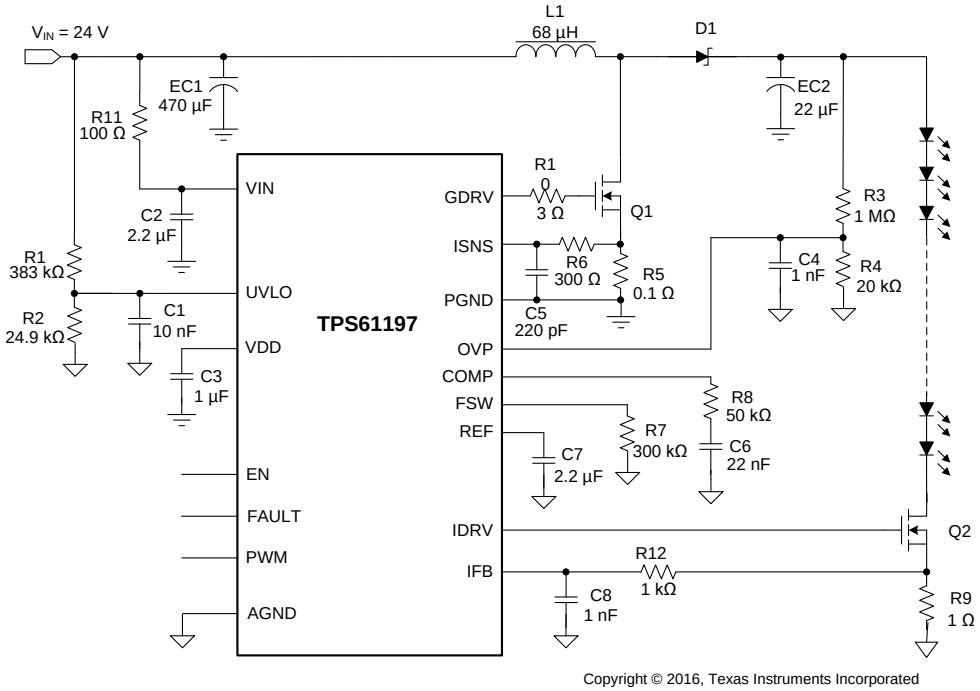


Figure 18. TPS61197 Simple Boost-Converter Application

Typical Applications (continued)

8.2.1.1 Design Requirements

For LED-driver applications, use the parameters listed in Table 4.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	8 V to 30 V
Output voltage	V_{IN} to 300 V
Output current	300 mA (maximum)
Programmable switching frequency	50 kHz to 800 kHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

The inductor is the most important component in switching power regulator design because it affects power supply steady state operation, transient behavior, and loop stability. The inductor value, DC resistance and saturation current are important specifications to be considered for better performance. Although the boost power stage can be designed to operate in discontinuous conduction mode (DCM) at maximum load, where the inductor current ramps down to zero during each switching cycle, most applications are more efficient if the power stage operates in continuous conduction mode (CCM), where a DC current flows through the inductor. Therefore, the Equation 7 and Equation 8 are for CCM operation only. The TPS61197 device is designed to work with inductor values from 4.7 µH and 470 µH, depending on the switching frequency. Running the controller at higher switching frequencies allows the use of smaller and/or lower profile inductors in the 4.7-µH range. Running the controller at slower switching frequencies requires the use of larger inductors, near 470 µH, to maintain the same inductor current ripple but may improve overall efficiency due to smaller switching losses. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value measured at near 0 A, depending on how the inductor vendor defines saturation.

In a boost regulator, the inductor DC current can be calculated with Equation 6.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (6)$$

where

- V_{OUT} = boost output voltage
- I_{OUT} = boost output current
- V_{IN} = boost input voltage
- η = power conversion efficiency, use 95% for TPS61197 applications

The inductor peak-to-peak ripple current can be calculated with Equation 7.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{L \times f_{SW} \times V_{OUT}} \quad (7)$$

where

- $\Delta I_{L(P-P)}$ = inductor ripple current
- L = inductor value
- f_{SW} = switching frequency
- V_{OUT} = boost output voltage
- V_{IN} = boost input voltage

Therefore, the inductor peak current is calculated with Equation 8.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (8)$$

Select an inductor, which saturation current is higher than calculated peak current. To calculate the worst case inductor peak current, use the minimum input voltage, maximum output voltage and maximum load current.

Regulator efficiency is dependent on the resistance of its high current path and switching losses associated with the switch FET and power diode. Besides the external switch FET, the overall efficiency is also affected by the inductor DC resistance (DCR). Usually the lower DC resistance shows higher efficiency. However, there is a tradeoff between DCR and inductor footprint; furthermore, shielded inductors typically have higher DCR than unshielded ones.

8.2.1.2.2 Output Capacitor

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability of the whole system. This ripple voltage is related to the capacitance of the capacitor and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$V_{RIPPLE(C)} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times C_{OUT}}$$

where

- V_{RIPPLE} is the peak-to-peak output voltage ripple
- D_{MAX} is the maximum duty cycle of the boost converter in the application (9)

D_{MAX} is approximately equal to ($V_{OUT(MAX)}$ – $V_{IN(MIN)}$) / $V_{OUT(MAX)}$) in applications. Care must be taken when evaluating a capacitor's derating under DC voltage. The DC bias voltage can also significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, leave the margin on the voltage rating to ensure adequate capacitance.

The ESR impact on the output ripple must be considered as well if tantalum or aluminum electrolytic capacitors are used. Assuming there is enough capacitance such that the ripple due to the capacitance can be ignored, the ESR needed to limit the V_{RIPPLE} is:

$$V_{RIPPLE(ESR)} = I_{L(P)} \times ESR \quad (10)$$

Ripple current flowing through a capacitor's ESR causes power dissipation in the capacitor. This power dissipation causes temperature increase internally to the capacitor. Excessive temperature can seriously shorten the expected life of a capacitor. Capacitors have ripple current ratings that are dependent on ambient temperature and must not be exceeded. Therefore, high ripple current type electrolytic capacitor with small ESR is used in the typical application as shown in Figure 18.

In the typical application, the output requires a capacitor in the range of 1 µF to 100 µF. The output capacitor affects the small signal control loop stability of the boost converter. If the output capacitor is below the range, the boost regulator may potentially become unstable.

8.2.1.2.3 Schottky Diode

The TPS61197 demands a high-speed rectification for optimum efficiency. Ensure that the average and peak current rating of the diode exceed the output LED current and inductor peak current. In addition, the reverse breakdown voltage of the diode must exceed the application output voltage.

8.2.1.2.4 Switch MOSFET and Gate Driver Resistor

The TPS61197 demands a power N-MOSFET (see Q1 in Figure 18) as a switch. The voltage and current rating of the MOSFET must be higher than the application output voltage and the inductor peak current. The applications benefit from the addition of a resistor (see R10 in Figure 18) connected between the GDRV pin and the gate of the switch MOSFET. With this resistor, the gate driving current is limited and the EMI performance is improved. TI recommends 3-Ω resistor value. The TPS61197 exhibits lower efficiency when the resistor value is above 3 Ω due to the more switching loss of the external MOSFET.

8.2.1.2.5 Current Sense and Current Sense Filtering

R5 determines the correct overcurrent limit protection. To choose the right value of R5, start with the total system power needed P_{OUT}, and calculate the input current I_{IN} by Equation 6. Efficiency can be estimated from Figure 20. The second step is to calculate the inductor peak current based on the inductor value L using Equation 7 and Equation 8. The maximum R5 can now be calculated as R5(maximum) = V_{ISNS_OC} / $I_{L(P)}$. TI recommends adding 20% or more margins to account for component variations. A small filter placed on the ISNS pin improves performance of the converter (see R6 and C5 in Figure 18). The time constant of this filter must be approximately 100 ns. The range of R6 must be from about 300 Ω to 1 kΩ for best results. Locate C5 as close as possible to the ISNS pin to provide noise immunity.

8.2.1.2.6 Loop Consideration

The COMP pin on the TPS61197 is used for external compensation, allowing the loop response to be optimized for each application. The COMP pin is the output of the internal trans-conductance amplifier. The external resistor R8, along with ceramic capacitors C6 (see Figure 18), are connected to the COMP pin to provide poles and zero. The pole and zero, along with the inherent pole and zero in a peak current mode control boost converter, determine the closed loop frequency response. This is important to converter stability and transient response.

The first step is to calculate the pole and the right half plane zero of the peak current mode boost converter by Equation 11 and Equation 12.

$$f_P = \frac{2I_{OUT}}{2\pi V_{OUT} \times C_{OUT}} \tag{11}$$

$$f_{ZRHP} = \frac{V_{OUT} \times (1-D)^2}{2\pi L \times I_{OUT}} \tag{12}$$

To make the loop stable, the loop must have sufficient phase margin at the crossover frequency where the loop gain is 1. To avoid the effect of the right half plane zero on the loop stability, choose the crossover frequency f_{CO} less than 1/5 of the f_{ZRHP}. Then calculate the compensation components by Equation 13 and Equation 14.

$$R8 = \frac{R5 \times 2\pi f_{CO} \times C_{OUT}}{(1-D) \times Gm_{EA}} \times \frac{V_{OUT\_OVP}}{V_{OVPTH}}$$

where

- V_{OVPTH} = 3.04 V, which is the overvoltage protection threshold at the OVP pin
- V_{OUT_OVP} is the setting output over-voltage protection threshold
- Gm_{EA} is the trans-conductance of the error amplifier (the typical value of the Gm_{EA} is 120 µs)
- f_{CO} is the crossover frequency, which normally is less than 1/5 of the f_{ZRHP} (13)

$$C6 = \frac{1}{2\pi f_P \times R8}$$

where

- f_P is the pole's frequency of the power stage calculated by Equation 11 (14)

If the output capacitor is the electrolytic capacitor which may have large ESR, a capacitor is required at the COMP pin or at the OVP pin to cancel the inherent zero of the output capacitor.

8.2.1.3 Application Curves

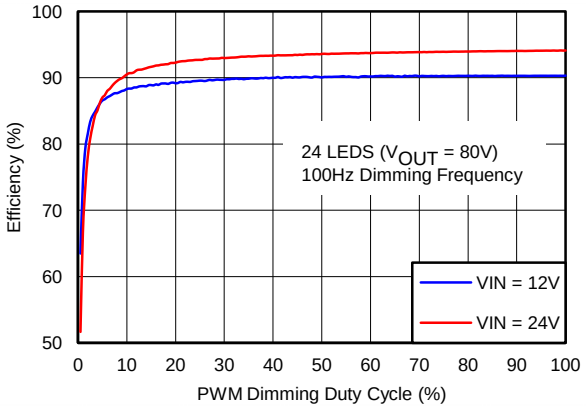


Figure 19. Efficiency (24 LEDs)

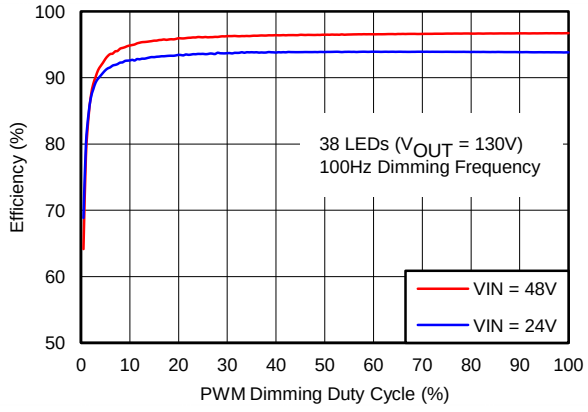


Figure 20. Efficiency (38 LED)

8.2.2 PWM Dimming Controlled by Boost Converter

The TPS61197 also supports the PWM dimming by turning on and off the boost converter to save cost of the dimming MOSFET. Figure 21 is the application circuit. This application requires small output capacitance so as to discharge the output voltage fast during dimming off period. The minimum dimming on time must be longer than 200 µs to ramp up the output voltage to achieve the setting LED current during dimming on period.

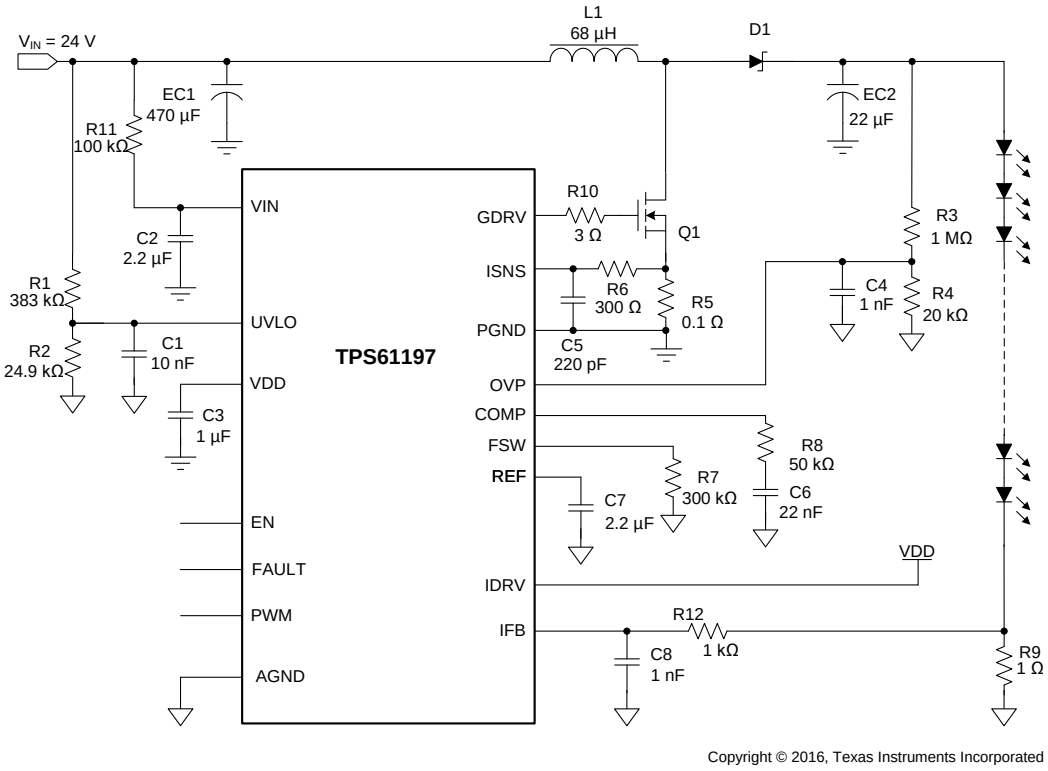


Figure 21. PWM Dimming By Turning On and Off the Boost Converter

8.2.3 High Boost Ratio Application

When the boost ratio is higher than 6, a transformer is required to replace the inductor to make the switching duty cycle near 50% and lower the voltage rating of the switch FET. Figure 22 is the application circuit.

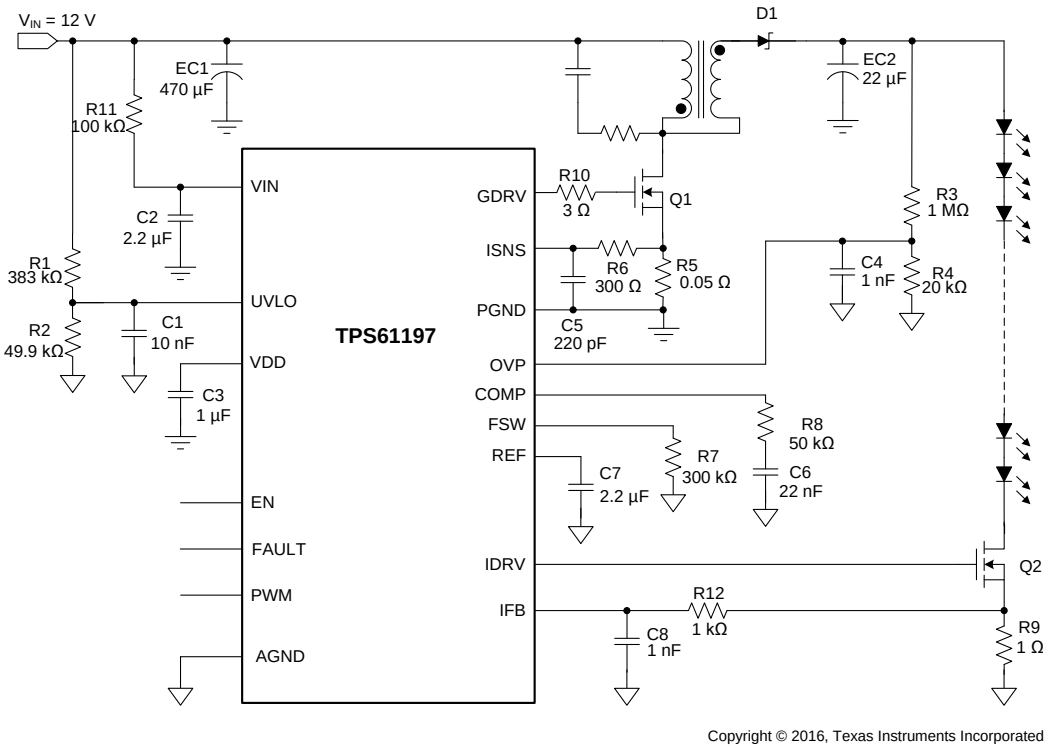


Figure 22. TPS61197 High Boost Ratio Application

9 Power Supply Recommendations

The TPS61197 requires a single-supply input voltage. This voltage can range from 8 V to 30 V and be able to supply enough current for a given application.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The VDD capacitor, C3 (see Figure 18) is the filter and noise decoupling capacitor for the internal linear regulator powering the internal circuitries. It must be placed as close as possible between the VDD and PGND pin to prevent any noise insertion to internal circuitry. The switch node at the drain of Q1 carries high current with fast rising and falling edges. Therefore, the connection between this node to the inductor and the Schottky diode must be kept as short and wide as possible. The ground of output capacitor EC2 must be kept close to input power ground or through a large ground plane because of the large ripple current returning to the input ground. When laying out signal grounds, TI recommends using short traces separate from power ground traces and connecting them together at a single point. Resistors R3, R4, and R7 (see Figure 18) are setting resistors for switching frequency and output overvoltage protection. To avoid unexpected noise coupling into the pins and affecting the accuracy, these resistors must be close to the pins with short and wide traces to AGND pin.

10.2 Layout Example

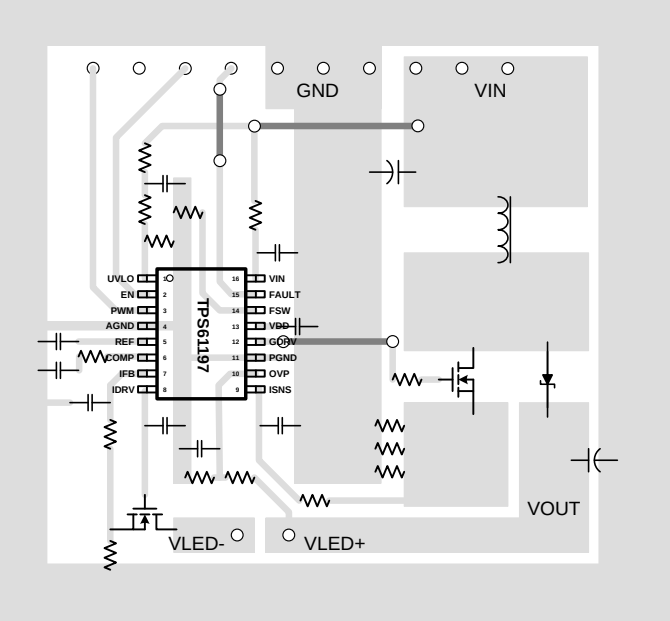


Figure 23. TPS61197 Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61197DR	NRND	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	TPS61197	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

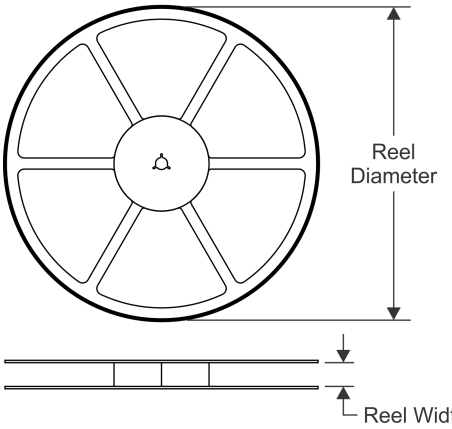
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

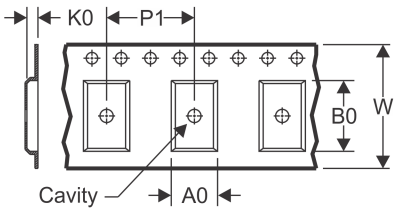
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

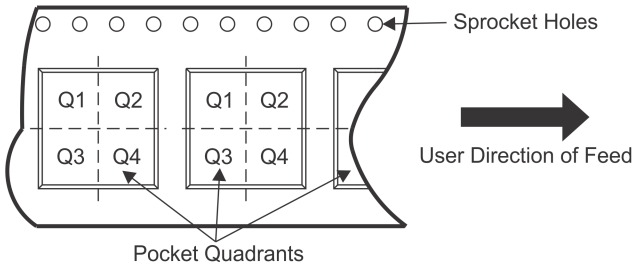


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

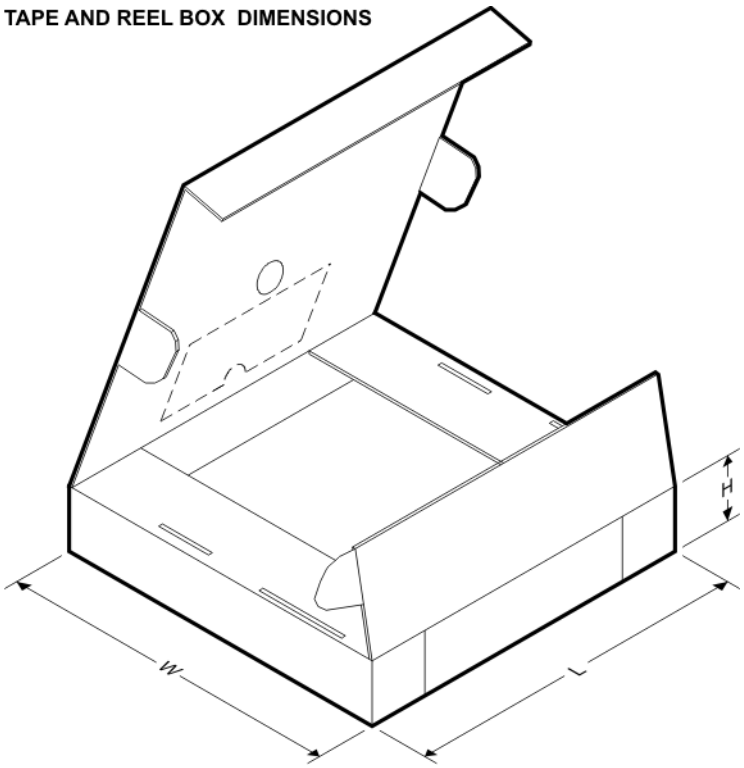
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61197DR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1

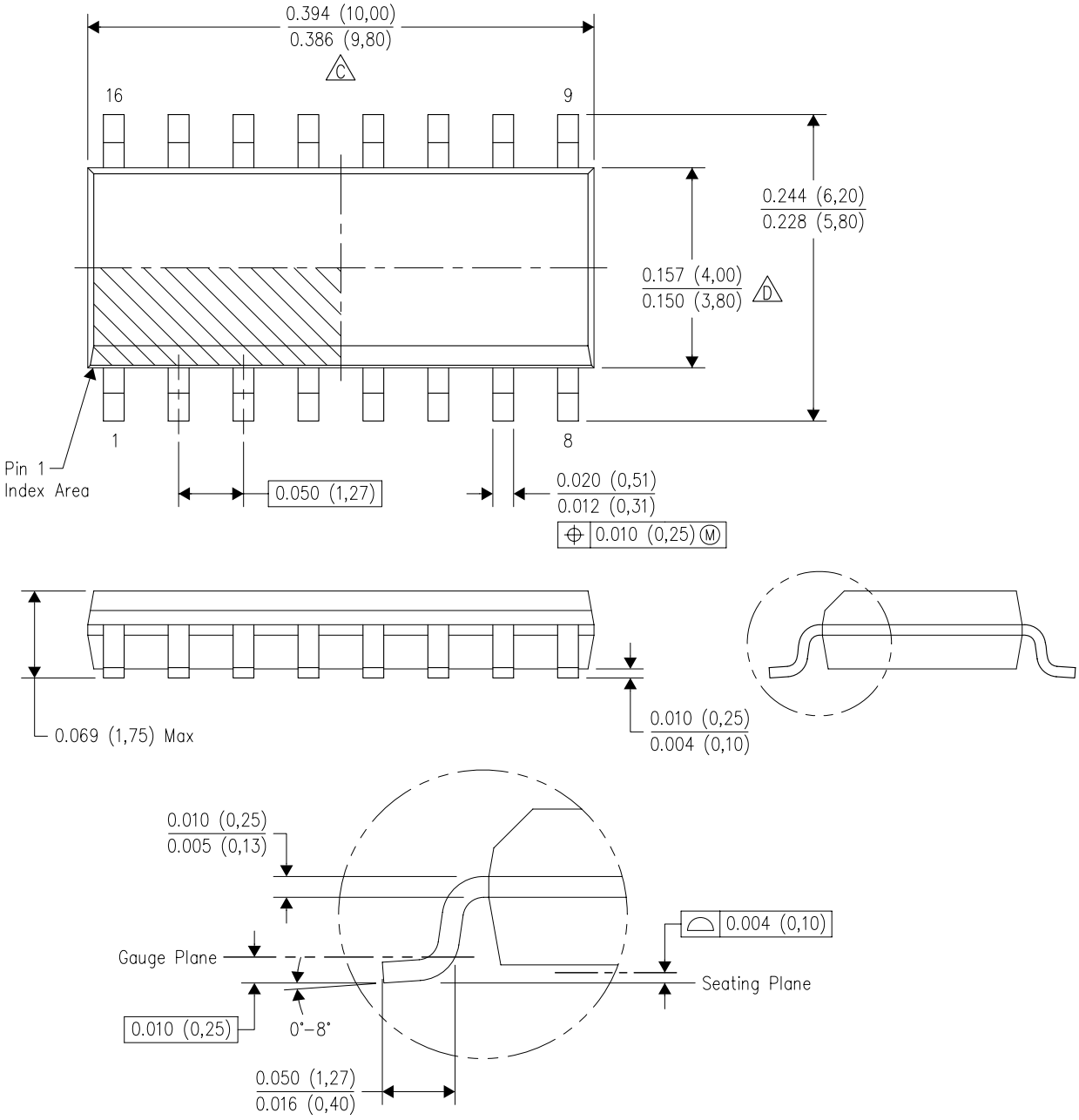
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

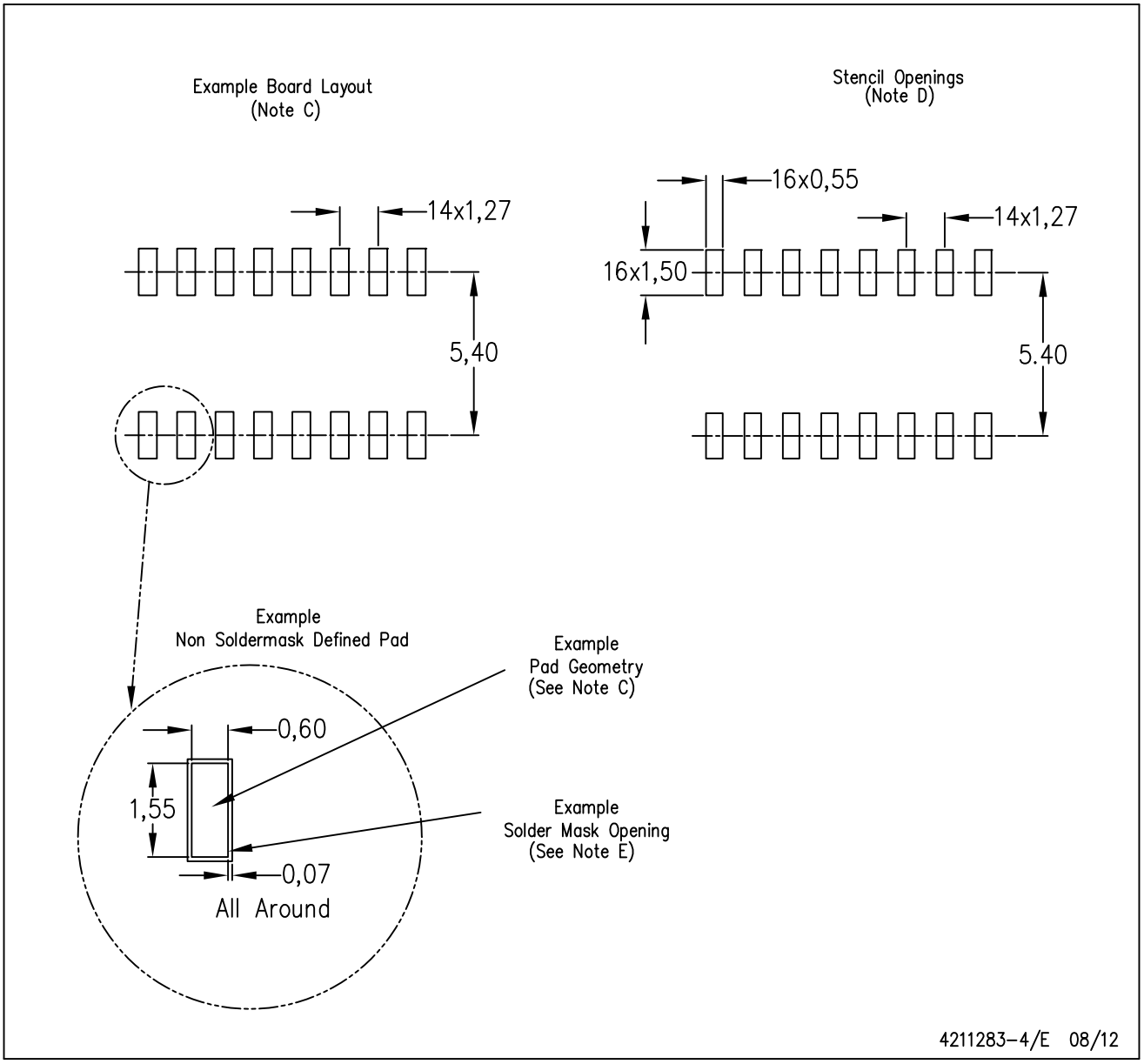
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61197DR	SOIC	D	16	2500	364.0	364.0	27.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265