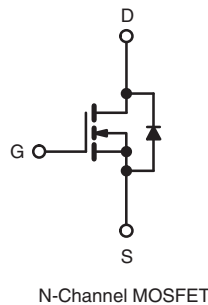
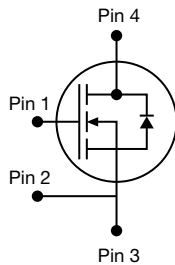
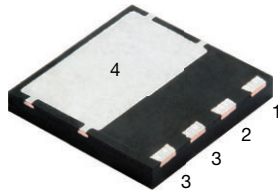


E Series Power MOSFET

| PRODUCT SUMMARY | | |
|---|-----------------|-------|
| V_{DS} (V) at T_J max. | 650 | |
| $R_{DS(on)}$ typ. (Ω) at 25 °C | $V_{GS} = 10$ V | 0.220 |
| Q_g max. (nC) | 82 | |
| Q_{gs} (nC) | 8 | |
| Q_{gd} (nC) | 16 | |
| Configuration | Single | |

PowerPAK® 8 x 8


FEATURES

- Fully lead (Pb)-free device
- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Kelvin connection for reduced gate noise
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)


| ORDERING INFORMATION | |
|---------------------------------|-------------------|
| Package | PowerPAK 8 x 8 |
| Lead (Pb)-free and Halogen-free | SiHH14N60E-T1-GE3 |

| ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted) | | | | |
|---|------------------|----------------|------|----|
| PARAMETER | SYMBOL | LIMIT | UNIT | |
| Drain-Source Voltage | V_{DS} | 600 | V | |
| Gate-Source Voltage | V_{GS} | ± 30 | | |
| Continuous Drain Current ($T_J = 150$ °C) | V_{GS} at 10 V | $T_C = 25$ °C | 16 | A |
| | | $T_C = 100$ °C | 10 | |
| Pulsed Drain Current ^a | | | 38 | |
| Linear Derating Factor | | 1.2 | W/°C | |
| Single Pulse Avalanche Energy ^b | E_{AS} | 173 | mJ | |
| Maximum Power Dissipation | P_D | 147 | W | |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +150 | °C | |
| Drain-Source Voltage Slope | dV/dt | 70 | V/ns | |
| Reverse Diode dV/dt ^c | | | | 19 |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 140$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 3.5$ A.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

| THERMAL RESISTANCE RATINGS | | | | |
|----------------------------------|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient | R_{thJA} | 42 | 55 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | 0.64 | 0.85 | |

| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|---------------------|---|---|---------------------------------------|-------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 600 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$ | | - | 0.65 | - | V/°C |
| Gate-Source Threshold Voltage (N) | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | | - | - | ± 100 | nA |
| | | $V_{GS} = \pm 30\text{ V}$ | | - | - | ± 1 | μA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$ | | - | - | 1 | μA |
| | | $V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | | - | - | 50 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 7\text{ A}$ | - | 0.220 | 0.255 | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = 30\text{ V}, I_D = 7\text{ A}$ | | - | 5.8 | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V},$ $V_{DS} = 100\text{ V},$ $f = 1\text{ MHz}$ | | - | 1416 | - | pF |
| Output Capacitance | C_{oss} | | | - | 74 | - | |
| Reverse Transfer Capacitance | C_{rss} | | | - | 6 | - | |
| Effective Output Capacitance, Energy Related ^a | $C_{o(er)}$ | | | - | 67 | - | |
| Effective Output Capacitance, Time Related ^b | $C_{o(tr)}$ | $V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$ | | - | 232 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 7\text{ A}, V_{DS} = 480\text{ V}$ | - | 41 | 82 | nC |
| Gate-Source Charge | Q_{gs} | | | - | 8 | - | |
| Gate-Drain Charge | Q_{gd} | | | - | 16 | - | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 480\text{ V}, I_D = 7\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$ | | - | 16 | 32 | ns |
| Rise Time | t_r | | | - | 21 | 42 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 56 | 84 | |
| Fall Time | t_f | | | - | 31 | 62 | |
| Gate Input Resistance | R_g | | | $f = 1\text{ MHz}, \text{open drain}$ | | 0.2 | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 16 | A |
| Pulsed Diode Forward Current | I_{SM} | | | - | - | 38 | |
| Diode Forward Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 7\text{ A}, V_{GS} = 0\text{ V}$ | | - | 0.9 | 1.2 | V |
| Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 7\text{ A},$ $dI/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$ | | - | 288 | 576 | ns |
| Reverse Recovery Charge | Q_{rr} | | | - | 3.5 | 7.0 | μC |
| Reverse Recovery Current | I_{RRM} | | | - | 22 | - | A |

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

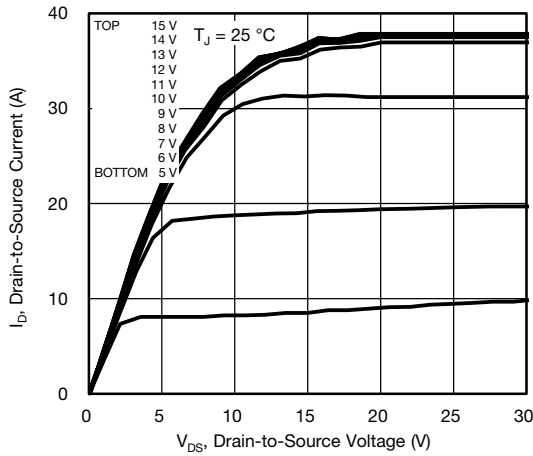


Fig. 1 - Typical Output Characteristics

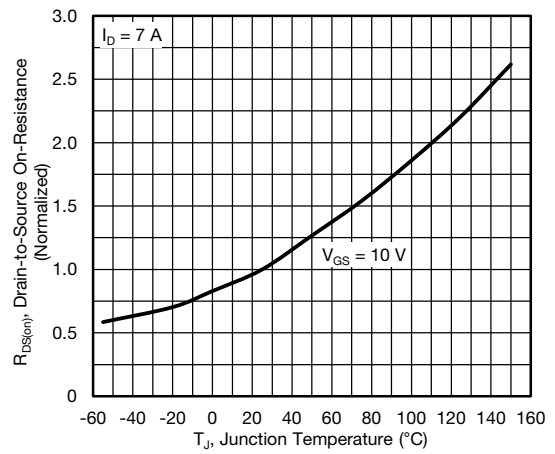


Fig. 4 - Normalized On-Resistance vs. Temperature

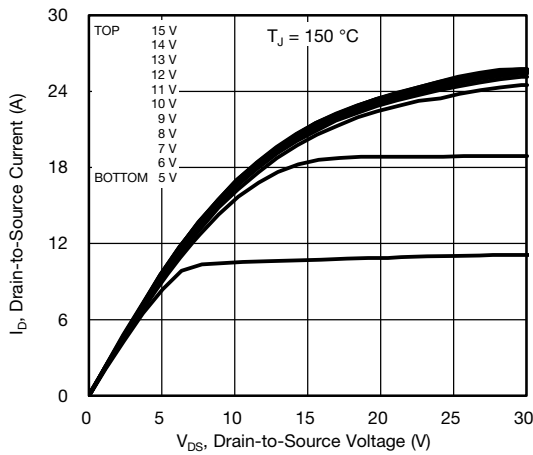


Fig. 2 - Typical Output Characteristics

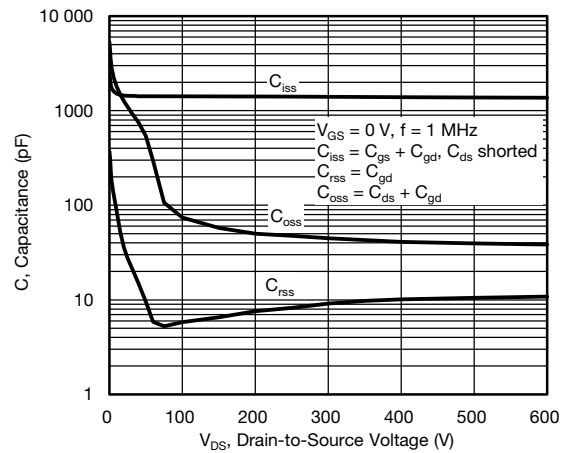


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

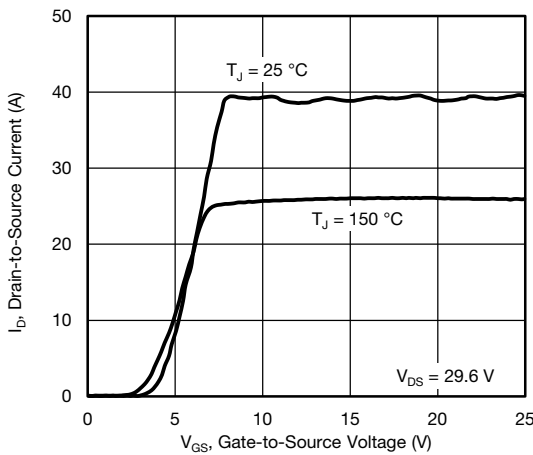


Fig. 3 - Typical Transfer Characteristics

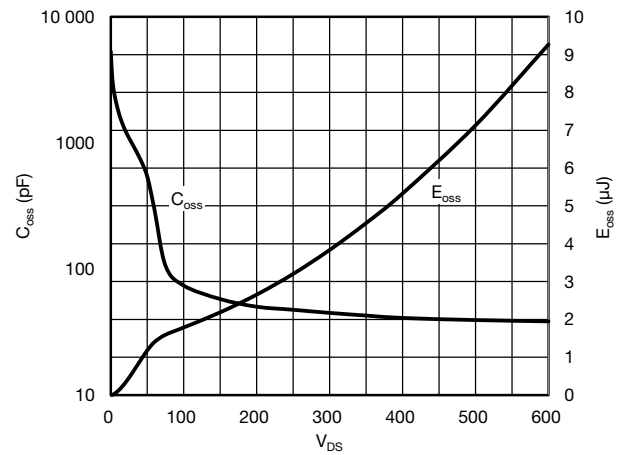


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

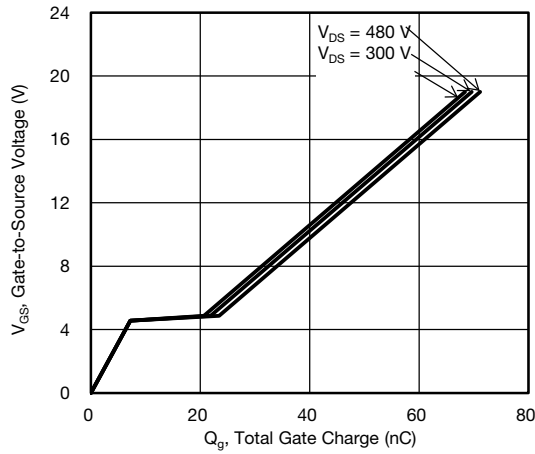


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

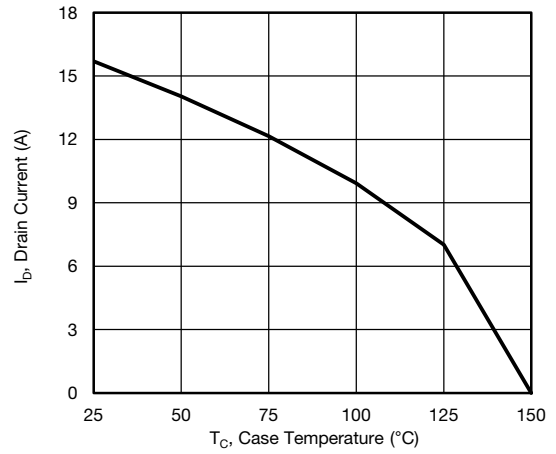


Fig. 10 - Maximum Drain Current vs. Case Temperature

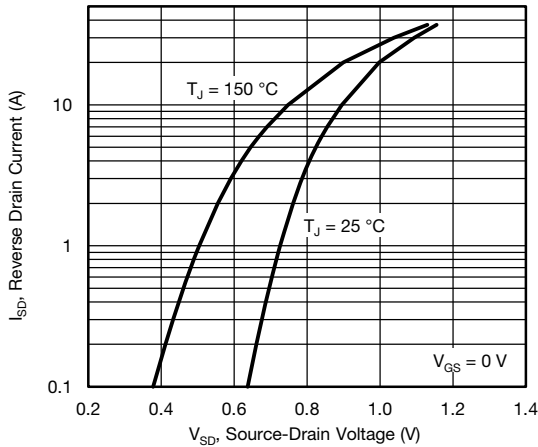


Fig. 8 - Typical Source-Drain Diode Forward Voltage

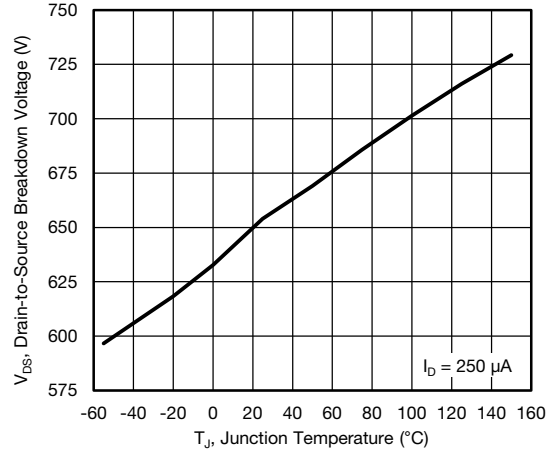


Fig. 11 - Temperature vs. Drain-to-Source Voltage

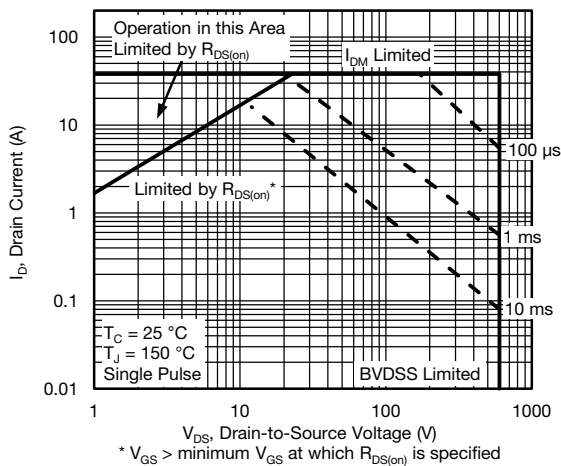


Fig. 9 - Maximum Safe Operating Area

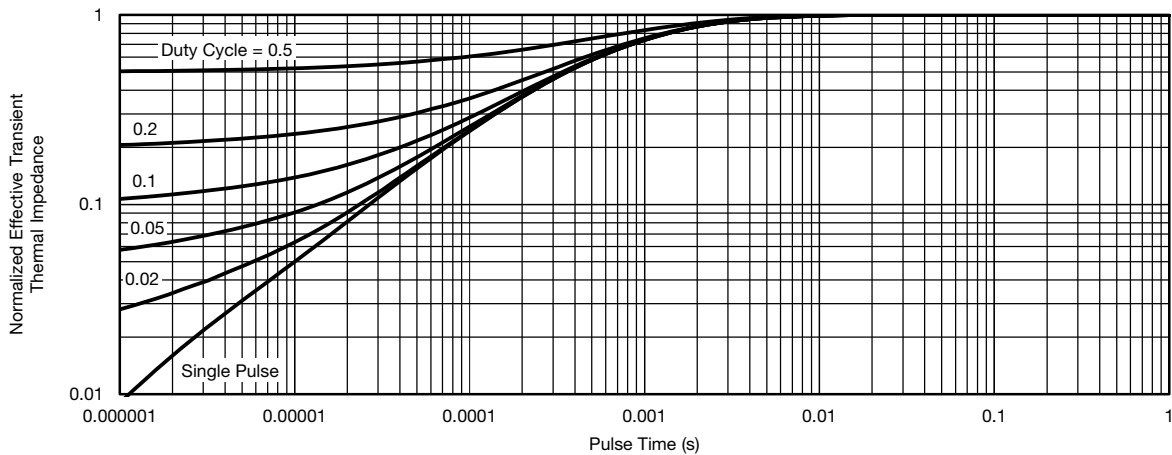


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

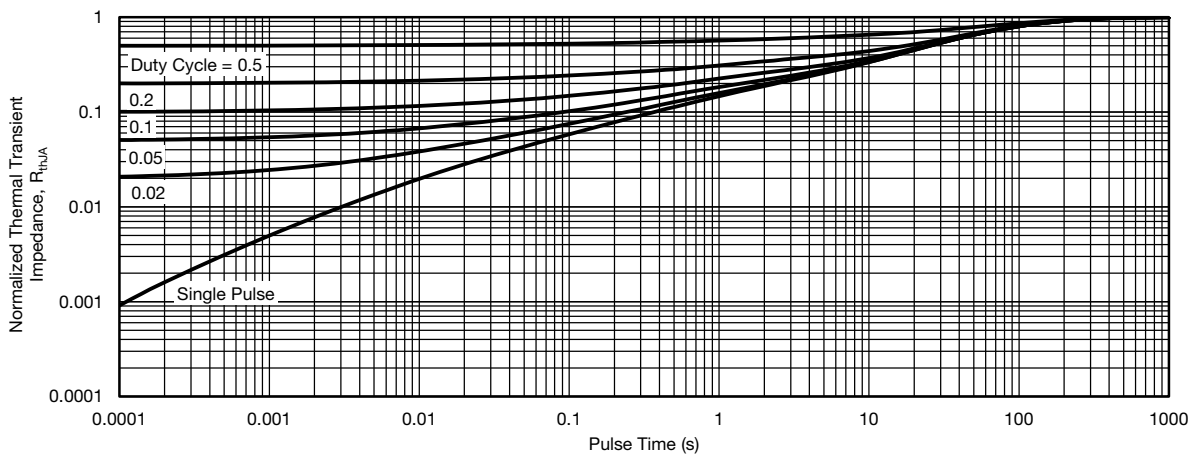


Fig. 13 - Normalized Thermal Transient Impedance, Junction-to-Ambient

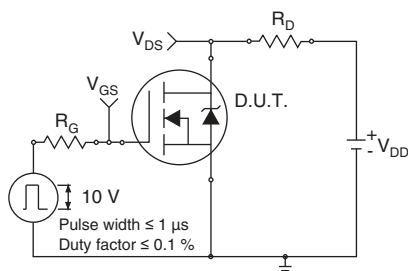


Fig. 14 - Switching Time Test Circuit

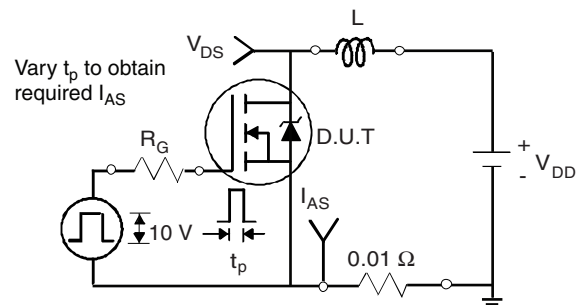


Fig. 16 - Unclamped Inductive Test Circuit

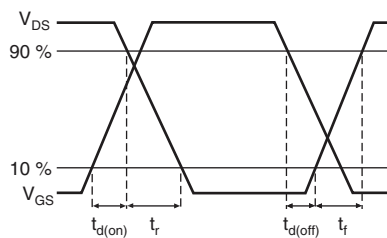


Fig. 15 - Switching Time Waveforms

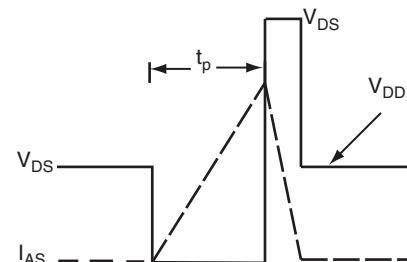


Fig. 17 - Unclamped Inductive Waveforms

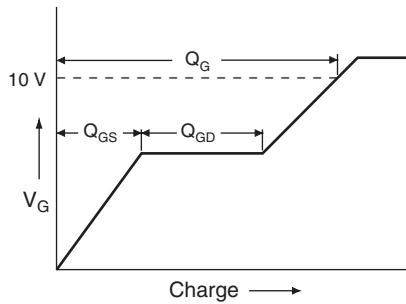


Fig. 18 - Basic Gate Charge Waveform

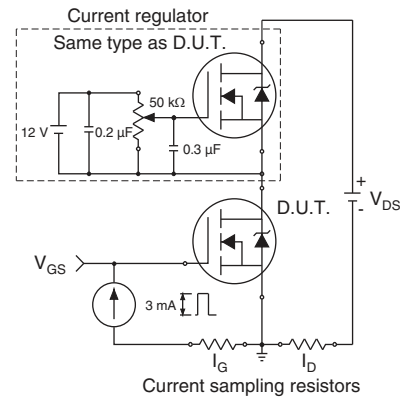
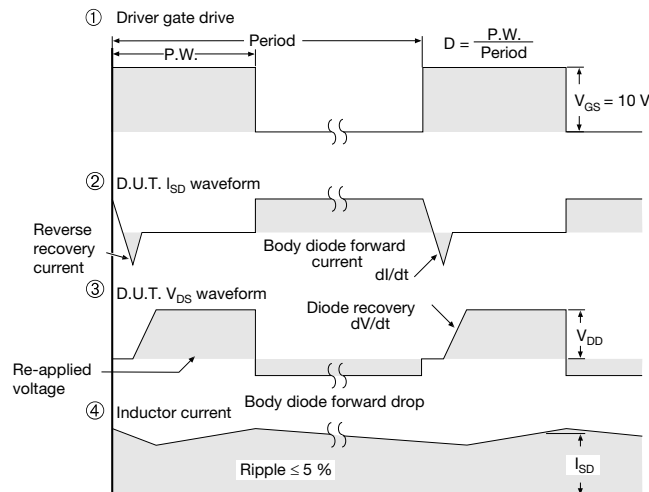
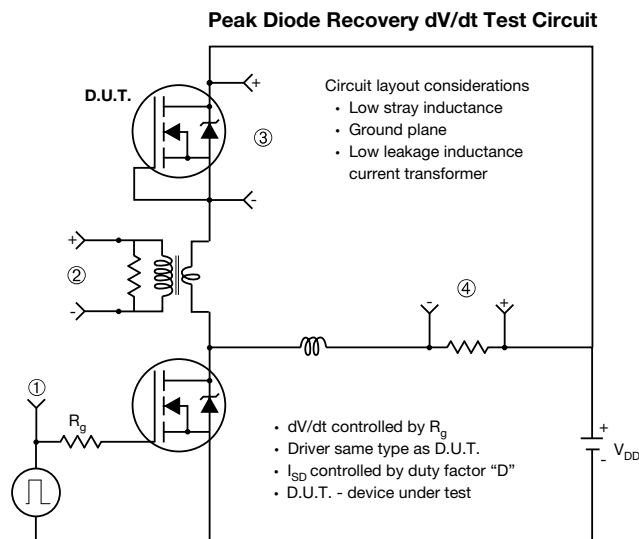


Fig. 19 - Gate Charge Test Circuit



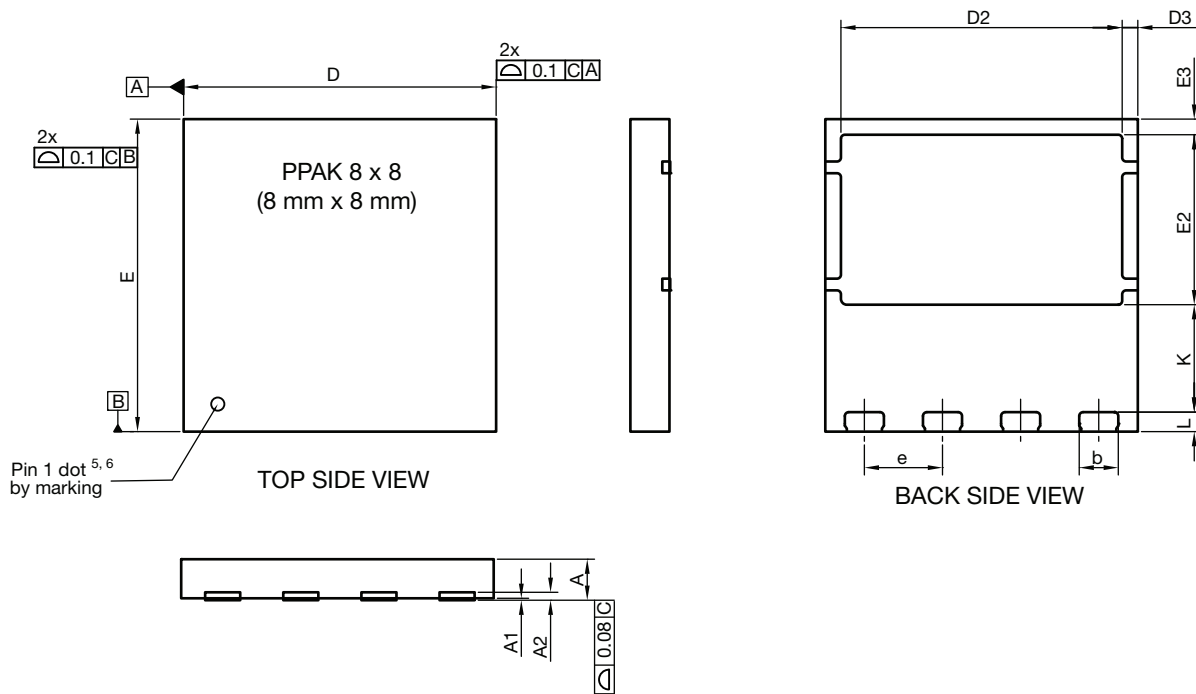
Note

a. $V_{GS} = 5V$ for logic level devices

Fig. 20 - For N-Channel

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PowerPAK[®] 8 x 8 Case Outline



| DIM. | MILLIMETERS | | | INCHES | | |
|------------------|-------------|------|------|------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| A1 | 0.00 | - | 0.05 | 0.000 | - | 0.002 |
| A2 | 020 ref. | | | 0.008 ref. | | |
| b | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| D | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| D2 | 7.10 | 7.20 | 7.30 | 0.280 | 0.283 | 0.287 |
| D3 | 0.40 BSC | | | 0.016 BSC | | |
| e | 2.00 BSC | | | 0.079 BSC | | |
| E | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| E2 | 4.30 | 4.35 | 4.40 | 0.169 | 0.171 | 0.173 |
| E3 | 0.40 BSC | | | 0.016 BSC | | |
| K | 2.75 BSC | | | 0.108 BSC | | |
| L | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| N ⁽³⁾ | 8 | | | 8 | | |

Notes

- (1) Use millimeters as the primary measurement
- (2) Dimensioning and tolerances conform to ASME Y14.5 M - 1994
- (3) N is the number of terminals
- (4) The pin 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- (5) Exact shape and size of this feature is optional

ECN: E20-0518-Rev. B, 28-Sep-2020
 DWG: 6041



Recommended Minimum PADs for PowerPAK[®] 8 mm x 8 mm



Dimensions in millimeters



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