IS2062/IS2064/BM62/BM64

IS2062/IS2064/BM62/BM64 Data Sheet Errata

IS2062/IS2064/BM62/BM64 Data Sheet Errata

The IS2062/IS2064/BM62/BM64 family of devices that you have received conform functionally to the current device data sheet except for the anomalies described in this document. Refer to the Microchip website for data sheets:

- https://www.microchip.com/wwwproducts/en/IS2062
- https://www.microchip.com/wwwproducts/en/IS2064
- https://www.microchip.com/wwwproducts/en/BM62
- https://www.microchip.com/wwwproducts/en/BM64

Affected Devices

Erratum	Affected Devices
EEPROM Content Corruption During Power Drop	IS2062, IS2064, BM62, and BM64

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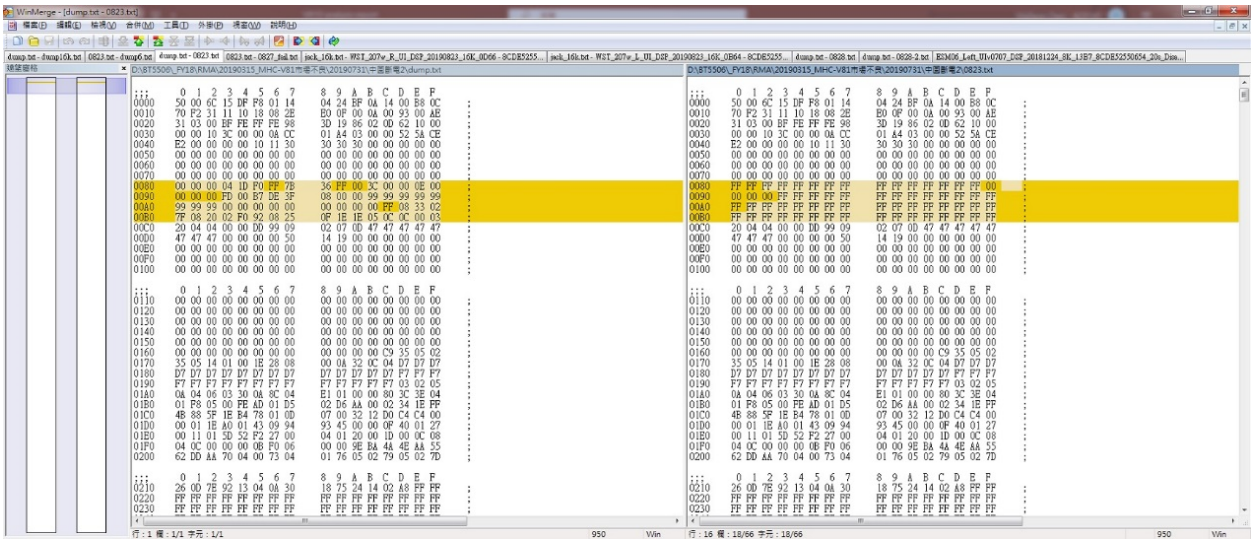
1. Errata Details

1.1 EEPROM Content Corruption During Power Drop

Under certain conditions, EEPROM content within the IS206x Bluetooth® Audio SoC can be corrupted with a specific pattern, a 64-byte sequence of 0xFF.

EEPROM write operations are typically performed within the IS206x SoC at runtime during, but not limited to, device pairing, shut down or while resetting to default configuration.

Figure 1-1. EEPROM Corrupted Data



Root Cause

If power goes down during the EEPROM write operation before it is completed, then a page of data in EEPROM may be corrupted. The first operation in an EEPROM write is a page-erase operation and typical evidence of EEPROM corruption is a 64-byte sequence of 0xFF.

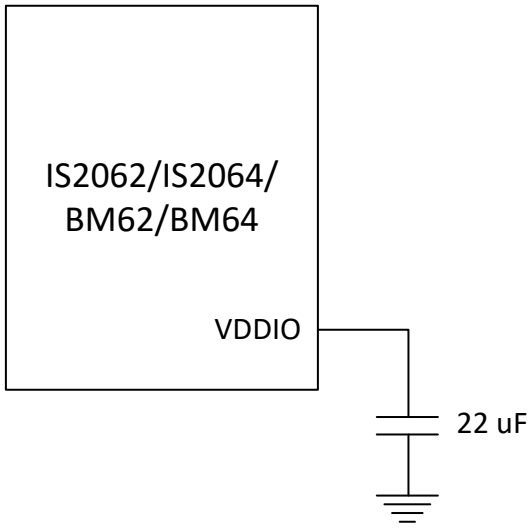
TWC (Total Write Time Cycle) for the EEPROM to complete an EEPROM write operation is 5 ms. A sudden power drop during the EEPROM write operation can result in corruption of EEPROM data in the page where the data byte resides since the writing of the data has not completed after the page erase process due to insufficient time allowed (5 ms). The page erase action will cause 64 bytes to become 0xFF before the data writing inside the page has concluded.

Work Around

Add a capacitor on the VDDIO power pin to delay the power drop to the EEPROM voltage supply line so that the TWC requirement may be met.

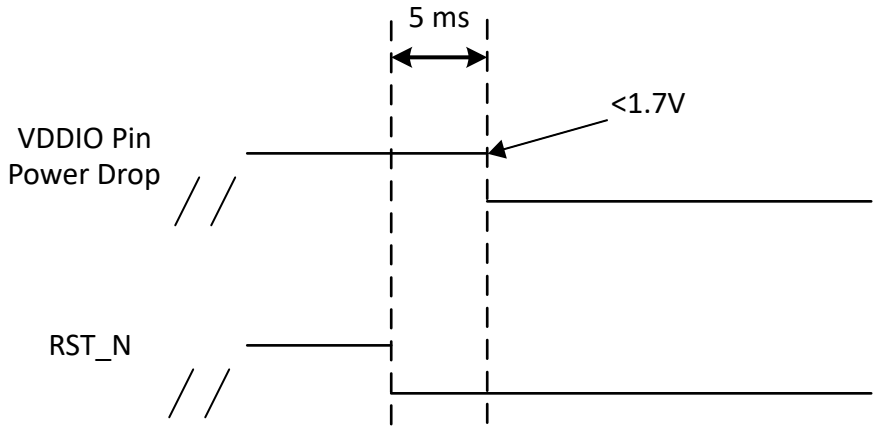
Both IS2062/IS2064 and BM62/BM64 data sheets specify an external Reset IC to protect the system from power drop. In addition to this protection IC, a 22 uF to 100 uF capacitor is suggested to add on the VDD_IO pin for delaying the power drop timing.

Figure 1-2. IS2062/IS2064/BM62/BM64 with Capacitor



Timing sequence for the RST_N signal and VDDIO drop is shown in the following figure.

Figure 1-3. RST_N Signal and VDDIO Drop Timing Sequence



2. Document Revision History

Revision	Date	Section	Description
B	01/2020	Figure 1-3	Updated figure
A	11/2019	Document	Initial Release

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