

# MOSFET - POWERTRENCH<sup>®</sup>, N-Channel

80 V, 110 A, 2.4 mΩ

## FDB86363-F085

### Features

- Typical  $R_{DS(on)} = 2.0\text{ m}\Omega$  at  $V_{GS} = 10\text{ V}$ ,  $I_D = 80\text{ A}$
- Typical  $Q_{g(tot)} = 131\text{ nC}$  at  $V_{GS} = 10\text{ V}$ ,  $I_D = 80\text{ A}$
- UIS Capability
- AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free, Halide Free and is RoHS Compliant

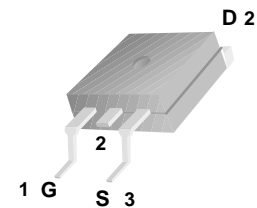
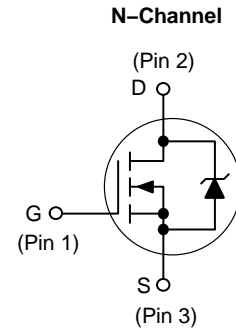
### Applications

- Automotive Engine Control
- Power Train Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems



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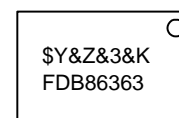


D<sup>2</sup>PAK-3 (TO-263, 3-LEAD)  
CASE 418AJ

### PIN CONFIGURATION

Position	Designation
Pin 1	Gate
Pin 2 / Tab	Drain
Pin 3	Source

### MARKING DIAGRAM



- \$Y = ON Semiconductor Logo
- &Z = Assembly Plant Code
- &3 = Numeric Date Code
- &K = Lot Code
- FDB86363 = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

## FDB86363–F085

### MOSFET MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ , Unless otherwise noted)

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-to-Source Voltage	80	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Drain Current –Continuous ( $V_{GS} = 10\text{ V}$ ) (Note 1) $T_C = 25^\circ\text{C}$	110	A
	–Pulsed $T_C = 25^\circ\text{C}$	See Figure 4	
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	512	mJ
$P_D$	Power Dissipation	300	W
	Derate Above $25^\circ\text{C}$	2.0	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	$-55$ to $+175$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	$^\circ\text{C/W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Current is limited by bondwire configuration.
- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.25\text{ mH}$ ,  $I_{AS} = 64\text{ A}$ ,  $V_{DD} = 80\text{ V}$  during inductor charging and  $V_{DD} = 0\text{ V}$  during time in avalanche.
- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a  $1\text{ in}^2$  pad of 2 oz copper.

### PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping <sup>†</sup>
FDB86363	FDB86363–F085	D2PAK (TO–263) (Pb–Free/Halide Free)	800 units / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

# FDB86363–F085

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### OFF CHARACTERISTICS

B <sub>V</sub> DSS	Drain-to-Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	80			V
I <sub>DSS</sub>	Drain-to-Source Leakage Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 25°C			1	μA
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175°C (Note 4)			1	mA
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>GS</sub> = ±20 V			±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2.0	3.0	4.0	V
R <sub>DS(on)</sub>	Drain-to-Source On-Resistance	I <sub>D</sub> = 80 A, V <sub>GS</sub> = 10 V, T <sub>J</sub> = 25°C		2.0	2.4	mΩ
		I <sub>D</sub> = 80 A, V <sub>GS</sub> = 10 V, T <sub>J</sub> = 175°C (Note 4)		3.8	4.3	

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 1 MHz			10000		pF
C <sub>oss</sub>	Output Capacitance				1400		pF
C <sub>rss</sub>	Reverse Transfer Capacitance				95		pF
R <sub>g</sub>	Gate Resistance	f = 1 MHz			3.3		Ω
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	V <sub>DD</sub> = 64 V, I <sub>D</sub> = 80 A		131	150	nC
Q <sub>g(th)</sub>	Threshold Gate Charge	V <sub>GS</sub> = 0 V to 2 V			18	21	nC
Q <sub>gs</sub>	Gate-to-Source Gate Charge				47		nC
Q <sub>gd</sub>	Gate-to-Drain "Miller" Charge				24		nC

### SWITCHING CHARACTERISTICS

t <sub>on</sub>	Turn-On Time	V <sub>DD</sub> = 40 V, I <sub>D</sub> = 80 A, V <sub>GS</sub> = 10V, R <sub>GEN</sub> = 6 Ω			231	ns
t <sub>d(on)</sub>	Turn-On Delay			38		ns
t <sub>r</sub>	Rise Time			129		ns
t <sub>d(off)</sub>	Turn-Off Delay			64		ns
t <sub>f</sub>	Fall Time			40		ns
t <sub>off</sub>	Turn-Off Time				135	ns

### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source-to-Drain Diode Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 80 A V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 40 A			1.25 1.2	V
t <sub>rr</sub>	Reverse-Recovery Time	I <sub>F</sub> = 80 A, ΔI <sub>SD</sub> /Δt = 100 A/μs, V <sub>DD</sub> = 64 V		88	101	ns
Q <sub>rr</sub>	Reverse-Recovery Charge			129	157	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T<sub>J</sub> = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

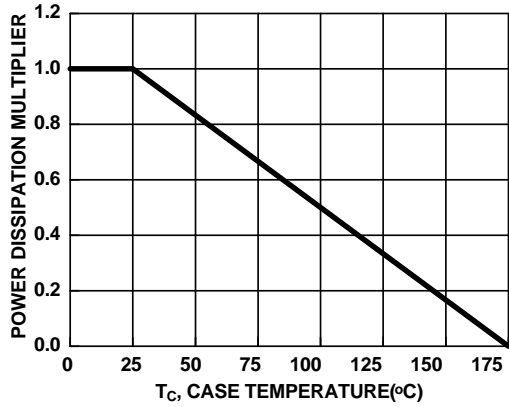


Figure 1. Normalized Power Dissipation vs. Case Temperature

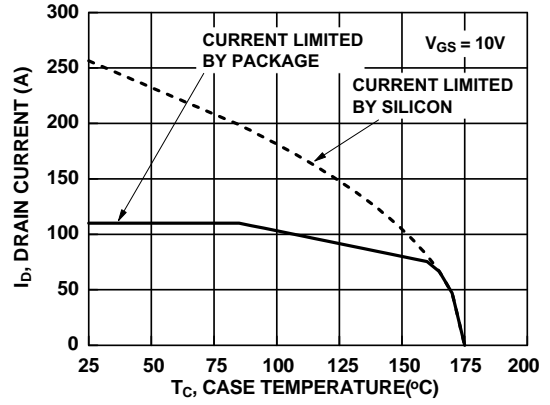


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

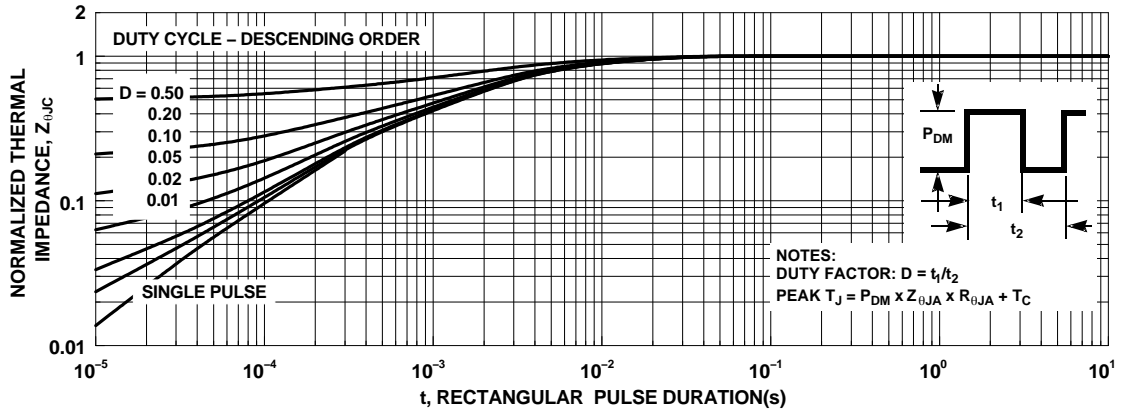


Figure 3. Normalized Maximum Transient Thermal Impedance

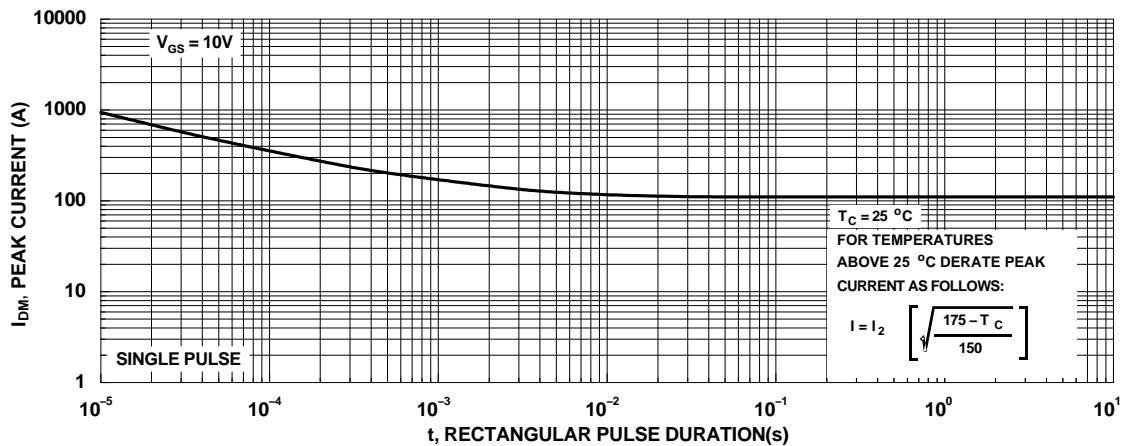


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

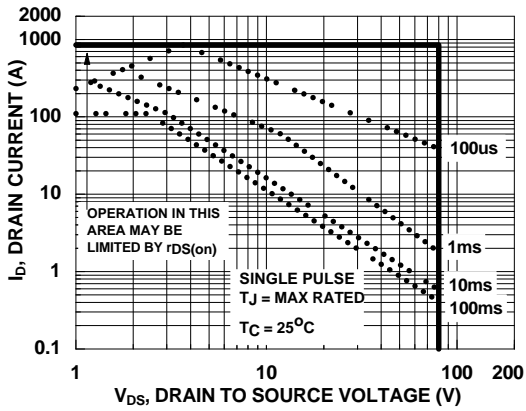
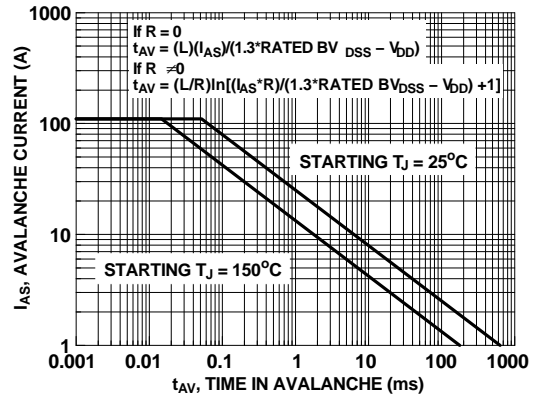


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

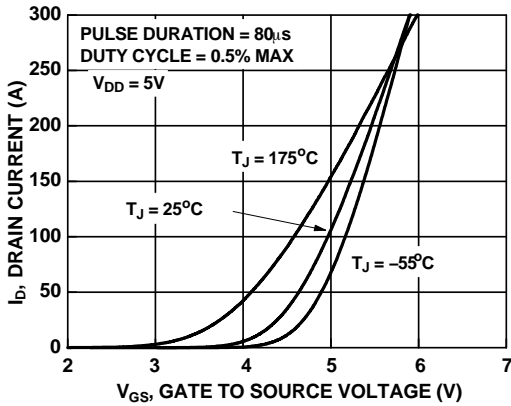


Figure 7. Transfer Characteristics

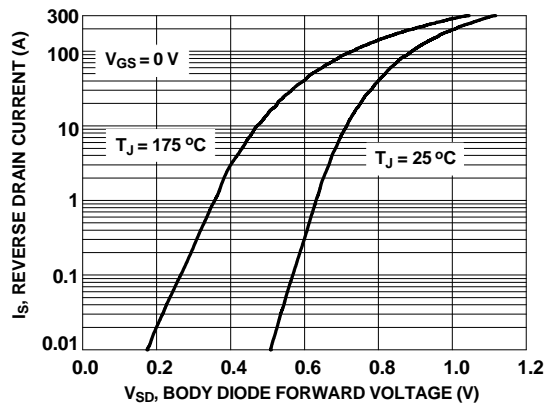


Figure 8. Forward Diode Characteristics

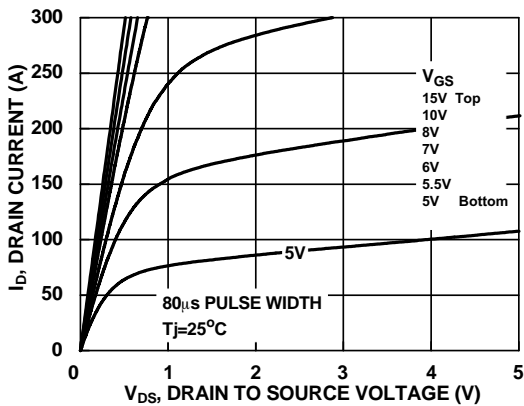


Figure 9. Saturation Characteristics

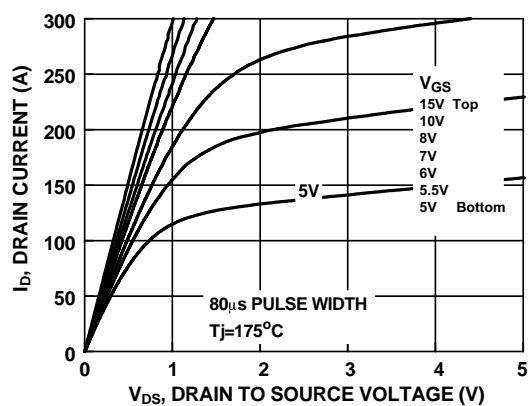


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

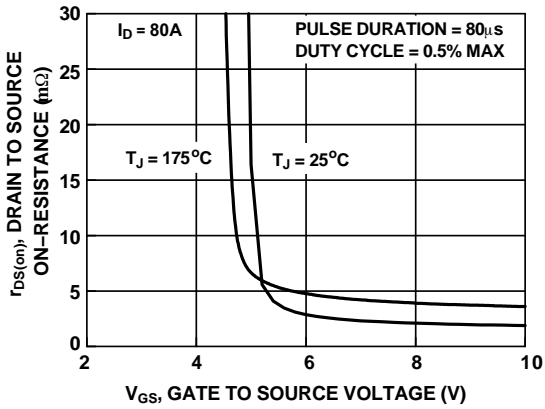


Figure 11.  $R_{DS(on)}$  vs. Gate Voltage

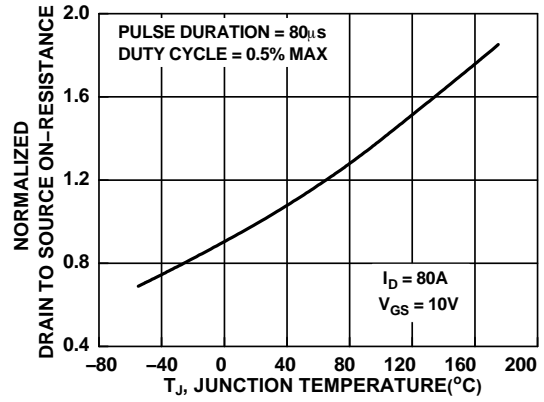


Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature

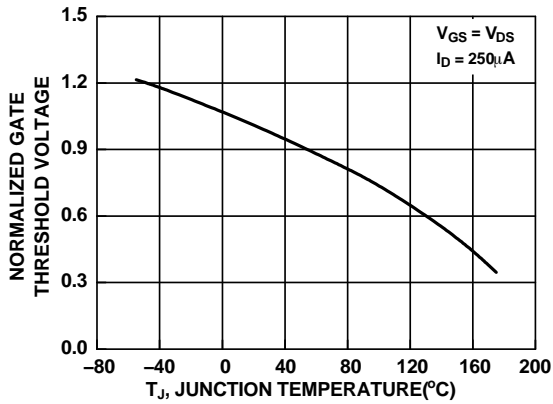


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

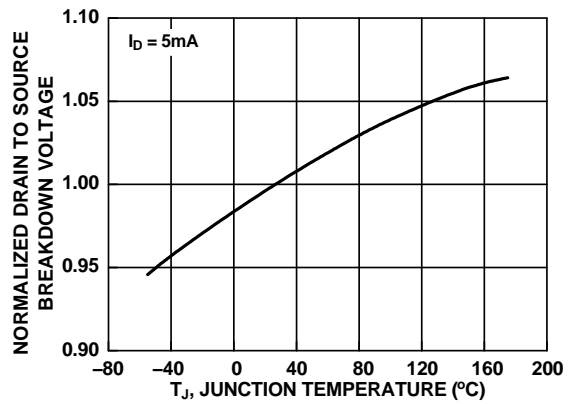


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

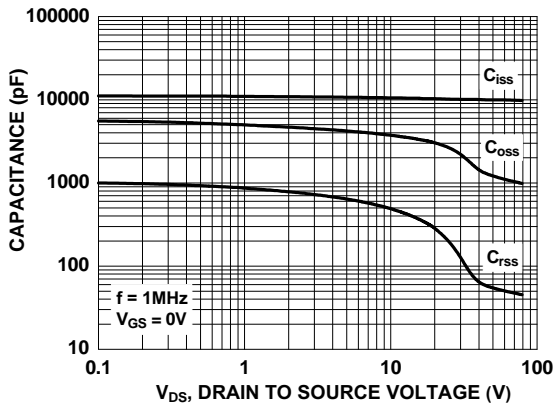


Figure 15. Capacitance vs. Drain to Source Voltage

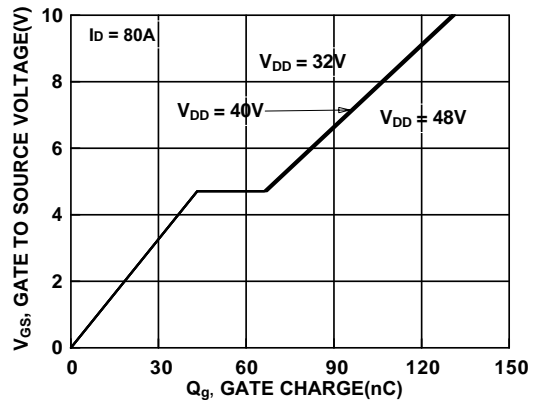


Figure 16. Gate Charge vs. Gate to Source Voltage

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

### D<sup>2</sup>PAK-3 (TO-263, 3-LEAD)

#### CASE 418AJ

#### ISSUE F

DATE 11 MAR 2021



#### RECOMMENDED MOUNTING FOOTPRINT

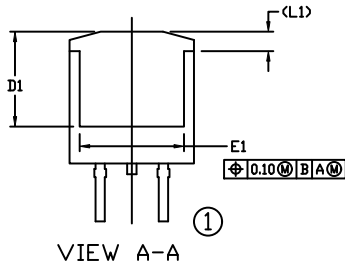
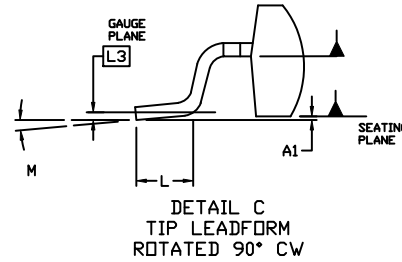
For additional information on our Pb-free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



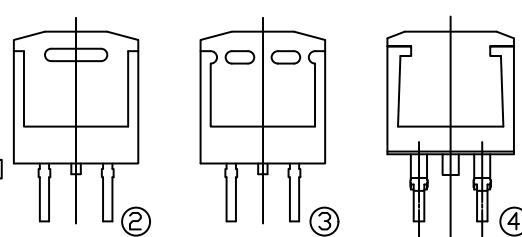
#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: INCHES
- CHAMFER OPTIONAL.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
- OPTIONAL MOLD FEATURE.
- ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	0*	8*	0*	8*

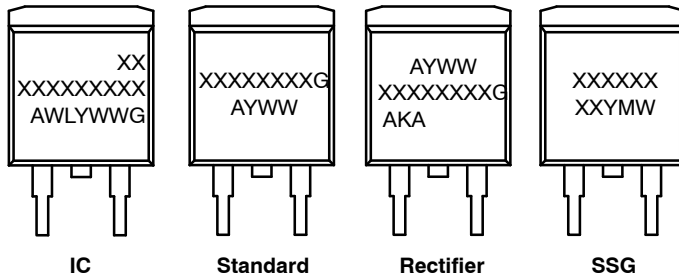


VIEW A-A



VIEW A-A  
OPTIONAL CONSTRUCTIONS

#### GENERIC MARKING DIAGRAMS\*



IC

Standard

Rectifier

SSG

- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- W = Week Code (SSG)
- M = Month Code (SSG)
- G = Pb-Free Package
- AKA = Polarity Indicator

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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