MEC172x
Silicon Errata and Data Sheet Clarification

TABLE 1: SILICON IDENTIFICATION

Part Number	Silicon Identifier	Functional Revision A	Functional Revision B	Functional Revision C(4)
MEC1721N-B0-I/LJ	Device ID(1)	0022_27h	0022_27h	0022_27h
	Revision ID for Silicon Revision(2)	00h	01h	02h
MEC1723N-B0-I/SZ	Device ID(1)	0022_34h	0022_34h	0022_34h
	Revision ID for Silicon Revision(2)	00h	01h	02h
MEC1723N-B0-I/LJ	Device ID(1)	0022_37h	0022_37h	0022_37h
	Revision ID for Silicon Revision(2)	00h	01h	02h
MEC1725N-B0-I/LJ	Device ID(1)	0022_57h	0022_57h	0022_57h
	Revision ID for Silicon Revision(2)	00h	01h	02h
MEC1727N-B0-I/SZ	Device ID(1)	0022_74h	0022_74h	0022_74h
	Revision ID for Silicon Revision(2)	00h	01h	02h
MEC1727N-B0-I/LJ	Device ID(1)	0022_77h	0022_77h	0022_77h
	Revision ID for Silicon Revision(2)	00h	01h	02h

Note 1: The Device ID is visible as an 8-bit number at Plug and Play Configuration Index 20h.
2: The HW Revision Number is visible as an 8-bit number at Plug and Play Configuration Index 21h.
3: Product Identification System (PIS) is defined in the Product Data Sheet.
4: The Rev C fixes have not been validated with silicon at this time. This is the current expectations.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item #	Issue Summary	Affected Revisions (1)	Affected Revisions (1)	Affected Revisions (1)
				A	B	C
QMSPI Controller	SPI Write	1.	API “api_qmspi_flash_cmd” does not write 3rd data byte for SPI Write only operation.	X	X	X
eSPI SAF	Prefetch data	2.	EC may return stale data to a eSPI 64 Byte read access, if prefetch and execute from Cache is enabled at the same time.	X	X	X
PCR	Processor Clock	3.	Processor clock switching may cause a clock glitch.	X	X	X
QMSPI	Shared SPI	4.	The SHD_SPI interface may not work at 96Mhz across all voltage and temperature ranges with sufficient margin.	X		

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item #	Issue Summary	Affected Revisions (1)	Affected Revisions (1)	Affected Revisions (1)
				A	B	C
SAF Bridge	Flash memory Sleep	5.	When eSPI Pre-fetch, Flash memory Sleep and Individual sleep enables are enabled together the EC may not enter sleep state	X		
PCR	JTAG Reset Status	6.	JTAG_RST# status does not reflect correctly on bit 7 of PCR Power Reset Status Register.	X		
Pads	5VT pad	7.	High leakage current on 5V Tolerant (5VT) pads	X		
Blinking/ Breathing LED	LED3	8.	LED3 is on GPIO226 alternate function 1 and not GPIO035 alternate function 4.	X		
Boot ROM	TAG1 Image Authentication	9.	Boot ROM does not authenticate the TAG1 image after Soft Reset.	X		
Boot ROM	JTAG Enable	10.	Boot ROM may take a long time to open JTAG port in case of Boot failure.	X		
Boot ROM	e(UDS) CRC	11.	Boot ROM clears E(UDS) CRC status bit in error when clearing SRAM.	X		
Boot ROM	Authentication	12.	Boot ROM revokes keys without authentication.	X		
PCR	VCC_PWRGD Status	13.	VCC_PWRGD status bit does not reflect the VCC_PWRGD pin status	X	X	X
ADC	Gain Error	14.	Analog to Digital converter Gain Error correction	X	X	X
QMSPI	LDMA TX	15.	Local DMA TX channel needs Block Soft reset after every transfer	X	X	X
VCI	VCI_IN0#	16.	VCI_IN0# has only falling (VCI_IN0# High to Low) interrupt available.	X	X	X
VCI	VCI_IN0#	17.	VCI_IN0# pin has no Schmitt input and any glitch protection	X	X	X
GPIO	GPIO	18.	GPIO230 through GPIO236 are not wake capable.	X	X	X
Manufacturability	Manufacturability	19.	Manufacturability and yield improvement			X
ADC	Channel 15	20.	ADC Channel 15 may exhibit low isolation relative to other ADC channels	X	X	X
eSPI	Prefetch	21.	eSPI prefetch feature should be disabled.	X	X	X
Boot ROM	TRNG	22.	Boot ROM does not disable TRNG at Boot exit	X	X	X

Silicon Errata Issues

1. Module: QMSPI Controller

DESCRIPTION

API “api_qmspi_flash_cmd” does not write 3rd data byte for SPI Write only operation.

While initiating a flash command with only transmit function (write) and having more than 3 bytes, API “api_qmspi_-flash_cmd” fails to transmit the third byte.

END USER IMPLICATIONS

While initiating a flash command with only transmit function (SPI Flash memory write) and having more than 3 bytes, API “api_qmspi_flash_cmd” fails to transmit the third byte. This issue is only observed while running the QMSPI block at 12MHz clock frequency or lower. The CLIB/PLIB collateral will have a recommended solution for this issue as a PLIB function.

2. Module: eSPI SAF Block

DESCRIPTION

EC may return stale data to a eSPI 64 Byte read access, if prefetch and execute from Cache is enabled at the same time.

if a flash is being modified over eSPI and verified 64 bytes at a time, and if the Prefetch feature and the new Cache feature are both active, eSPI may return stale data from before the Write was performed.

END USER IMPLICATIONS

User may not be able to use the exact below sequence.

Program aligned 64 bytes, Read back the same 64 bytes, Program next 64 bytes, Read back these 64 bytes.

Work Around

Only the above described sequence is affected when eSPI 64 Byte read access to the previously written location is done with Prefetch and execute from Cache enabled at the same time. It is recommended that eSPI read some other address in between Write and Read to the same 64 Byte address or read the same 64 Byte address twice.

3. Module: PCR Block

DESCRIPTION

Processor clock switching may cause a clock glitch.

Glitch on the clock may corrupt the instruction and data fetch from the memory.

END USER IMPLICATIONS

Processor may end up in unknown state.

Work Around

The above problem can be completely avoided by using 4 NOP instruction before and after the processor clock switch instruction followed by Data and Instruction Barrier instruction as shown in the sample code below.

```
__nop; __nop; __nop; __nop;
(*(unsigned char*) 0x4008_0104 = Clock Divide value;
__nop; __nop; __nop; __nop;
__DSB(); // Data instruction barrier to complete any write before the next instruction
__ISB(); //Instruction barrier to complete the instruction and to flush the pipe
```

4. Module: QMSPI Block

DESCRIPTION

The SHD_SPI interface may not work at 96Mhz across all voltage and temperature ranges with sufficient margin.

END USER IMPLICATIONS

When used at 96MHz, the Shared SPI interface (SHD_* pins) may not transfer data properly at 96MHz across all voltage and temperature ranges.

Work Around

For Rev A parts, 96Mhz on Shared SPI interface should not be used for production.

5. Module: SAF Bridge Block

DESCRIPTION

When eSPI Pre-fetch, Flash memory sleep and Individual block sleep enables are enabled together the EC may not enter sleep state.

END USER IMPLICATIONS

When eSPI Pre-fetch, Flash memory sleep and Individual block sleep enables are enabled together the EC may not enter sleep state and continue to consume normal power.

Work Around

This problem can be solved by using Sleep All bit instead of Individual block sleep enable bits.

6. Module: PCR Block

DESCRIPTION

JTAG_RST# status does not reflect correctly on bit 7 of PCR Power Reset Status Register.

END USER IMPLICATIONS

Raw JTAG RESET pin (JTAG_RST#) status does not reflect correctly on bit 7 of PCR Power Reset Status Register. This bit status should not be used to determine the JTAG_RST# pin status by the application code.

Work Around

Currently there is no workaround for this problem.

7. Module: Pads Block

DESCRIPTION

High leakage current on 5V Tolerant (5VT) pads.

END USER IMPLICATIONS

5V-tolerant (5VT) pads show leakage of about 12uA at room when applying 5V with all VTRs down.

Work Around

There is no workaround for this issue in Rev A.

8. Module: Blinking/Breathing LED Block

DESCRIPTION

LED3 is on GPIO226 alternate function 1 and not GPIO035 alternate function 4.

END USER IMPLICATIONS

LED3 is on alternate function 1 on GPIO226.

Work Around

LED3 is not on GPIO0035 alternate function 4. LED3 is on alternate function 1 on GPIO226 in Rev A parts. This needs to be considered for PCB design.

9. Module: Boot ROM Block

DESCRIPTION

Boot ROM does not authenticate the TAG1 image after Soft Reset, if the key hash Blob was authenticated previously.

END USER IMPLICATIONS

When Boot ROM validates a key hash blob, it sets an associated flag in a scratch register to indicate that the blob was checked. If a “checked” flag is already set following a soft reset, the Boot ROM will not use the associated key hash blob to authenticate a TAGx image.

Work Around

There is no workaround for this issue in Rev A.

10. Module: Boot ROM Block

DESCRIPTION

Boot ROM may take a long time to open JTAG port in case of Boot failure.

END USER IMPLICATIONS

By default at Power On Reset (POR) the JTAG port is disabled and locked. When Boot ROM runs the final Boot exit sequence, it enables the JTAG port if Debug is enabled through the OTP bit. In case of Boot failure, the Boot ROM may try up to 15 attempts to authenticate, decrypt and load the application image taking considerable time. In case power sequencing feature is enabled through OTP, there may be even longer delay or wait for power up event, before JTAG port is enabled.

Work Around

If the JTAG port is not been opened up and power sequencing feature is enabled in the part, please ensure all Power sequencing event complete as expected. There is no workaround for this issue in Rev A parts. This issue is fixed in Rev B.

11. Module: Boot ROM

DESCRIPTION

Boot ROM clears E(UDS) CRC status bit in error when clearing SRAM.

END USER IMPLICATIONS

Application code does not know if the E(UDS) value stored in the read/write locked OTP memory has been altered from its original programmed value.

Work Around

None. There is no fix for this problem in Rev A parts, however it is fixed in Rev B parts.

12. Module: Boot ROM

DESCRIPTION

Boot ROM only set the authentication status bits if authentication is enabled and the authentication check fails.These bits are not set when:

- Authentication enabled and authentication passes.
- Authentication disabled and the hash integrity check fails.

END USER IMPLICATIONS

If authentication is not enabled, the authentication status of both images is unknown. User must not use these bits when authentication is disabled.

Work Around

We have common status bit which will tell which TAG image has been loaded for images with integrity check.

TABLE 3: ROM ACTION FLAG 64 BITS TOTAL (0X1F4)

Bit Number	Description
27	RLOG_LOAD_FROM_TAG0
28	RLOG_LOAD_FROM_TAG1

There is no fix for this problem in Rev A parts, however it is fixed in Rev B parts.

13. Module: PCR Block

DESCRIPTION

VCC_PWRGD status at bit[2] in PCR Power Reset Status Register does not give the value of VCC_PWRGD pin.

END USER IMPLICATIONS

VCC_PWRGD status at bit[2] in PCR Power Reset Status Register at offset 0x10 in PCR block does not give the status of VCC_PWRGD pin. If the EC application code waits for this bit to be asserted before asserting PWR_INV bit, the code will not proceed further.

Work Around

VCC_PWRGD is on GPIO057 (GPIO057/VCC_PWRGD). The workaround is to read the GPIO input register of GPIO057 in place of VCC_PWRGD status. This will give the value of VCC_PWRGD pin.

14. Module: Analog to Digital converter Gain Error Correction

DESCRIPTION

VREF observed at ADC input is less than VREF applied to external pin and requires correction in ADC calculations.

END USER IMPLICATIONS

Real internal VREF is less then external one. This causes gain error.

Work Around

For all measurements,10 or 12 bit ADC, VREF value has to be corrected by application code as below.

VREF_ACTUAL = VREF- VREF/Alpha, where VREF_ACTUAL is the actual ADC reference. Rounding of VREF_ACTUAL to the nearest allowable precision digit should be done as the last step before substituting the value in the below equation to calculate the input voltage.

VREF is the external ADC reference.

Input Voltage = (ADC Reading + [Beta])*(VREF_ACTUAL)/((2^res)-1) where res = 10 or 12, respectively, depending on bit resolution used.

TABLE 4: ALPHA AND BETA VALUE FOR ADC READING CORRECTION

Vref	Alpha	Beta for 10 bit resolution	Beta for 12 bit resolution
3.3V	0x86	1	3
3.0V	0x10E	1	3

15. Module: QMSPI LDMA TX Channel Requires Soft Reset After Every Transfer

DESCRIPTION

The QMSPI LDMA TX Channel has a corner case where the transfer may not happen on the SPI bus. This condition only occurs for the FW initiated QMSPI LDMA TX Channel and does not affect any other transfer from any other source.

END USER IMPLICATIONS

When the error condition happens, the transfer does not happen on the SPI bus and there is no indication of this error to the EC.

Work Around

The QMSPI LDMA TX requires soft reset after every transfer to reset all the internal variables. This would mean that all the registers will have to be reprogrammed after soft reset. Our recommendation is to save and restore the following QMSPI registers after every soft reset: Mode, Interface Control, CS Timing, Mode ALT1, TAPS, TAPS ADJ, TAPS CTRL. These registers do not change for every transaction. All other registers will need to be reprogrammed.

16. Module: VCI_IN0# has only falling edge interrupt

DESCRIPTION

VCI_IN0# has only falling (VCI_IN0# High to Low) interrupt available. VCI_IN0# does not have rising (VCI_IN0# Low to High) interrupt available.

END USER IMPLICATIONS

Customer will not be able to get the VCI_IN0# rising interrupt.

Work Around

Tie VCI_IN0# with any of the free and available VCI_IN1#, VCI_IN2#, VCI_IN3# or VCI_IN4# pins and use VCI_IN0# for VCI_OUT generation and the other VCI_IN1#, VCI_IN2#, VCI_IN3# or VCI_IN4# pin connected to VCI_IN0# to get the interrupts.

17. Module: VCI_IN0# pin has no Schmitt input and any glitch protection

DESCRIPTION

VCI_IN0# pin has no Schmitt input and any glitch protection, so any noise as small as 10mV from high to low will generate the interrupt

END USER IMPLICATIONS

Noise of 10mV could generate false VCI_IN0# interrupt.

Work Around

Tie VCI_IN0# with any of the free and available VCI_IN1#, VCI_IN2#, VCI_IN3# or VCI_IN4# pins and use VCI_IN0# for VCI_OUT generation and the other VCI_IN1#, VCI_IN2#, VCI_IN3# or VCI_IN4# pin connected to VCI_IN0# to get the interrupts.

18. Module: GPIO230 through GPIO236 are not wake capable

DESCRIPTION

GPIO230 through GPIO236 are not wake capable.

END USER IMPLICATIONS

Customer should not use these GPIO’s for waking up EC from light and heavy sleep condition. The system may not wake from light and heavy sleep if any of GPIO230 through GPIO236 are used as wake up source for EC.

Work Around

Customer should use other wake capable GPIO's. GPIO230 through GPIO236 have interrupts and wake cable interrupt. Only the GPIO wake interrupts are not connected, the regular interrupt to EC works correctly. All other wake capable GPIO's implemented in the package and defined in the Table 3-3 "Interrupt Aggregator Bit Assignments", are wake capable. VCI_IN4# on GPIO234 is EC wake capable and will be able to wake the EC from Light and heavy sleep, however GPIO234 is not wake capable.

19. Module: Manufacturability and yield improvement

DESCRIPTION

Minor change to the physical design for manufacturability and yield improvement.

END USER IMPLICATIONS

No impact to FW or Hardware Design.

20. Module: ADC

DESCRIPTION

Under certain operating conditions of ADC conversion, ADC channel 15 may exhibit low isolation relative to other ADC channels, causing ADC channel 15 voltage to bleed through to ADC channel 0 through14, irrespective of channel 15 configuration settings or GPIO pin control register settings.

END USER IMPLICATIONS

Any ADC channel that is actively involved in an ADC conversion is susceptible to cross-talk from channel 15.

Work Around

Do not apply voltage to ADC channel 15 while any other channel is undergoing conversion. The resistance of the external circuitry which is driving any particular ADC channel input is a significant factor in influencing the magnitude of the cross-talk. The greater the deviation from an ideal, zero-resistance output stage feeding each ADC channel, the greater the susceptibility to cross-talk from channel 15. Applying ground to ADC Ch. 15 while other ADC channels are in use is advisable. All other ADC channels should be exhausted before utilizing channel 15. Additionally, if any of ADC channel 0 through ADC channel 14 are to be used for GPIO operation (as set by the respective Pin Control Register), care should be taken that no ADC conversion is triggered on that same GPIO pin. This will similarly expose the selected GPIO pin to potential adverse readings due to conflict with the ADC.

21. Module: eSPI

DESCRIPTION

When the eSPI Prefetch feature is enabled, and there are prefetch transfers from both eSPI and EC, there may be a case when the state machine may get stuck and not complete the transfer.

END USER IMPLICATIONS

If prefetch feature is enabled and there is read from both eSPI and EC with, eSPI block in EC may get stuck and not return data even if it has fetched the data from the Flash memory.

Work Around

Do not enable prefetch mode of eSPI block.

22. Module: Boot ROM

DESCRIPTION

If application code encryption and Authentication is enabled, Boot ROM uses True Random Number Generator (TRNG). Boot ROM does not disable the TRNG block during boot exit sequence.

END USER IMPLICATIONS

This results in higher power consumption when the application runs and when the EC goes in light and heavy sleep mode.

Work Around

The workaround for this issue is to call TRNG block disable from application code using ROM API, mchp_ndrng_enable(FALSE). This will disable the TRNG block and put it to sleep. Application code should do this at the start of the application code to reduce the power consumed by EC.

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet.

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

TABLE 5: DATA SHEET CLARIFICATION SUMMARY

Module	Item Number	Issue Summary
Boot ROM	1.	In MEC172x ROM description addendum TABLE 5-5: FIRMWARE IMAGE HEADER FORMAT, in Byte “0x14 to 0x17”, Bits [5:0] should be read as Bits [6:0].
ARM M4F	2.	ARM M4F base address is 0xE000ED00 and is incorrect in Table 3-5 in the data sheet.
IO Pads	3.	Power sequence for Sleep and Wake up should ensure IO Pads of the rails that will be unpowered are all disabled, if Core voltage remains on.
EC Subsystem	4.	Crypto bandwidth needs to be optimized.
CACHE Controller	5.	Cache is an optional feature in this family of parts.
Internal SPI	6.	It is recommended that internal SPI pins should be configured to drive high during chip sleep.
OTP	7.	TABLE C-1: OPTIONAL OTP FEATURES in MEC172x ROM Description Addendum OTB Bytes 416-991 should be read as OTP bytes 416-671 and 960-979 are Microchip reserved and OTP Bytes 672 -959 are for Application Use.
Internal SPI	8.	Internal flash must be in sleep for least power in heavy sleep.
Pad	9.	Pads are held in reset and connected to pull down resistor during power up
VCI	10.	VCI_IN0# has purely combinatorial path and do not have Input Enable.
VCI	11.	VCI_OVRD_IN pin does not have input buffer control.
WDT	12.	WDT Control Register bit 2 HIBERNATION_TIMER_STALL definition is corrected
QMSPI	13.	TABLE 57-19: “SPI SETUP AND HOLD TIMES PARAMETERS” values are incorrect in datasheet

1. Module: Boot ROM

In the MEC172x ROM description addendum document TABLE 5-5: FIRMWARE IMAGE HEADER FORMAT, in “Byte 0x14 to 0x17” row “Bits [5:0] must be 0” should be read as “Bits [6:0] must be 0” so as to be evenly divisible by 128.

2. Module: ARM M4F

ARM M4F module base address and registers mentioned in Table 3-5 REGISTER MAP are incorrect. The correct addresses of the registers are given in the below table.

TABLE 3-5 REGISTER MAP

Block	Instance	Register	Host Type	Register Address
ARM M4F	0	Auxiliary_Control		E000E008
ARM M4F	0	SystemTick_Ctrl_Status		E000E010
ARM M4F	0	SystemTick_Reload_Value		E000E014
ARM M4F	0	SystemTick_Current_Value		E000E018
ARM M4F	0	SystemTick_Calibration_Value		E000E01C
ARM M4F	0	CPU_ID		E000ED00
ARM M4F	0	Interrupt_Ctl_and_State		E000ED04

Block	Instance	Register	Host Type	Register Address
ARM M4F	0	Vector_Table_Offset		E000ED08
ARM M4F	0	Application_Interrupt_and_Reset_Ctl		E000ED0C
ARM M4F	0	System_Ctl		E000ED10
ARM M4F	0	Config_and_Ctl		E000ED14
ARM M4F	0	System_Handler_Priority1		E000ED18
ARM M4F	0	System_Handler_Priority2		E000ED1C
ARM M4F	0	System_Handler_Priority3		E000ED20
ARM M4F	0	System_Handler_Ctl_and_State		E000ED24
ARM M4F	0	Configurable_Fault_Status		E000ED28
ARM M4F	0	Hard_Fault_Status		E000ED2C
ARM M4F	0	Debug_Fault_Status		E000ED30
ARM M4F	0	Debug_Halting_Ctl_and_Status		E000EDF0
ARM M4F	0	Debug_Core_Register_Selector		E000EDF4
ARM M4F	0	Debug_Core_Register_Data		E000EDF8
ARM M4F	0	Debug_Exception_and_Monitor_Ctl		E000EDFC
ARM M4F	0	Bus_Fault_Address		E000ED38
ARM M4F	0	Auxiliary_Fault_Status		E000ED3C
ARM M4F	0	Processor_Feature0		E000ED40
ARM M4F	0	Processor_Feature1		E000ED44
ARM M4F	0	Debug_Features0		E000ED48
ARM M4F	0	Auxiliary_Features0		E000ED4C
ARM M4F	0	Memory_Model_Feature0		E000ED50
ARM M4F	0	Memory_Model_Feature1		E000ED54
ARM M4F	0	Memory_Model_Feature2		E000ED58
ARM M4F	0	Memory_Model_Feature3		E000ED5C
ARM M4F	0	Instruction_Set_Attributes0		E000ED60
ARM M4F	0	Instruction_Set_Attributes1		E000ED64
ARM M4F	0	Instruction_Set_Attributes2		E000ED68
ARM M4F	0	Instruction_Set_Attributes3		E000ED6C
ARM M4F	0	Instruction_Set_Attributes4		E000ED70
ARM M4F	0	Coprocessor_Access_Ctl		E000ED88
ARM M4F	0	Software_Triggered_Interrupt		E000EF00

3. Module: IO Pads

When any of the VTR rails are turned OFF while VTR_REG is still powered up, the EC firmware must ensure that all the IO pads on those rails are disabled (input disabled) when the IO Pad rail (VTR1, VTR2 and VTR3) are powered down. This will ensure that there is no crowbar current through the IO pads.

4. Module: EC Subsystem Block

DESCRIPTION

Crypto bandwidth needs to be optimized.

Work Around

Program 0x0500 at register offset 0x58 in EC Subsystem for proper system performance while Crypto operations are running. This will ensure that there is sufficient AHB bandwidth for other high speed peripheral to share the AHB bus while Crypto operations are being executed.

5. Module: CACHE Controller Block

DESCRIPTION

Cache is an optional feature in this family of parts. Please contact Microchip sales and marketing if you require this feature.

6. Module: Internal SPI

For MEC1727 parts containing internal SPI memory, it is recommended that internal SPI GPIO pins should be configured to drive high during chip sleep. The application firmware should program GPIO074, GPIO075, GPIO116 and GPIO117 to drive logic 1 before going to sleep state. This will reduce the sleep current.

7. Module: OTP

Boot ROM document does not correctly mention the Application use space in TABLE C-1: OPTIONAL OTP FEATURES in MEC172x ROM Description Addendum. The Table C-1 mentions that Bytes 480 to 991 is for Application use. However OTP bytes 416-671 and 960-979 are Microchip reserved. OTP Bytes 672 -959 are available for Application use. All other portions of the table are correct.

8. Module: Internal SPI

In MEC1727 that contains internal SPI Flash memory, application firmware code must put the Internal SPI in sleep mode by writing command byte 0x89 to internal SPI and program the associated GPIO's in pad disable mode before enabling heavy sleep in EC to have minimum power consumption.The internal GPIO pins that need to be input disabled are GPIO074, GPIO075, GPIO076, GPIO116 and GPIO117.

9. Module: Pads

DESCRIPTION

During EC power up, the pad protection logic holds the pads in reset and connects it to ground via a 60KOhm typical pull down resistor until the pad power is within the operating range. This means that if there is an external pull up resister on the pad, there will be voltage drop across the internal pull down resister, resulting in voltage at the pad pin during power up.

END USER IMPLICATIONS

If there is a pull up resistor on the GPIO pin, there will be current path from the external pull up through the internal pad pull down resister during power up, resulting in voltage at the pad during power up. Customer should account for 60KOhm typical (minimum is 40KOhm and Maximum is 80KOhm) of pull down resistor in the pad during power up. Once the pad power pin voltage is above the minimum threshold (Power Good signal is asserted), the pad pull down resistor will be disabled and all the pads will be in Input/output/interrupt disabled state, except for the ones described in TABLE 3-4: GPIO PIN CONTROL DEFAULT VALUES in the data sheet.

Work Around

Customer should choose the Pull up resistor value to ensure minimum voltage at the pad pin during power up.

10. Module: VCI_IN0# has purely combinatorial path and do not have Input Enable

DESCRIPTION

In VBAT-POWERED CONTROL INTERFACE chapter, VCI Input Enable Register at offset 0x0C is implemented for bit [6:1] corresponding to VCI_IN[6:1]#. There is no input enable implemented for VCI_IN0#. The datasheet lists VCI Input Enable Register as IE[6:0] Input Enables for VCI_INx# signals. However IE[0] bit in the register is "Reserved" and does not have any functionality associated with it. VCI_IN0# is designed to work regardless of brownout condition on coin cell.

11. Module: VCI_OVRD_IN pin does not have input buffer control

DESCRIPTION

Since VCI_OVRD_IN is a dedicated pin and needs to work even in VBAT Brownout condition, therefore there is no input buffer control implemented for VCI_OVRD_IN pin

12. Module: WDT Control Register bit 2 HIBERNATION_TIMER_STALL definition is corrected

DESCRIPTION

In Section 20.7.2 in Datasheet, WDT Control Register bit 2 HIBERNATION_TIMER_STALL definition is updated. Correct definition is given below

HIBERNATION_TIMER_STALL

This bit enables the WDT Stall function if the Hibernation Timer 0 is active.

1=The WDT is stalled while the Hibernation Timer 0 is active

0=The WDT is not affected by Hibernation Timer 0

13. Module: TABLE 57-19: "SPI SETUP AND HOLD TIMES PARAMETERS" values are incorrect in datasheet

DESCRIPTION

TABLE 57-19: "SPI SETUP AND HOLD TIMES PARAMETERS" values are not updated in datasheet. The correct values are given in the table below

TABLE 57-18: SPI CLOCK TIMING PARAMETERS

Name	Description	MIN	TYP	MAX	Units
Tr	SPI Clock Rise Time. Measured from 10% to 90%.			3	ns
Tf	SPI Clock Fall Time. Measured from 90% to 10%.			3	ns
Th/Tl	SPI Clock High Time/SPI Clock Low Time	40% of SPCLK Period	50% of SPCLK Period	60% of SPCLK Period	ns
Tp	SPI Clock Period – As selected by SPI Clock Generator Register	10.42		2,656	ns
Note: Test conditions are as follows: output load is C_L=30pF, pin drive strength setting is 4mA and slew rate setting is slow.					

APPENDIX A: DOCUMENT REVISION HISTORY

Revision	Description
DS80000913F (03-08-22)	Added Errata 22. for TRNG block disable.
	Added Data Sheet Clarification 13.
	Added Data Sheet Clarification 12.
	Added Data Sheet Clarification 10. and 11.
DS80000913E (10-27-21)	Added Errata 20. for ADC Channel 15. Added Errata 21. for eSPI Prefetch feature. Added Data Sheet Clarification 9. for Pad protection feature.
DS80000913D (07-26-21)	Added Data Sheet Clarification 8. for least power consumption in heavy sleep EC state.
	Added Errata 19. and Functional Revision C in Table 1 and Table 2.
	Added Errata 18. GPIO230 to GPIO236 are not wake capable.
	Added Errata 17. VCI_IN0# pin has no Schmitt input and any glitch protection.
	Added Errata 16. VCI_IN0# has only falling edge interrupt.
DS80000913C (04-22-21)	Added Data Sheet Clarification 3. for avoiding IO Pads leakage current.
	Added Data Sheet Clarification 4. EC Subsystem Block register programming.
	Added Data Sheet Clarification 5. for Optional CACHE Controller support.
	Added Data Sheet Clarification 6. for Internal SPI Flash.
	Added Data Sheet Clarification 7. for OTP bytes 416-991.
DS80000913B (01-21-21)	Added Data Sheet Clarification 2. for ARM M4F module base address and registers mentioned in Table 3-5. Revision ID changed from 0x82 to 0x00 for Functional Revision A and 0x82 to 0x01 for Functional Revision B in Table 1.
DS80000913A (10-22-20)	Added Errata 14. for ADC Gain Error Correction.
	Added Errata 15. for QMSPI LDMA TX.
	Added MEC1727N-B0-I/SZ and MEC1727N-B0-I/LJ packages.
	Added Errata 5. and removed MEC1723N-P0-I/9Y package.
	Added Errata 4. to 13.
	Initial release.

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