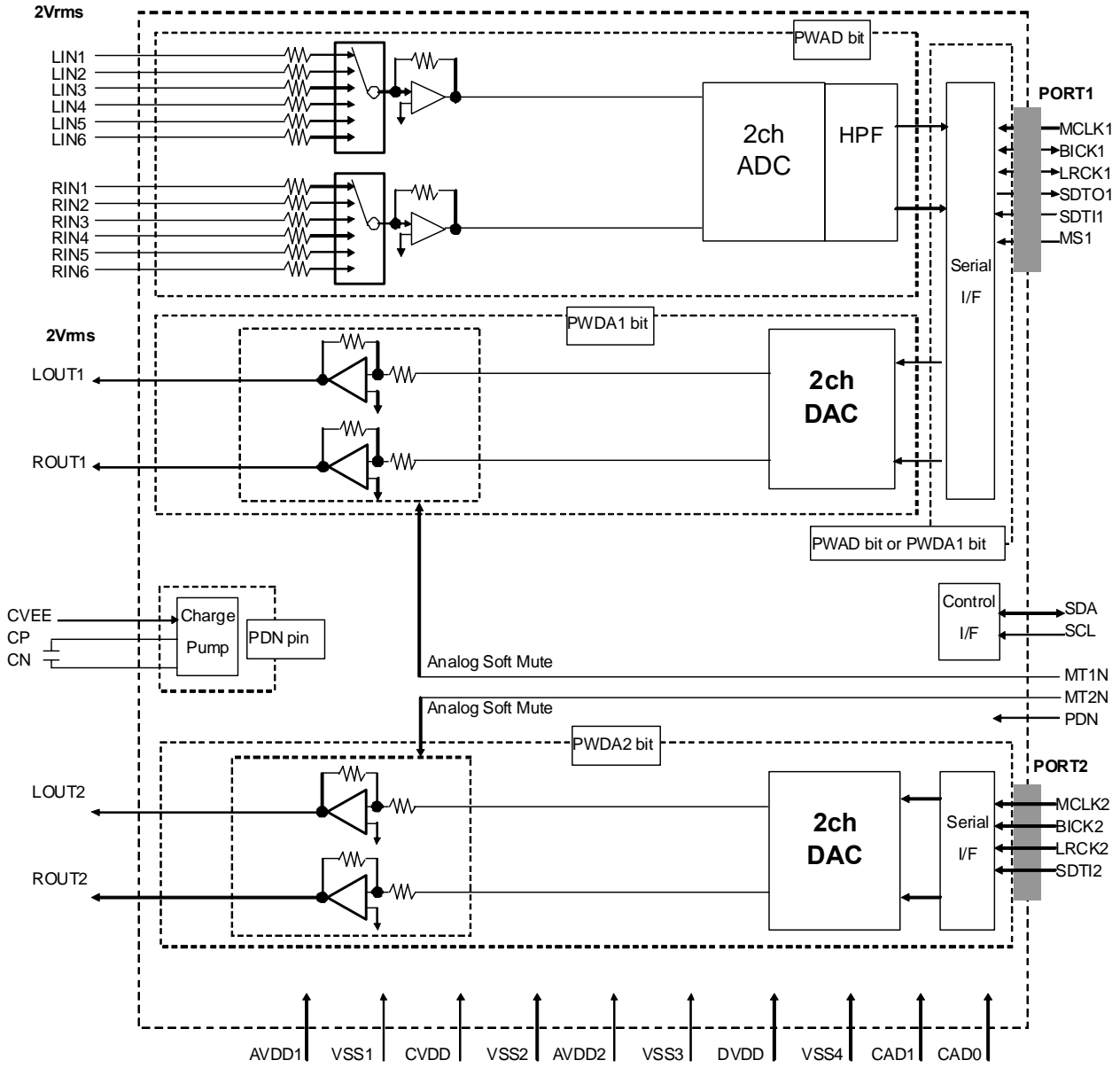# AK4686

Multi-channel CODEC with Capless Stereo Selector

GENERAL DESCRIPTION

The AK4686 is a single chip audio CODEC that includes one stereo ADC and two stereo DACs in addition to the input selector and the line drivers. The interfaces of ADC/DAC can accept up to 24bit input data and support asynchronous operation. Both the input stereo selector and output drivers support ground reference I/O to remove AC-coupling capacitors and reducing external parts. The AK4686 has a dynamic range of 96dB for ADC, 100dB for DAC, and it is well suitable for digital TV and Home theater systems.

FEATURES

☐ Asynchronous Operation between Port 1(ADC and DAC1) and Port 2 (DAC2)
☐ 6:1 Capless Stereo Line Input Selector
☐ 24bit Stereo ADC
- 64x Oversampling
- Sampling Rate up to 48kHz
- Linear Phase Digital Anti-Alias Filter
- S/(N+D): 88dB
- Dynamic Range, S/N: 96dB
- Digital HPF for Offset Cancellation
☐ 24bit Two Stereo DAC
- 128x Oversampling
- Sampling Rate up to 192kHz
- 24bit 8 times Digital Filter
- S/(N+D): 88dB
- Dynamic Range, S/N: 100dB
- De-emphasis Filter
- Analog Soft Mute
☐ High Jitter Tolerance
☐ TTL Level Digital I/F
☐ External Master Clock Input:
        256fs, 384fs, 512fs 768fs (fs=32kHz ~ 48kHz)
        128fs, 192fs, 256fs 384fs (fs=64kHz ~ 96kHz)
        128fs, 192fs (fs=128kHz ~ 192kHz)
☐ 2 Audio Serial I/F (PORT1, PORT2)
- Master/Slave mode (PORT1)
- I/F format
    PORT2: MSB, LSB justified (16/24 bit), I2S
    PORT1: MSB, LSB justified (16/24 bit), I2S
☐ I^{2}C Bus μP I/F for mode setting
☐ Operating Voltage:
- Digital I/O: 3.0V ~ 3.6V
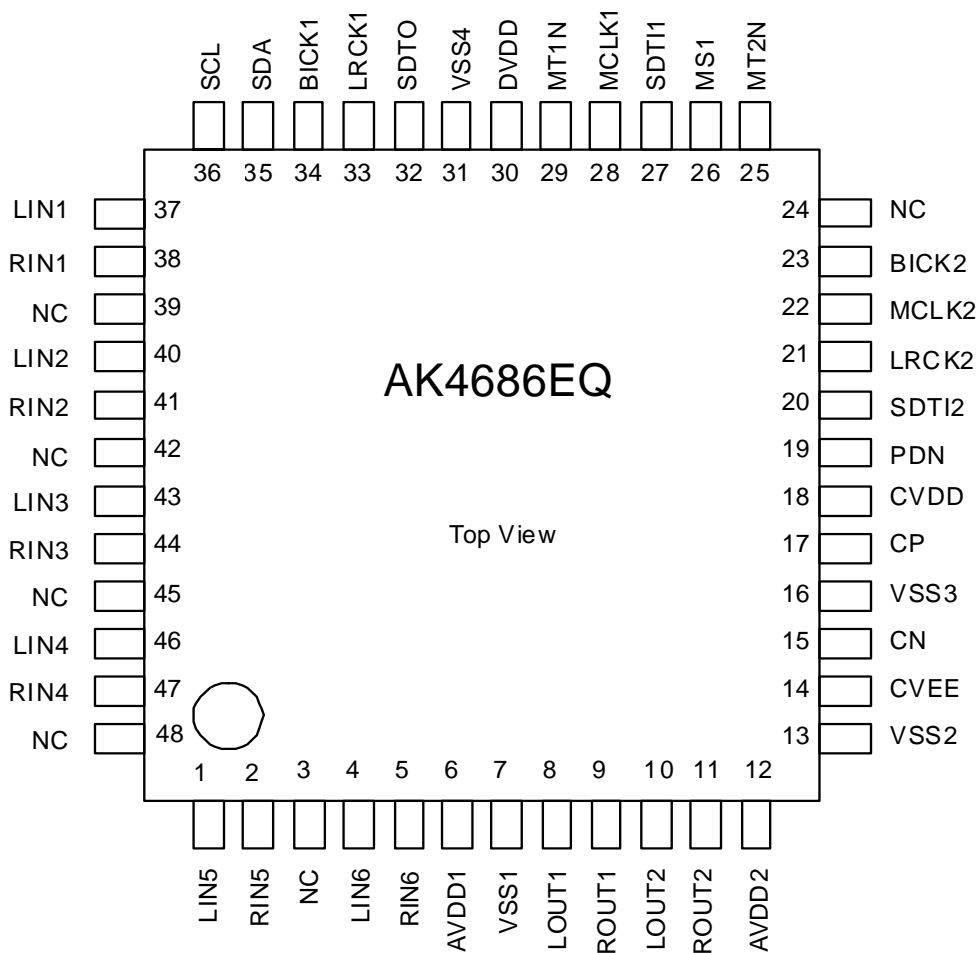- Charge Pump: 3.0V ~ 3.6V
- Analog: 3.0V ~ 3.6V
☐ Package: 48pinLQFP

AK4686 Block Diagram

■ **Ordering Guide**

AK4686EQ   -20 ~ +85°C   48pin LQFP (0.5mm pitch)
AKD4686   Evaluation Board for the AK4686

■ **Pin Layout**

```
                    SCL SDA BICK1 LRCK1 SDTO VSS4 DVDD MT1N MCLK1 SDTI1 MS1 MT2N
                    36  35  34    33    32   31   30   29   28    27    26  25

          LIN1 ┤37                                                    24├ NC
          RIN1 ┤38                                                    23├ BICK2
          NC   ┤39                                                    22├ MCLK2
          LIN2 ┤40                                                    21├ LRCK2
          RIN2 ┤41            AK4686EQ                                 20├ SDTI2
          NC   ┤42                                                    19├ PDN
          LIN3 ┤43                                                    18├ CVDD
          RIN3 ┤44                                                    17├ CP
          NC   ┤45              Top View                              16├ VSS3
          LIN4 ┤46                                                    15├ CN
          RIN4 ┤47                                                    14├ CVEE
          NC   ┤48                                                    13├ VSS2

                     1   2   3   4   5   6   7   8   9  10  11  12
                    LIN5 RIN5 NC LIN6 RIN6 AVDD1 VSS1 LOUT1 ROUT1 LOUT2 ROUT2 AVDD2
```

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	LIN5	I	Lch Input 5 Pin
2	RIN5	I	Rch Input 5 Pin
3	NC	-	This pin must be connected to the ground.
4	LIN6	I	Lch Input 6 Pin
5	RIN6	I	Rch Input 6 Pin
6	AVDD1	-	ADC&DAC1 Analog Power Supply Pin, 3.0V~3.6V
7	VSS1	-	ADC&DAC1 Analog Ground Pin, 0V
8	LOUT1	O	Lch Analog Output Pin1
9	ROUT1	O	Rch Analog Output Pin1
10	LOUT2	O	Lch Analog Output Pin2
11	ROUT2	O	Rch Analog Output Pin2
12	AVDD2	-	DAC2 Analog Power Supply Pin, 3.3V~3.6V
13	VSS2	-	DAC2 Analog Ground Pin, 0V
14	CVEE	O	Charge Pump Circuit Negative Voltage Output Pin (for Analog Input/Output)
15	CN	I	Negative Charge Pump Capacitor Terminal Pin (for Analog Input/Output)
16	VSS3	-	Charge Pump Circuit Analog Ground Pin, 0V (for Analog Input/Output)
17	CP	I	Positive Charge Pump Capacitor Terminal Pin (for Analog Input/Output)
18	CVDD	-	Charge Pump Circuit Positive Power Supply Pin 3.0V~3.6V (for Analog Input/Output)
19	PDN	I	Power-Down Mode & Reset Pin When "L", the AK4686 is powered-down, all registers are reset. And then all digital output pins go "L". The AK4686 must be reset once upon power-up.
20	SDTI2	I	Audio Serial Data Input Pin (for PORT2)
21	LRCK2	I	**Input Channel Clock Pin (for PORT2)**
22	MCLK2	I	DAC2 Master Clock Input Pin (for PORT2)
23	BICK2	I	Audio Serial Data Clock Pin (for PORT2)
24	NC	-	This pin must be connected to the ground.
25	MT2N	I	DAC2 Mute Pin "H": Normal Operation "L": Mute
26	MS1	I	PORT1 Master Mode Select Pin. "L"(connected to the ground): Slave mode. "H"(connected to DVDD) : Master mode.
27	SDTI1	I	Audio Serial Data Input Pin (for PORT1)
28	MCLK1	I	ADC&DAC1 Master Clock Input Pin (for PORT1)
29	MT1N	I	DAC1 Mute Pin "H": Normal Operation "L": Mute
30	DVDD	-	Digital Power Supply Pin, 3.0V~3.6V
31	VSS4	-	Digital Ground Pin, 0V
32	SDTO	O	Audio Serial Data Output 1 Pin (for PORT1)
33	LRCK1	I/O	Channel Clock 1 Pin (for PORT1)
34	BICK1	I/O	Audio Serial Data Clock 1 Pin (for PORT1)
35	SDA	I/O	Control Data Pin
36	SCL	I	Control Data Clock Pin
37	LIN1	I	Lch Input 1 Pin
38	RIN1	I	Rch Input 1 Pin
39	NC	-	This pin must be connected to the ground.
40	LIN2	I	Lch Input 2 Pin
41	RIN2	I	Rch Input 2 Pin
42	NC	-	This pin must be connected to the ground.

PIN/FUNCTION (Continued)

No.	Pin Name	I/O	Function
43	LIN3	I	Lch Input 3 Pin
44	RIN3	I	Rch Input 3 Pin
45	NC	-	This pin must be connected to the ground.
46	LIN4	I	Lch Input 4 Pin
47	RIN4	I	Rch Input 4 Pin
48	NC	-	This pin must be connected to the ground.

Note: All digital input pins must not be left floating.

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LOUT1-2, ROUT1-2, LIN1-6, RIN1-6	These pins must be open.
Digital	SDTO1, LRCK1(Master), BICK1(Master)	These pins must be open.
	MCLK1-2, LRCK1(Slave), LRCK2, BICK1(Slave), BICK2, SDTI1-2, MS1, CAD0	These pins must be connected to VSS4.
	SDA, SCL, MT1N, MT2N	These pins must be pulled-up to DVDD.
-	NC	These pins should be connected to the ground.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=VSS4 =0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supply	DVDD	-0.3	4.0	V
	AVDD1	-0.3	4.0	V
	AVDD2	-0.3	4.0	V
	CVDD	-0.3	4.0	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Digital Input Voltage (MCLK1-2, PDN, LRCK1-2, BICK1-2, SDTI1-2, SDA, SCL, MS1, CAD0, MT1N and MT2N pins)	VIND	-0.3	DVDD+0.3	V
Analog Input Voltage (LIN1-6, RIN1-6 pins)	VINA	-0.3	AVDD1+0.3	V
Ambient Operating Temperature	Ta	-20	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 1. VSS1, VSS2, VSS3 and VSS4 must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
    Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=VSS4= 0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supply (Note 2)	DVDD	3.0	3.3	3.6	V
	AVDD1	3.0	3.3	3.6	V
	AVDD2	3.0	3.3	3.6	V
	CVDD	3.0	3.3	3.6	V

Note 2. The AVDD1, AVDD2 and CVDD must be the same voltage.
   The voltage difference between DVDD and other voltages (AVDD1, AVDD2 and CVDD) must be less than 0.3V.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD1=AVDD2= CVDD = DVDD= 3.3V; VSS1=VSS2= VSS3=VSS4=0V; fs=48kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement Frequency = 20Hz~ 20kHz at fs=48kHz, 20Hz~40kHz at fs=96kHz; 20Hz~40kHz at fs=192kHz, all blocks are synchronized, unless otherwise specified)

Parameter			min	typ	max	Units
Input Impedance			12	16.4		kΩ
Analog Input (LIN1-6, RIN1-6pin) to ADC Analog Input Characteristics						
Resolution					24	Bits
S/(N+D) (-1dBFS)	fs=48kHz		75	88		dB
DR (-60dBFS)	fs=48kHz, A-weighted		88	96		dB
S/N (input off)	fs=48kHz, A-weighted		88	96		dB
Interchannel Isolation (Note 3)			90	100		dB
Interchannel Gain Mismatch				0	0.6	dB
Gain Drift				50	-	ppm/°C
Input Voltage	AIN= 2.2 x AVDD1/3.3		2	2.2	2.4	Vrms
Power Supply Rejection (Note 4)				50		dB
DAC to Analog Output (LOUT1-2, ROUT1-2 pin) Characteristics						
Resolution					24	Bits
S/(N+D) (0dBFS)	fs=48kHz		76	88		dB
	fs=96kHz		-	84		dB
	fs=192kHz		-	84		dB
DR (-60dBFS)	fs=48kHz, A-weighted		94	100		dB
	fs=96kHz		-	96		dB
	fs=96kHz, A-weighted		-	100		dB
	fs=192kHz		-	96		dB
	fs=192kHz, A-weighted		-	100		dB
S/N ("0" data)	fs=48kHz, A-weighted		94	100		dB
	fs=96kHz		-	96		dB
	fs=96kHz, A-weighted		-	100		dB
	fs=192kHz		-	96		dB
	fs=192kHz, A-weighted		-	100		dB
Interchannel Isolation			90	100		dB
Interchannel Gain Mismatch				0	0.5	dB
Gain Drift				50	-	ppm/°C
Output Voltage	AOUT= 2 x AVDD1(AVDD2)/3.3		1.90	2	2.15	Vrms
Load Resistance	(AC Load)		5			kΩ
Load Capacitance	(C1)				30	pF
Load Resistance	(R1)		446.5	470		Ω
Load Capacitance	(C2)			1	1.5	nF
Power Supply Rejection	(Note 4)			50		dB

Note 3. This value is the channel isolation for all other channels when inputting full scale signal to one channel.
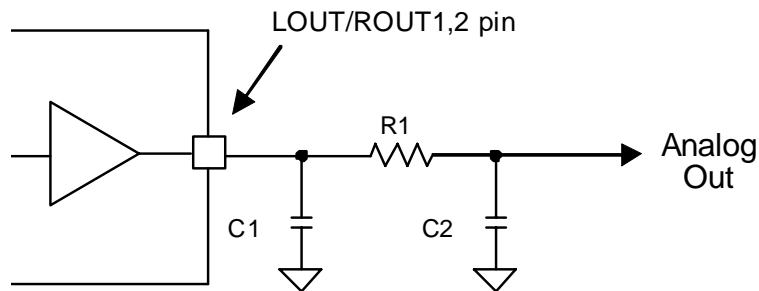Note 4. PSR is applied to AVDD1, AVDD2, DVDD and CVDD with 1kHz, 50mVpp.

Figure 1. Lineout Circuit Example

Power Supplies				
Parameter	**min**	**typ**	**max**	**Units**
Power Supply Current				
Normal Operation (PDN pin = "H")				
DVDD+AVDD1+AVDD2		26	34	mA
CVDD		8	13	mA
Power-Down Mode (PDN pin = "L"; Note 5)				
DVDD+AVDD1+AVDD2+CVDD		10	100	µA

Note 5. All digital inputs including clock pins (MCLK1-2, BICK1-2, LRCK1-2 and SDTI1-2) are held at DVDD or VSS4.

FILTER CHARACTERISTICS

(Ta=-20°C ~+85°C; AVDD1=AVDD2= CVDD = DVDD= 3.3V; fs=48kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 6)	±0.1dB	PB	0		18.5	kHz
	-0.2dB		-	19.9	-	kHz
	-3.0dB		-	22.9	-	kHz
Stopband		SB	27.9			kHz
Stopband Attenuation		SA	61			dB
Group Delay (Note 7)		GD		15.7		1/fs
Group Delay Distortion		ΔGD		0		µs
ADC Digital Filter (HPF):						
Frequency Response (Note 6)	-3dB	FR		1.0		Hz
	-0.1dB			6.5		Hz
DAC Digital Filter:						
Passband (Note 6)	-0.1dB	PB	0		21.8	kHz
	-6.0dB		-	24.0	-	kHz
Stopband		SB	26.2			kHz
Passband Ripple		PR			±0.02	dB
Stopband Attenuation		SA	54			dB
Group Delay (Note 7)		GD		19		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response: 0 ~ 20.0kHz		FR		±0.2		dB
40.0kHz (Note 8)		FR		±0.3		dB
80.0kHz (Note 8)		FR		±1.0		dB

Note 6. The passband and stopband frequencies scale with fs.
    For example, 21.8kHz at –0.1dB is 0.454 x fs (DAC). The reference frequency of these responses is 1kHz.
Note 7. The calculating delay time occurred at digital filtering. This time is from setting the input of analog signal to setting the 24bit data of both channels to the output register of PORT1.
    For DAC, this time is from setting the 20/24bit data of both channels on input register of PORT2 to the output of analog signal.
Note 8. 40.0kHz@fs=96kHz, 80.0kHz@fs=192kHz.

DC CHARACTERISTICS

(Ta=-20°C ~+85°C; AVDD1=AVDD2=CVDD = DVDD= 3.3V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
High-Level Output Voltage (Iout=-400μA)	VOH	DVDD-0.4	-	-	V
Low-Level Output Voltage	VOL	-		0.4	V
(Iout= -400μA(except SDA pin), 3mA(SDA pin))					
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=-20°C ~+85°C; AVDD1=AVDD2=CVDD = DVDD= 3.3V; C_L= 20pF (except for SDA pin), Cb=400pF(SDA pin))

Parameter	Symbol	min	typ	max	Units
Master Clock Timing					
Frequency	fECLK	8.192		36.864	MHz
Duty	dECLK	40	50	60	%
Master Clock					
256fsn, 128fsd:	fCLK	8.192		12.288	MHz
Pulse Width Low	tCLKL	27			ns
Pulse Width High	tCLKH	27			ns
384fsn, 192fsd:	fCLK	12.288		18.432	MHz
Pulse Width Low	tCLKL	20			ns
Pulse Width High	tCLKH	20			ns
512fsn, 256fsd, 128fsq:	fCLK	16.384		24.576	MHz
Pulse Width Low	tCLKL	15			ns
Pulse Width High	tCLKH	15			ns
768fsn, 384fsd, 192fsq:	fCLK	24.576		36.864	MHz
Pulse Width Low	tCLKL	10			ns
Pulse Width High	tCLKH	10			ns
LRCK1/2Timing (Slave Mode)					
Normal mode					
Normal Speed Mode	fsn	32		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty	45		55	%
LRCK1 Timing (Master Mode)					
Normal mode					
Normal Speed Mode	fsn	32		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty		50		%
Power-down & Reset Timing					
PDN Pulse Width (Note 9)	tPD	150			ns
PDN "↑" to SDTO1 valid (Note 10)	tPDV		296		1/fs

Note 9. The AK4686 can be reset by bringing the PDN pin = "L".
Note 10. After a rising edge of PDN, the internal counter starts by divided clock of MCLK and ADC power down is
      released by a falling edge of CVEE after 256/fs on LRCK, then SDTO1 is output 40/fs later.

Parameter	Symbol	min	typ	max	Units
Audio Interface Timing (Slave Mode)					
PORT1(DAC1), PORT2 (DAC2)					
BICK1, 2 Period	tBCK	81			ns
BICK1, 2 Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCK1, 2 Edge to BICK1, 2 "↑" (Note 11)	tLRB	20			ns
BICK1, 2 "↑" to LRCK1, 2 Edge (Note 11)	tBLR	20			ns
SDTI1, 2 Hold Time	tSDH	10			ns
SDTI1, 2 Setup Time	tSDS	10			ns
PORT1 (ADC)					
BICK1 Period	tBCK	324			ns
BICK1 Pulse Width Low	tBCKL	128			ns
Pulse Width High	tBCKH	128			ns
LRCK1 Edge to BICK1 "↑" (Note 11)	tLRB	80			ns
BICK1 "↑" to LRCK1 Edge (Note 11)	tBLR	80			ns
LRCK1 to SDTO1 (MSB)	tLRS			80	ns
BICK1 "↓" to SDTO1	tBSD			80	ns
Audio Interface Timing (Master Mode)					
BICK1 Frequency	fBCK		64fs		Hz
BICK1 Duty	dBCK		50		%
BICK1 "↓" to LRCK1 Edge	tMBLR	-20		20	ns
BICK1 "↓" to SDTO1	tBSD			20	ns
SDTI1 Hold Time	tSDH	25			ns
SDTI1 Setup Time	tSDS	10			ns
Control Interface Timing (I²C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	μs
Start Condition Hold Time	tHD:STA	0.6		-	μs
(prior to first clock pulse)					
Clock Low Time	tLOW	1.3		-	μs
Clock High Time	tHIGH	0.6		-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	μs
SDA Hold Time from SCL Falling (Note 12)	tHD:DAT	0		-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	μs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6		-	μs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	-		50	ns
Capacitive load on bus	Cb	0		400	pF

Note 11. BICK rising edge must not occur at the same time as LRCK edge.
Note 12. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 13. I²C-bus is a trademark of NXP B.V.

■ Timing Diagram

Clock Timing (Normal mode)

Audio Interface Timing
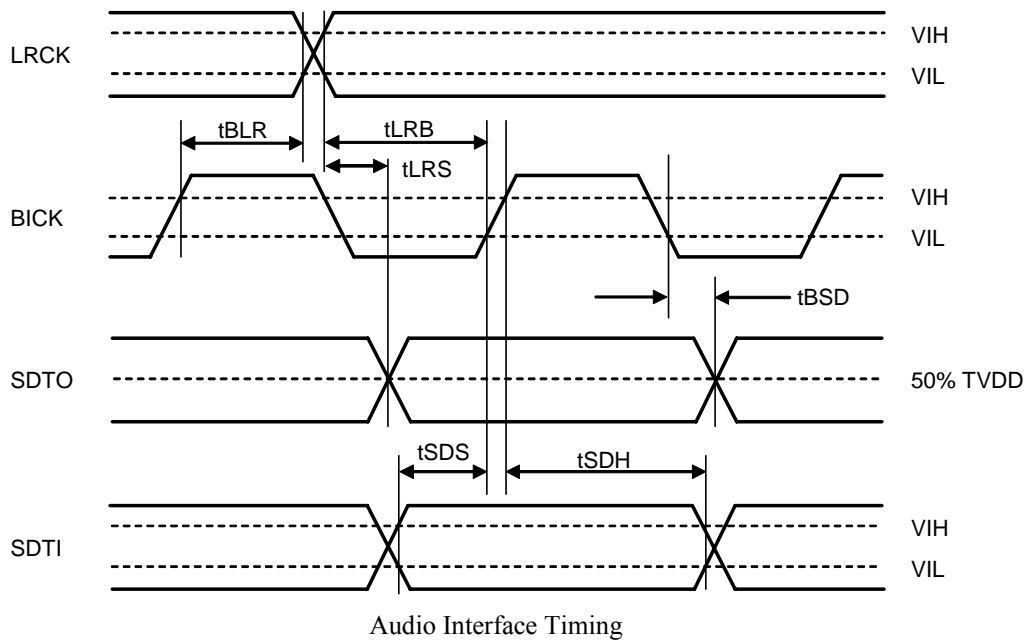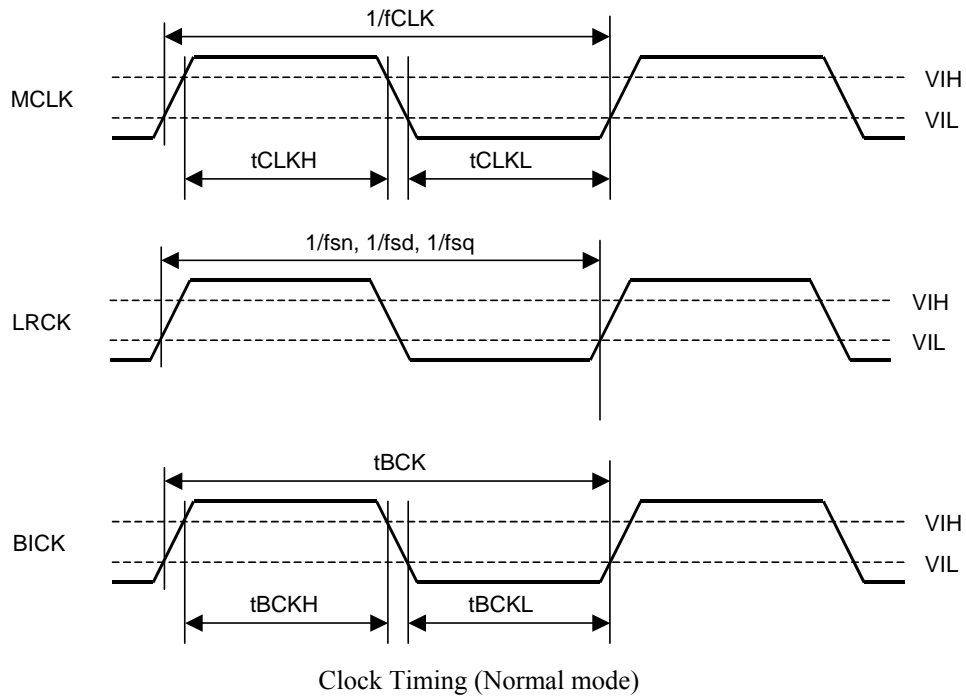
LRCK= LRCK1, LRCK2
BICK= BICK1, BICK2
SDTI= SDTI1/2
SDTO= SDTO1.
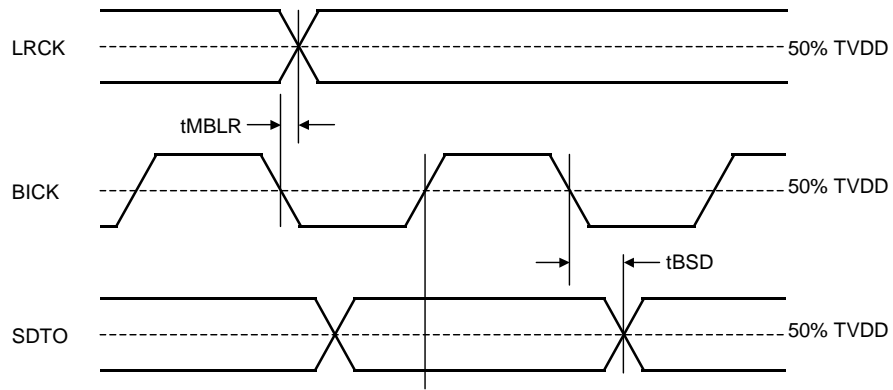
Audio Interface timing (Master Mode)
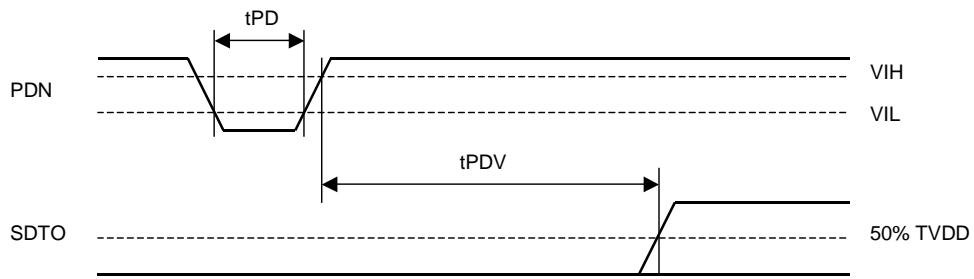
Power Down & Reset Timing
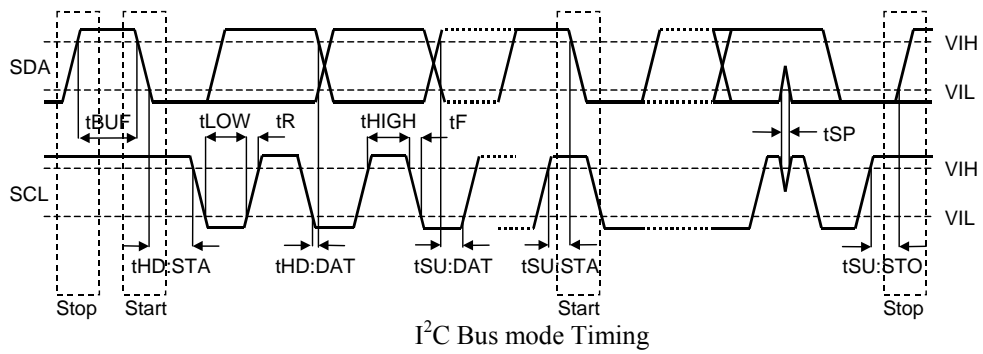
I^{2}C Bus mode Timing

<div style="text-align: center;">**OPERATION OVERVIEW**</div>

■ System Clock

The AK4686 has two audio serial interfaces (PORT1 and PORT2) which can be operated asynchronously. At each PORT, the external clocks, which are required to operate the AK4686, are MCLK1 (MCLK2), LRCK1 (LRCK2) and BICK1 (BICK2). The MCLK1 (MCLK2) must be synchronized with LRCK1 (LRCK2) but the phase is not critical. The PORT2 is an audio data interfaces for DAC2, the PORT1 is for ADC and DAC1.

The AK4686 is automatically powered down, then the ADC output becomes "0" data and DAC output is pulled down (VSS) when MCLK1 (MCLK2) is stopped more than 2μs or BICK1 or LRCK1 (BICK2 or LRCK2) are stopped more than 1024*MCLK cycles during an operation (PDN pin = "H"). The power down state is released when MCLK1, BICK1 and LRCK1 (MCLK2, BICK2 and LRCK2) are input and the AK4686 starts an operation. When reset is released (PDN pin = "L" → "H"), such as when power up the device, the AK4686 is in power down state until MCLK1 (MCLK2) is input.

The AK4686 is reset automatically and the phase is synchronized by a phase detection circuit when internal timings are unsynchronized by clock change during an operation.

■ Master/Slave Mode

The MS1 pin controls master/slave mode of the PORT1. The PORT2 supports slave mode only. In master mode, LRCK1 pin and BICK1 pin are output pins. In slave mode, LRCK1, LRCK2 pins and BICK1, BICK2 pins are input pins (Table 1).

PDN pin	MS1 pin	PORT1 (ADC, DAC1) BICK1, LRCK1	PORT2 (DAC2) BICK2, LRCK2
L	L	Input (slave mode)	Input (slave mode)
	H	Output "L"(master mode)	Input (slave mode)

<div style="text-align: center;">Table 1. Master/Salve Mode</div>

■ PORT1 (ADC, DAC1) Clock Control

In master mode (MS1 pin = "H"), the CKS12-0 bits select the clock frequency (Table 2). The external clock (MCLK1) must always be supplied except in power-down mode (PDN pin = "L" or PWAD bit, PWDA1 bit = "0"). The ADC is in power-down mode until MCLK1 is supplied.

CKS12	CKS11	CKS10	Sampling Speed (fs)		Master Clock Speed	
0	0	0	Normal or Double	32kHz~48kHz, 64kHz~96kHz	256fs	(default)
0	0	1	Normal or Double	32kHz~48kHz, 64kHz~96kHz	384fs	
0	1	0	Normal	32kHz~48kHz	512fs	
0	1	1	Normal	32kHz~48kHz	768fs	
1	0	0	Double or Quad	64kHz~96kHz, 128kHz~192kHz	128fs	
1	0	1	Double or Quad	64kHz~96kHz, 128kHz~192kHz	192fs	
1	1	X	X		N/A	

Table 2. PORT1(ADC, DAC1) Master Clock Control (Master Mode)

In slave mode (MS1 pin = "L"), external clocks (MCLK1, BICK1, LRCK1) must always be present whenever the ADC is in normal operation mode (PDN pin = "H" or PWAD bit = PWDA1 bit = "1"). The master clock (MCLK1) must be synchronized with LRCK1 but the phase is not critical. If these clocks are not provided, the ADC may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC and DAC1 must be in power-down mode (PDN pin = "L" or PWAD bit = PWDA1 bit = "0") or in reset mode (RSTN bit = "0"). After exiting reset at power-up and etc., ADC is in power-down mode until MCLK1 and LRCK1 are input.

There are two modes for controlling the sampling speed of ADC and DAC1. One is Manual Setting Mode (ACKS1 bit = "0") using the DFS11-10 bits, and the other is Auto Setting Mode (ACKS1 bit = "1"). The ADC only supports Normal Speed Mode, and it is powered-down in Double Speed Mode and Quad Speed Mode.

1. Manual Setting Mode (ACKS1 bit = "0")
When the ACKS1 bit = "0", ADC and DAC1 is in Manual Setting Mode and the sampling speed is selected by DFS11-10 bits (Table 3).

DFS11	DFS10	ADC Sampling Speed (fs)		DAC1 Sampling Speed (fs)		
0	0	Normal Speed Mode	32kHz~48kHz	Normal Speed Mode	32kHz~48kHz	(default)
0	1	Power down		Double Speed Mode	64kHz~96kHz	
1	0	Power down		Quad Speed Mode	128kHz~192kHz	
1	1	Not Available				

Table 3. PORT1(ADC, DAC1) Sampling Speed (ACKS1bit = "0", Manual Setting Mode)

LRCK1	MCLK1 (MHz)				BICK1 (MHz)
fs	256fs	384fs	512fs	768fs	64fs
32.0kHz	8.1920	12.2880	16.3840	24.5760	2.0480
44.1kHz	11.2896	16.9344	22.5792	33.8688	2.8224
48.0kHz	12.2880	18.4320	24.5760	36.8640	3.0720

Table 4. ADC, DAC1 System Clock Example (ADC, DAC1 Normal Speed Mode @Manual Setting Mode)

LRCK1	MCLK1 (MHz)				BICK1 (MHz)
fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	11.2896	16.9344	22.5792	33.8688	5.6448
96.0kHz	12.2880	18.4320	24.5760	36.8640	6.1440

Table 5. DAC1 System Clock Example (DAC1 Double Speed Mode @Manual Setting Mode)

LRCK1	MCLK1 (MHz)				BICK1 (MHz)
fs	128fs	192fs	256fs	384fs	64fs
176.4kHz	22.5792	33.8688	-	-	11.2896
192.0kHz	24.5760	36.8640	-	-	12.2880

Table 6. DAC1 System Clock Example (DAC1 Quad Speed Mode @Manual Setting Mode)

2. Auto Setting Mode (ACKS1 bit = "1")

When the ACKS1 bit = "1", ADC and DAC1 are in Auto Setting Mode and the sampling speed is selected automatically by the ratio of MCLK1/LRCK1, as shown in the Table 7 and the internal master clock is set to the appropriate frequency (Table 8). The ADC only supports Normal Speed Mode, and it is powered-down in Double Speed Mode and Quad Speed Mode. In this mode, the settings of DFS11-10 bits are ignored. (Table 5, Table 6)

MCLK1	LRCK1	ADC Sampling Speed	DAC Sampling Speed
512fs, 768fs	32kHz~48kHz	Normal Speed Mode	Normal Speed Mode
256fs, 384fs	64kHz~96kHz	Power down	Double Speed Mode
128fs, 192fs	120kHz~192kHz	Power down	Quad Speed Mode

Table 7. PORT1(ADC,DAC1) Sampling Speed (ACKS1 bit = "1", Auto Setting Mode)

LRCK1	MCLK1 (MHz)						ADC Sampling Speed	DAC1 Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs		
32.0kHz	-	-	-	-	16.3840	24.5760	Normal	Normal
44.1kHz	-	-	-	-	22.5792	33.8688		
48.0kHz	-	-	-	-	24.5760	36.8640		
88.2kHz	-	-	22.5792	33.8688	-	-	Power down	Double
96.0kHz	-	-	24.5760	36.8640	-	-		
176.4kHz	22.5792	33.8688	-	-	-	-	Power down	Quad
192.0kHz	24.5760	36.8640	-	-	-	-		

Table 8. PORT1 (ADC, DAC1) System Clock Example (Auto Setting Mode)

■ **PORT2 (DAC2) Clock Control**

External clocks (MCLK2, BICK2 and LRCK2) must always be present whenever the DAC is in normal operation mode (PDN pin = "H" or PWDA2 bit= "1"). The master clock MCLK2 must be synchronized with LRCK2 but the phase is not critical. If these clocks are not provided, the DAC may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the DAC must be in power-down mode (PDN pin = "L" or PWDA2 bit = "0") or in reset mode (RSTN bit = "0"). After exiting reset at power-up and etc., the DAC is in power-down mode until MCLK2 and LRCK2 are input.

There are two modes for controlling the sampling speed of DAC2. One is the Manual Setting Mode (ACKS2 bit = "0") using the DFS21-20 bits, and the other is Auto Setting Mode (ACKS2 bit = "1").

1. Manual Setting Mode (ACKS2 bit = "0")
When the ACKS2 bit = "0", DAC2 is in Manual Setting Mode and the sampling speed is selected by DFS21-20 bits (Table 9).

DFS21	DFS20	DAC2 Sampling Speed (fs)	
0	0	Normal Speed Mode	32kHz~48kHz
0	1	Double Speed Mode	64kHz~96kHz
1	0	Quad Speed Mode	128kHz~192kHz
1	1	Not Available	-

(default)

Table 9. PORT2(DAC2) Sampling Speed (ACKS2 bit = "0", Manual Setting Mode)

LRCK2	MCLK2 (MHz)				BICK2 (MHz)
fs	256fs	384fs	512fs	768fs	64fs
32.0kHz	8.1920	12.2880	16.3840	24.5760	2.0480
44.1kHz	11.2896	16.9344	22.5792	33.8688	2.8224
48.0kHz	12.2880	18.4320	24.5760	36.8640	3.0720

Table 10. DAC2 System Clock Example (DAC Normal Speed Mode @Manual Setting Mode)

LRCK2	MCLK2 (MHz)				BICK2 (MHz)
fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	11.2896	16.9344	22.5792	33.8688	5.6448
96.0kHz	12.2880	18.4320	24.5760	36.8640	6.1440

Table 11. DAC2 System Clock Example (DAC Double Speed Mode @Manual Setting Mode)

LRCK2	MCLK2 (MHz)				BICK2 (MHz)
Fs	128fs	192fs	256fs	384fs	64fs
176.4kHz	22.5792	33.8688	-	-	11.2896
192.0kHz	24.5760	36.8640	-	-	12.2880

Table 12. DAC2 System Clock Example (DAC Quad Speed Mode @Manual Setting Mode)

2. Auto Setting Mode (ACKS2 bit = "1")

When the ACKS2 bit = "1", DAC2 is in Auto Setting Mode and the sampling speed is selected automatically by the ratio of MCLK2/LRCK2, as shown in the Table 13 and the internal master clock is set to the appropriate frequency (Table 14). In this mode, the settings of DFS1-0 bits are ignored.

MCLK2	DAC Sampling Speed (fs) LRCK2	
512fs, 768fs	Normal Speed Mode	32kHz~48kHz
256fs, 384fs	Double Speed Mode	64kHz~96kHz
128fs, 192fs	Quad Speed Mode	128kHz~192kHz

Table 13. PORT2(DAC2) Sampling Speed (ACKS2 bit = "1", Auto Setting Mode)

LRCK2	MCLK2 (MHz)						Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	
32.0kHz	-	-	-	-	16.3840	24.5760	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	
48.0kHz	-	-	-	-	24.5760	36.8640	
88.2kHz	-	-	22.5792	33.8688	-	-	Double
96.0kHz	-	-	24.5760	36.8640	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	Quad
192.0kHz	24.5760	36.8640	-	-	-	-	

Table 14. PORT2 (DAC2) System Clock Example (Auto Setting Mode)

■ **De-emphasis Filter**

The AK4686 includes a digital de-emphasis filter (tc=50/15μs) by IIR filter. This filter corresponds to three sampling frequencies (32kHz, 44.1kHz, 48kHz). De-emphasis filter is off in Double speed mode and Quad speed mode. De-emphasis of each DAC can be set individually by registers.

Mode	DEM11 (DEM21)	DEM10 (DEM20)	DEM	
0	0	0	44.1kHz	
1	0	1	OFF	(default)
2	1	0	48kHz	
3	1	1	32kHz	

Table 15. De-emphasis Control

■ **ADC Digital High Pass Filter**

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz at fs=48kHz and scales with sampling rate (fs).

■ **Audio Serial Interface Format**

Each PORT1/2 can select independent audio interface format. The DIF11-10 bits control the audio format for PORT1. The DIF21-20 bits control the audio format for PORT2. In all modes the serial data is MSB-first, 2's complement format. The SDTO1 pin is clocked out on the falling edge of BICK1 pin and the SDTI1-2 pins are latched on the rising edge of BICK1-2 pins.

1. PORT1(ADC,DAC1) Setting

The MS1 pin and DIF11-10 bits select following four serial data formats (Table 16).

Mode	MS1 pin	DIF11 bit	DIF10 bit	SDTO	SDTI1	LRCK1		BICK1		
						L/R	I/O	speed	I/O	
0	0	0	0	24/16bit, L J	16bit, R J	H/L	I	≥ 48fs or 32fs	I	
1	0	0	1	24bit, L J	24bit, R J	H/L	I	≥ 48fs	I	
2	0	1	0	24bit, L J	24bit, L J	H/L	I	≥ 48fs	I	
3	0	1	1	24bit, I^2S	24bit, I^2S	L/H	I	≥ 48fs	I	(default)
4	1	0	0	24bit, L J	16bit, R J	H/L	O	64fs	O	
5	1	0	1	24bit, L J	24bit, R J	H/L	O	64fs	O	
6	1	1	0	24bit, L J	24bit, L J	H/L	O	64fs	O	
7	1	1	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	(default)

Table 16. Audio Interface Format (Normal mode, x: Don't care, L J: Left justified, R J: Right justified.)

2. PORT2(DAC2) Setting

The DIF21-20 bits select following four serial data formats (Table 17).

Mode	DIF21 bit	DIF20 bit	SDTI2	LRCK2		BICK2		
				L/R	I/O	speed	I/O	
0	0	0	16bit, Right justified	H/L	I	≥ 48fs or 32fs	I	
1	0	1	24bit, Right justified	H/L	I	≥ 48fs	I	
2	1	0	24bit, Left justified	H/L	I	≥ 48fs	I	
3	1	1	24bit, I^2S	L/H	I	≥ 48fs	I	(default)

Table 17. Audio Interface Format
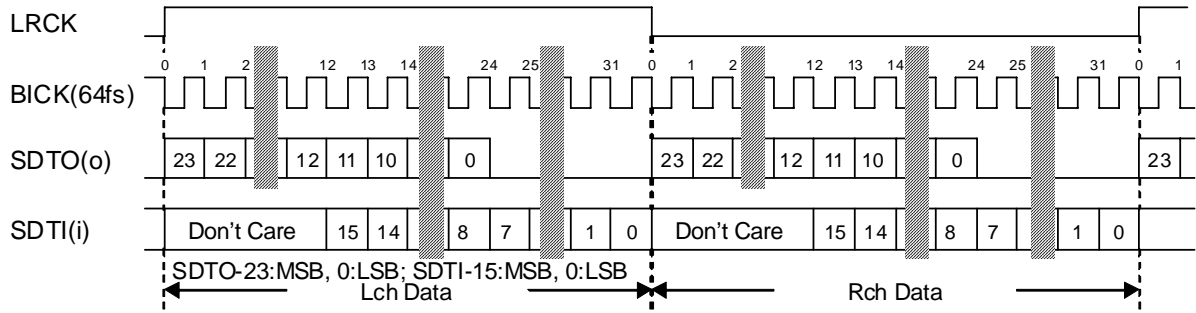
Figure 2. Mode 0/4 Timing
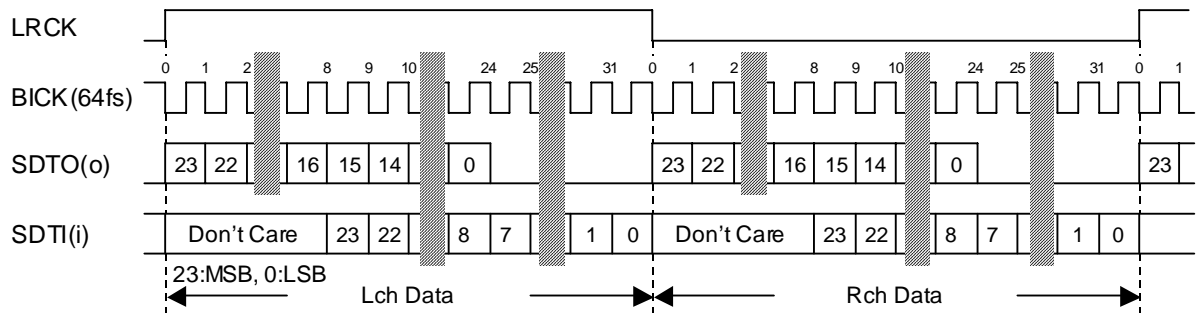
Figure 3. Mode 1/5 Timing
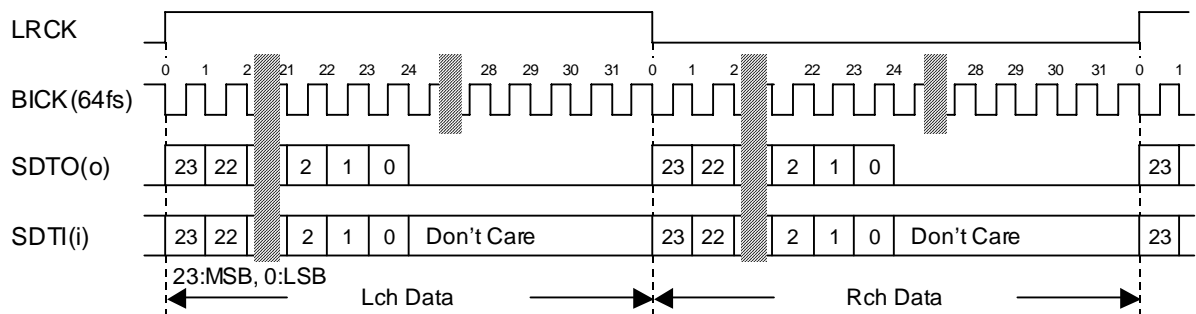
Figure 4. Mode 2/6 Timing
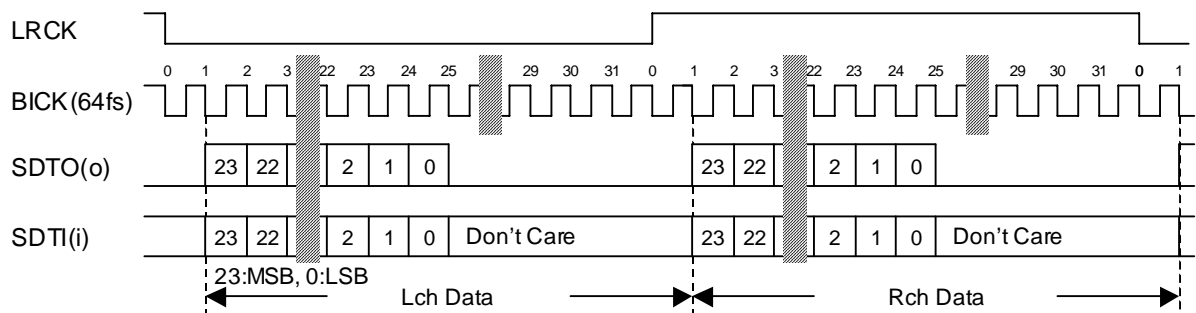
Figure 5. Mode 3/7 Timing

■ Analog Soft Mute Function

LOUT1, ROUT1/LOUT2, ROUT2 are muted in soft transition when the MT1N/2N pins are set to "L" from "H". After the soft mute transition is finished, the DAC and Lineout are in powered-down mode and output ground level voltage (VSS1/VSS3). The transition time is set by AMTS1-0 bits. Clocks and data must always be supplied until soft mute transition is finished. The DAC and Lineout return to a normal operation and start digital to analog conversion when the MT1N/2N pins are set to "H". Mute is cancelled in soft transition after initializing time of DAC. When the MT1N/2N pin = "L" or MT1N/2N bit = "0", LOUT1, ROUT1/LOUT2, ROUT2 are muted.
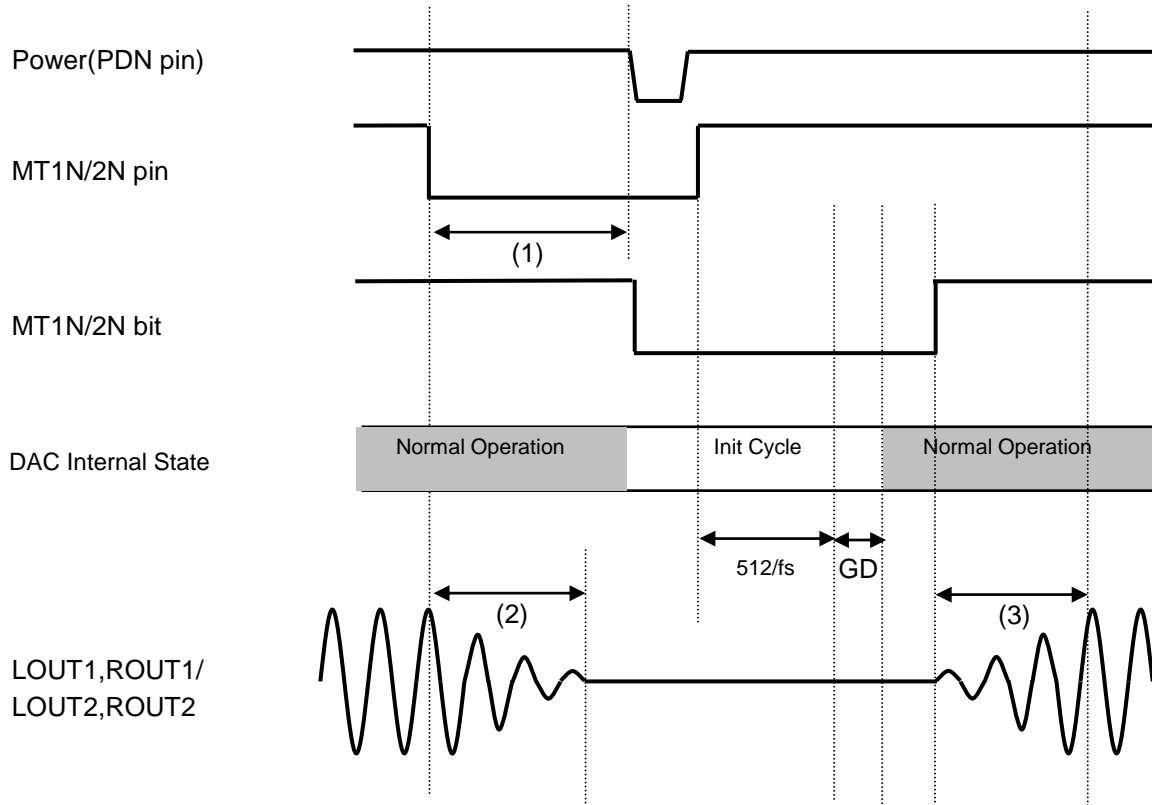
(1) Click noise may occur if each power supply (DVDD, AVDD1/2 and CVDD) is OFF during mute period. Power supplies should be ON longer than the soft mute time set by AMTS1-0 bits.
(2) Soft mute time is set by AMTS1-0 bits (2).
(3) Soft mute time is set by AMTS1-0 bits (3).

Figure 6. Mute Sequence Example

AMTS2	AMTS1	AMTS0	Soft Mute Time (fs=48kHz)			
			(2)		(3)	
			MT1N/2N pin	MT1N/2N bit	MT1N/2N	
0	0	0	16ms	16ms	16ms	
0	0	1	32ms	32ms	32ms	(default)
0	1	0	64ms	64ms	64ms	
0	1	1	128ms	128ms	128ms	
1	0	0	256ms	256ms	256ms	
1	0	1	8ms	16ms	16ms	
1	1	X	2ms	16ms	16ms	

(X: Don't care)
Table 18. Soft Mute Time Select (@48kHz)
When AMTS2-0 bits = "101" or "11X", the soft mute time by MT1N/2N pin and by MT1N/2N bit are different.

■ **Input Selector**

The AK4686 has 6:1 stereo input selectors. ATIN3-0 bits control each input channel. (Table 19)

AIN3 bit	AIN2 bit	AIN1 bit	AIN0 bit	Input Selector	
0	0	0	0	LIN1 / RIN1	(default)
0	0	0	1	LIN2 / RIN2	
0	0	1	0	LIN3 / RIN3	
0	0	1	1	LIN4 / RIN4	
0	1	0	0	LIN5 / RIN5	
0	1	0	1	LIN6 / RIN6	
0	1	1	0	(reserved)	
0	1	1	1	(reserved)	
1	x	x	x	Mute	

Table 19. Input Selector (for ADC, x: Don't care)

■ Charge Pump Circuit

The internal charge pump circuit generates negative voltage (CVEE) from CVDD voltage for analog input and output.

The power up time of charge pump circuit is 5.3ms@48kHz. When PWAD and PWDA1/2 bits = "1", the ADC and DAC1/2 are powered-up after the charge pump circuit is powered-up.

■ Analog Input/Output (LIN1-6/RIN1-6, LOUT1-2/ROUT1-2 pins)

Power supply voltage for analog input/output is applied from a regulator for positive power and a charge-pump for negative power. The Regulator is driven by AVDD2 and the charge-pump1 is driven by CVDD. The analog input/output is single-ended and centered on 0V (VSS3). Therefore, the capacitor for AC-coupling can be removed. The minimum load resistance is 5kΩ. When the DAC input signal level is 0dBFS, the output voltage is 2Vrms.

■ System Reset

When power-up the AK4686, the PDN pin should be "L" and changed to "H" after all power supplies (DVDD, AVDD1, AVDD2 and CVDD) are supplied. After this reset is released (PDN pin = "L" → "H"), all blocks are in power-down mode. This ensures that all internal registers reset to their initial values.

■ Power ON/OFF Sequence

The each block of the AK4686 is placed in power-down mode by bringing the PDN pin to "L" and both digital filters are reset at the same time. The PDN pin ="L" also reset the control registers to their default values. In power-down mode, the DAC1/2 outputs 0V and the SDTO1 pin goes to "L". This reset must always be executed after power-up.

In slave mode, after exiting reset at power-up and etc., the ADC/DAC1/DAC2 starts operation from the rising edge of LRCK1/2 after MLCK1/2 inputs. The AK4686 is in power-down mode until MCLK1/2 and LRCK1/2 are input.

The analog initialization cycle of ADC starts after exiting the power-down mode. Therefore, the output data, SDTO1 becomes available after 514/fs cycles of LRCK1 clock. In case of the DAC1/2 an analog initialization cycle starts after exiting the power-down mode. The analog outputs are 0V during the initialization. Figure 7 shows the sequences of the power-down and the power-up.

The ADC and all DACs can be powered-down individually by PWAD and PWDA1/2 bits. These bits do not initialize the internal register values. When PWAD bit = "0", the SDTO1 pin goes to "L". When PWDA bit = "0", the DAC1/2 outputs go to 0V. As some click noise occurs, the analog output should be muted externally if the click noise influences system application.
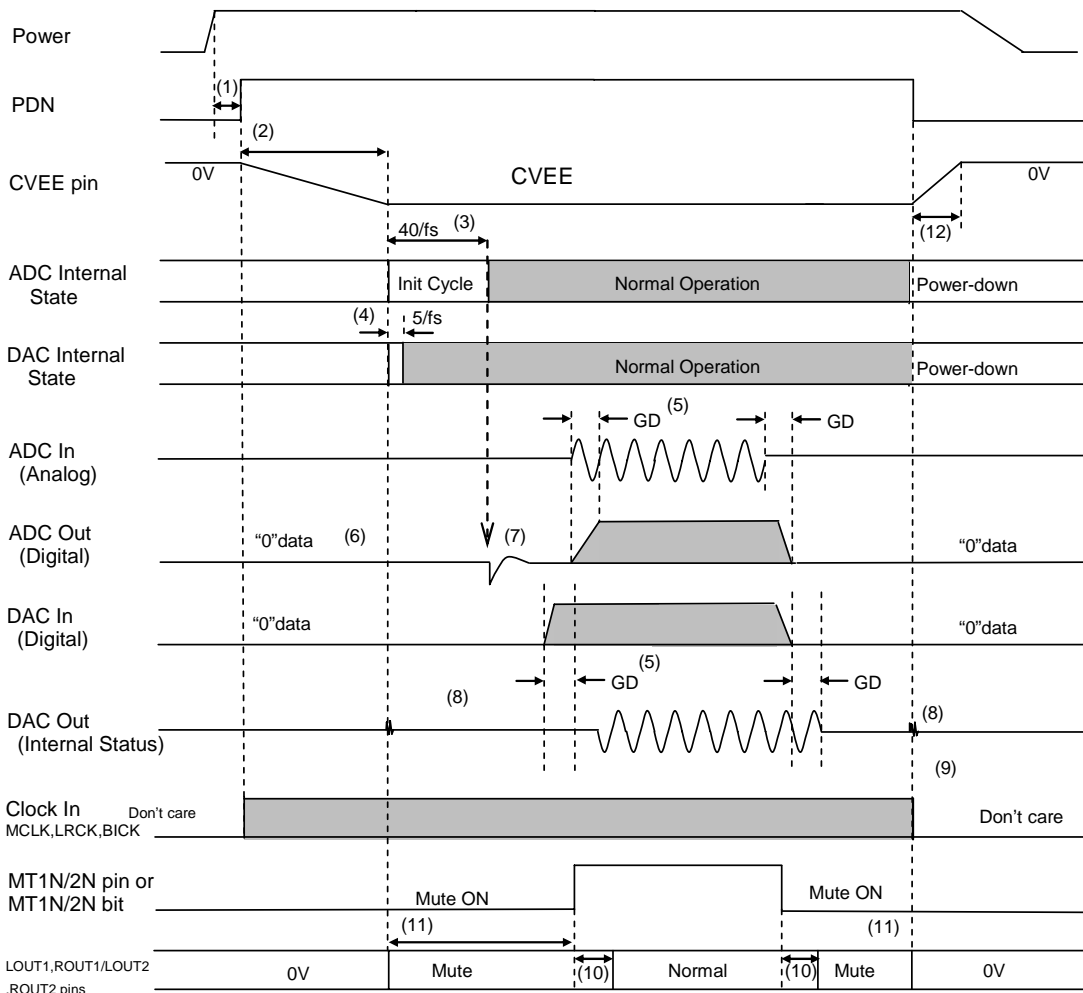
Figure 7. Power-up/down sequence example

Notes:
(1) The timing of the PDN pin "L"➔"H" should be after the all powers (DVDD, AVDD1/2 and CVDD1) are supplied.
The AK4686 requires 150ns or longer "L" period for the reset. Supply the power during the PDN pin = "L".

(2) Power-on the charge pump circuit:
   PDN pin = "L" → "H" & MCLK1 or MCLK2 is input.
   CVEE pin becomes to the same voltage as CVEE1/2 within about 5.3ms(fs=48KHz).
   Note: If the PWAD, PWDA1 and PWDA2 bits are set to "1" when the charge-pump is power-on, ADC, DAC1 and
      DAC2 are initialized after the charge-pump1 circuit is powered-on.
(3) The analog block of ADC is initialized after exiting the power-down state.
(4) The analog block of DAC is initialized after exiting the power-down state.
(5) Digital outputs corresponding to analog inputs and analog outputs corresponding to digital inputs have group delay
   (GD).
(6) ADC outputs "0" data in power-down state.
(7) Click noise occurs at the end of initialization of the analog block. Mute the digital outputs externally if the click
   noise influences system application.
(8) Click noise occurs at the falling edge of PDN and 512/fs after the rising edge(after charge-pump is powered-on) of
   PDN.
(9) The CVEE pin becomes 0V according to the time constant of the capacitor at the CVEE pin and the internal
   resistor. The internal resistor is 17.5kΩ (typ.). Charge Pump Circuit can be powered-up during this period.
(10) AMTS1-0 bits control the soft mute transition time. When releasing the mute, the maximum DC offset is ±20mV
   (at design value). This transition is a soft transition so that no clicking noise occurs.
(11) Maximum 5mV DC offset is generated when power up the lineout circuit. More than **5.3ms(fs=48KHz)+2msec**
   interval (after 2msec from falling edge of CVEE)is needed from a falling edge of PDN signal to a mute release to
   prevent a click noise.
(12) Charge pump circuit power down:
   PDN pin = "H" → "L"
   The CVEE pin becomes 0V according to a flying capacitor and internal resistor. The internal resister is 50kΩ
   (typ). Therefore, when the CVEE pin has a flying capacitor of 2.2μF, the time constant is 110ms (typ).

■ **Reset Function**

When RSTN bit = "0", ADC and DACs are powered-down but the internal register are not initialized. The DAC1/2 outputs become 0V and the SDTO1 pin outputs "L". As some click noise occurs, the analog output should be muted externally if the click noise influences system application. The Figure 8 shows the power-up sequence.
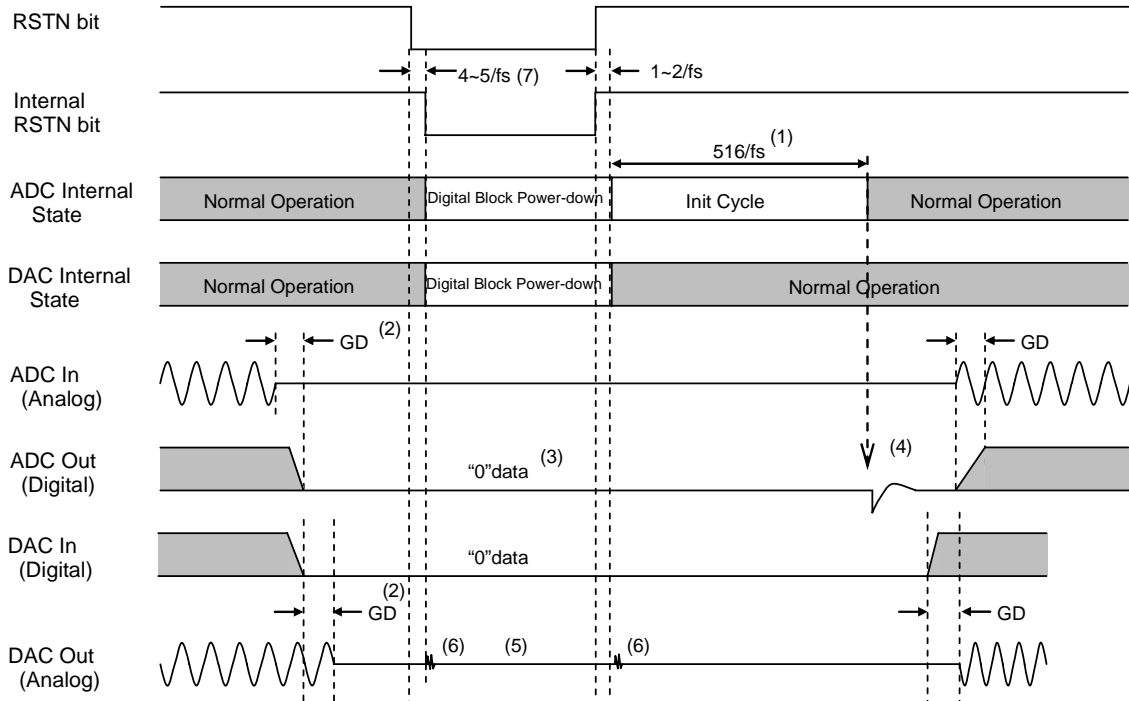
Notes:
(1) The analog block of ADC is initialized after exiting the reset state.
(2) Digital outputs corresponding to analog inputs and analog outputs corresponding to digital inputs have group delay (GD).
(3) ADC outputs "0" data in power-down state.
(4) Click noise occurs at the end of initialization cycle of ADC. Mute the digital output externally if the click noise influences system application.
(5) When RSTN bit = "0", the analog outputs become 0V.
(6) Click noise occurs in 4~5/fs after RSTN bit becomes "0", and occurs in 1~2/fs after RSTN bit becomes "1". This noise is output even if "0" data is input.
(7) There is a delay about 4~5/fs from RSTN bit "0" to the internal RSTN bit "0".

Figure 8. Reset sequence example

■ Serial Control Interface

The AK4686 supports fast-mode I^{2}C-bus system (max: 400kHz).

1. Data Transfer

In order to access any IC devices on the I^{2}C BUS, input a start condition first, followed by a single Slave address which includes the Device Address. IC devices on the BUS compare this Slave address with their own addresses and the IC device which has an identical address with the Slave-address generates an acknowledgement. An IC device with the identical address then executes either a read or write operation. After the command execution, input a stop condition.

1-1. Data Change

Change the data on the SDA line while SCL line is "L". SDA line condition must be stable and fixed while the clock is "H". Change the Data line condition between "H" and "L" only when the clock signal on the SCL line is "L". Change the SDA line condition while SCL line is "H" only when the start condition or stop condition is input.
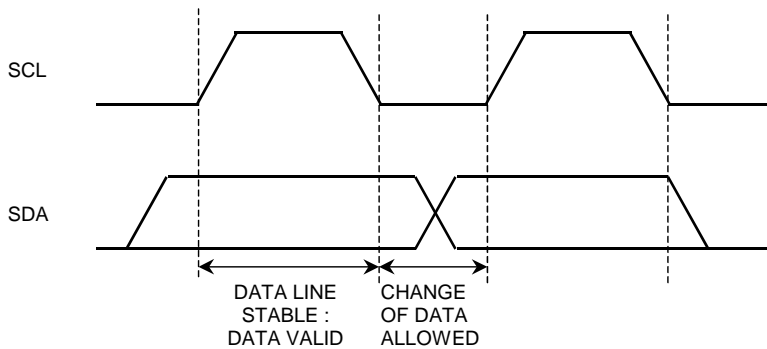
Figure 9. Data Transfer

1-2. Start Condition and Stop Condition

A start condition is generated by the transition of "H" to "L" on the SDA line while the SCL line is "H". All instructions are initiated by a start condition. A stop condition is generated by the transition of "L" to "H" on SDA line while SCL line is "H". All instructions end by a stop condition.
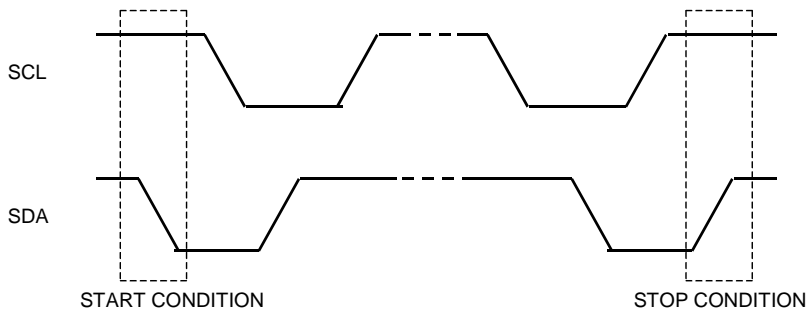
Figure 10. START and STOP conditions

1-3. Acknowledge

An external device that is sending data to the AK4686 releases the SDA line ("H") after receiving one-byte of data. An external device that receives data from the AK4686 then sets the SDA line to "L" at the next clock. This operation is called "acknowledgement", and it enables verification that the data transfer has been properly executed. The AK4686 generates an acknowledgement upon receipt of a start condition and Slave address. For a write instruction, an acknowledgement is generated whenever receipt of each byte is completed. For a read instruction, succeeded by generation of an acknowledgement, the AK4686 releases the SDA line after outputting data at the designated address, and it monitors the SDA line condition. When the master side generates an acknowledgement without sending a stop condition, the AK4686 outputs data at the next address location. When no acknowledgement is generated, the AK4686 ends data output (not acknowledged).
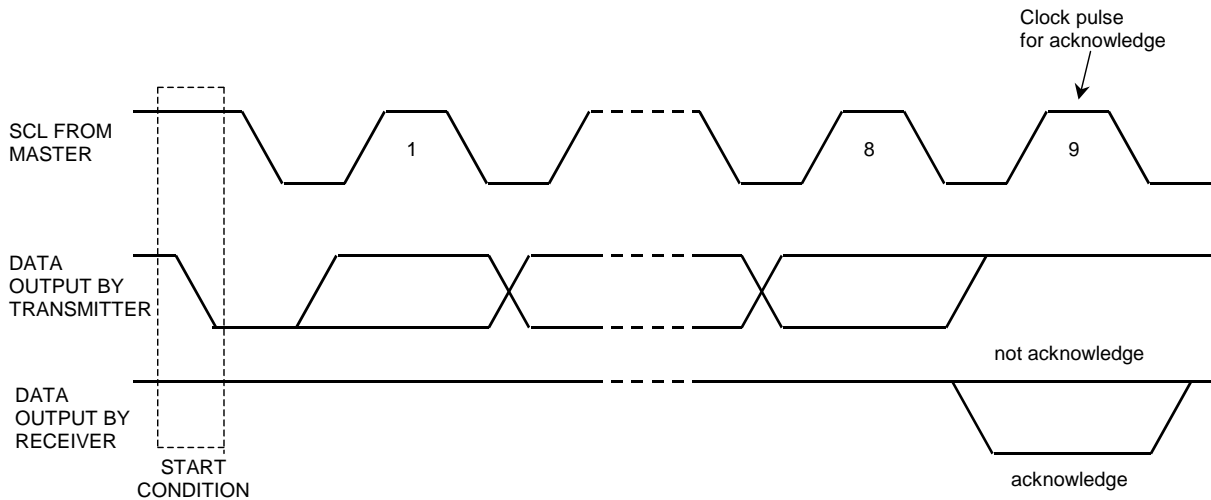
Figure 11. Acknowledge on the I^{2}C-bus

1-4. FIRST BYTE

The First Byte which includes the Slave-address is input after the Start condition is set, and a target IC device that will be accessed on the bus is selected by the Slave-address. The Slave-address is configured with the upper 7-bits. Data of the upper 5-bits is "00100". The next 2 bits are address bits that select the desired IC, and these CAD1 and CAD0 bits are fixed to "10". When the Slave-address is inputted, an external device that has the identical device address generates an acknowledgement and instructions are then executed. The 8th bit of the First Byte (lowest bit) is allocated as the R/W bit. When the R/W bit is "1", the read instruction is executed, and when it is "0", the write instruction is executed.

0	0	1	0	0	CAD1	CAD0	R/W

Figure 12. The First Byte

2. WRITE Operations

Set R/W bit = "0" for the WRITE operation of the AK4686.
After receipt of the start condition and the first byte, the AK4684 generates an acknowledge, and awaits the second byte (register address). The second byte consists of the address for control registers of AK4686. The format is MSB first, and those most significant 3-bits are "Don't care".

*	*	*	A4	A3	A2	A1	A0

(*: Don't care)
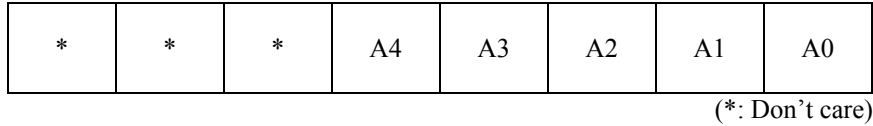
Figure 13. The Second Byte

After receipt of the second byte, the AK4686 generates an acknowledge, and awaits the third byte. Those data after the second byte contain control data. The format is MSB first, 8bits.

D7	D6	D5	D4	D3	D2	D1	D0
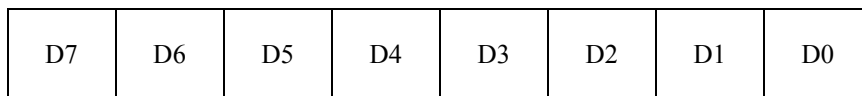
Figure 14. Byte Structure after the Second Byte

The AK4686 is capable of more than one byte write operation by one sequence.
After receipt of the third byte, the AK4686 generates an acknowledge, and awaits the next data again. The master can transmit more than one data word instead of terminating the write cycle after the first data word is transferred. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 05H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.
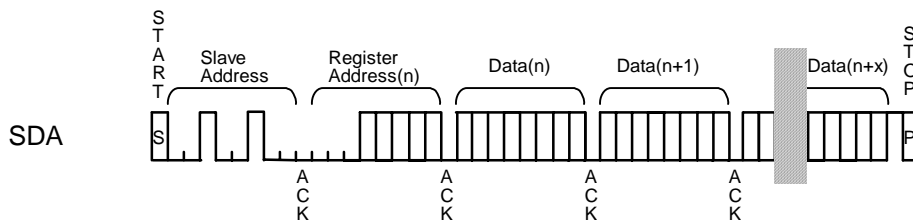
Figure 15. WRITE Operation

3. READ Operations

Set R/W bit = "1" for the READ operation of the AK4686.
The master can read next address's data by generating the acknowledge instead of terminating the write cycle after the receipt of the first data word. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 0DH prior to generating stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4686 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

3-1. CURRENT ADDRESS READ

The AK4686 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address "n", the next CURRENT READ operation would access data from the address "n+1".
After receipt of the slave address with R/W bit set to "1", the AK4686 generates an acknowledge, transmits 1byte data, which address is set by the internal address counter, and increments the internal address counter by 1. If the master does not generate an acknowledge but generate stop condition, the AK4686 discontinues transmission
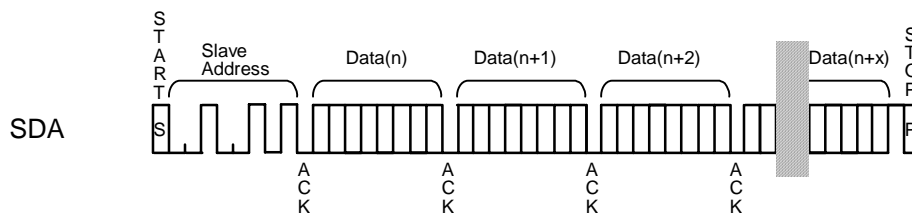
Figure 16. CURRENT ADDRESS READ

3-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation.
The master issues start condition, slave address(R/W bit="0") and then the register address to read. After the register address's acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4686 generates an acknowledge, 1byte data and increments the internal address counter by 1. If the master does not generate an acknowledge but generate the stop condition, the AK4686 discontinues transmission.
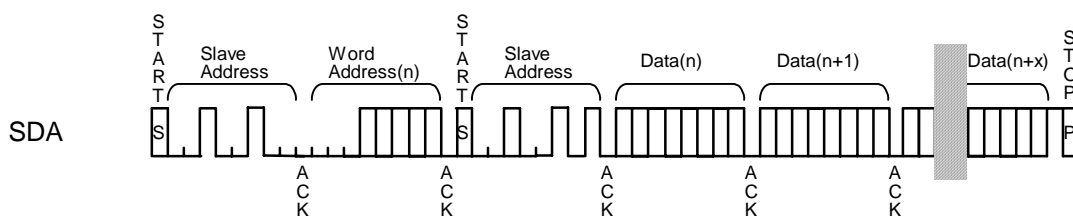
Figure 17. RANDOM READ

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Powerdown 1	0	0	0	0	0	MT2N	MT1N	RSTN
01H	Powerdown 2	0	PWDA2	PWDA1	PWAD	0	ACKS2	DFS21	DFS20
02H	Audio Data Format	0	0	0	0	DIF21	DIF20	DIF11	DIF10
03H	De-emphasis/ ATT speed	DEM21	DEM20	DEM11	DEM10	0	0	0	0
04H	Clock Control	0	ACKS1	DFS11	DFS10	0	CKS12	CKS11	CKS10
05H	Input Selector Control & Analog mute control	0	AMTS2	AMTS1	AMTS0	AIN3	AIN2	AIN1	AIN0

Note: For addresses from 06H to 1FH, data must not be written.
 When the PDN pin is set to "L", the registers are initialized to their default values.
 When RSTN bit is set to "0", the internal timing is reset, but registers are not initialized to their default values.
 The bits defined as 0 must contain a "0" value.

■ **Register Definitions**

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Powerdown 1	0	0	0	0	0	MT2N	MT1N	RSTN
	R/W	RD	RD	RD	RD	RD	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	1

RSTN: CODEC Initial Timing Reset
>   0: Reset. Registers are not initialized.
>   1: Normal operation (default)

MT1N: DAC1 Mute Control
>   0: Mute (default)
>   1: Normal Output

MT2N: DAC2 Mute Control
>   0: Mute (default)
>   1: Normal Output

MT1N: DAC1 Analog Soft Mute Control

MT1N Pin	MT1N bit	DAC1Analog Mute Status	
L	0	Mute	(default)
L	1	Mute	
H	0	Mute	(default)
H	1	Unmute	

Table 20. DAC1 Analog Mute Control

MT2N: DAC2 Analog Soft Mute Control

MT2N Pin	MT2N bit	DAC2 Analog Mute Status	
L	0	Mute	(default)
L	1	Mute	
H	0	Mute	(default)
H	1	Unmute	

Table 21. DAC1 Analog Mute Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Powerdown 2	0	PWDA2	PWDA1	PWAD	0	ACKS2	DFS21	DFS20
R/W		RD	R/W	R/W	R/W	RD	R/W	R/W	R/W
Default		0	1	1	1	0	0	0	0

DFS21-20: PORT2(DAC2) Sampling Speed Control
  These settings are ignored in Auto Setting Mode. Refer to Table 9.

ACKS2: PORT2(DAC2) Auto Setting Mode Control
  0: Disable, Manual Setting Mode (default)
  1: Enable, Auto Setting Mode
  Master clock frequency is detected automatically when ACKS2 bit ="1". In this case, the DFS21-20
  bits are ignored. When this bit is "0", DFS21-20 bits set the sampling speed mode.

PWAD: Power-down control of ADC
  0: Power-down
  1: Normal operation (default)

PWDA1: Full-Power-down control of DAC1
  0: Power-down
  1: Normal operation (default)

PWDA2: Full-Power-down control of DAC2
  0: Power-down
  1: Normal operation (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Audio Data Format	0	0	0	0	DIF21	DIF20	DIF11	DIF10
	R/W	RD	RD	RD	RD	R/W	R/W	R/W	R/W
	Default	0	0	0	0	1	1	1	1

DIF21-20: Audio format control for PORT2
　　　　　Refer to Table 17.

DIF11-10: Audio format control for PORT1
　　　　　Refer to Table 16.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	De-emphasis/ ATT speed	DEM21	DEM20	DEM11	DEM10	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	RD	RD	RD	RD
	Default	0	1	0	1	0	0	0	0

DEM11-10: DAC1 De-emphasis filter control
DEM21-20: DAC2 De-emphasis filter control
　　　　　Refer to Table 15.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Clock Control	0	ACKS1	DFS11	DFS10	0	CKS12	CKS11	CKS10
	R/W	RD	R/W	R/W	R/W	RD	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

CKS12-10: PORT1(ADC&DAC1) Clock control in Master mode.
　　　　　Refer to Table 2.

DFS11-10: PORT1(ADC&DAC1) Sampling Speed Control
　　　　　These settings are ignored in Auto Setting Mode. Refer to Table 3.

ACKS1: PORT1(ADC&DAC1) Auto Setting Mode
　　　　0: Disable, Manual Setting Mode (default)
　　　　1: Enable, Auto Setting Mode
　　　　Master clock frequency is detected automatically when ACK1S bit ="1". In this case, the DFS11-10
　　　　bits are ignored. When this bit is "0", DFS11-10 bits set the sampling speed mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Input Selector Control & Analog mute control	0	AMTS2	AMTS1	AMTS0	AIN3	AIN2	AIN1	AIN0
	R/W	RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	1	0	0	0	0

AIN3-0: ADC input selector control
    0000: LIN1/RIN1 (default)
    0001: LIN2/RIN2
    0010: LIN3/RIN3
    0011: LIN4/RIN4
    0100: LIN5/RIN5
    0101: LIN6/RIN6
    1xxx: Mute (x: don't care)

AMTS2-0: Analog Mute Clock Source Control
    Default: "001"
    Refer to Table 18.

SYSTEM DESIGN

Figure 18 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.
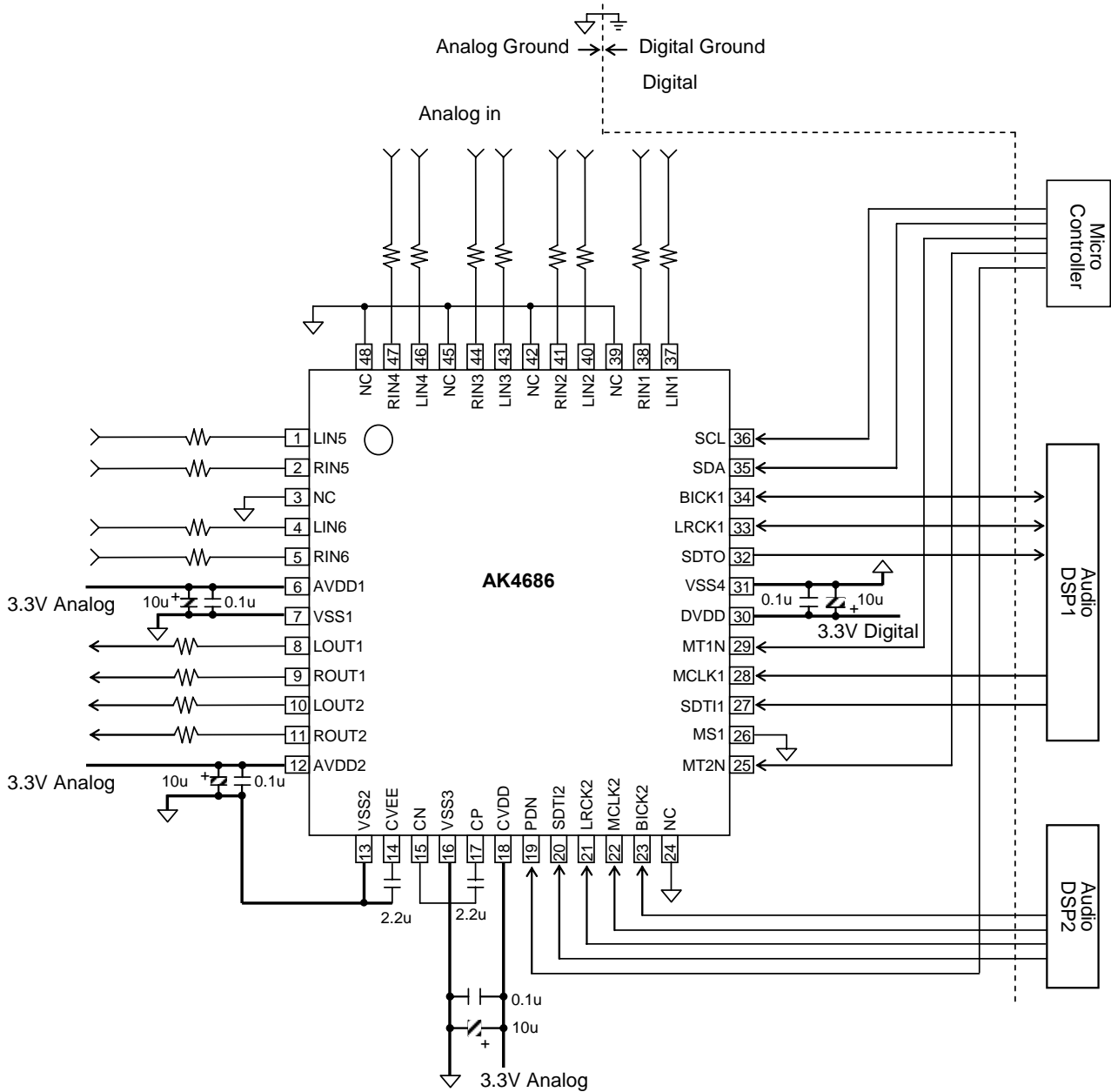
Figure 18. Typical Connection Diagram (Slave mode)

Notes:
  - VSS1, VSS2, VSS3, and VSS4 must be connected to the same analog ground plane.

1. Grounding and Power Supply Decoupling

The AK4686 requires careful attention to power supply and grounding arrangements. AVDD1, AVDD2, DVDD and CVDD are usually supplied from analog supply in system. If AVDD1, AVDD2, DVDD, and CVDD are supplied separately, it is recommended to power-up DVDD first to avoid a click noise. **VSS1, VSS2, VSS3 and VSS4 of the AK4686 must be connected to analog ground plane.** System analog ground and digital ground must be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4686 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference Inputs

The voltage of AVDD1 sets the ADC input range, and AVDD1 (AVDD2) sets the DAC1(DAC2) analog output range. A $0.1\mu F$ ceramic capacitor should be attached between the AVDD1/2 pin and VSS1/2 pin.

3. Analog Inputs

The AK4686 receives the analog input through the single-ended Pre-amp. The input range is 2.2 x AVDD1/3.3 Vrms (typ. fs=48kHz) at each analog input pins. Each input pins are biased to 0V(typ) internally. The ADC output data format is 2's complement. The internal digital HPF removes the DC offset.

The AK4686 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. The AK4686 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.
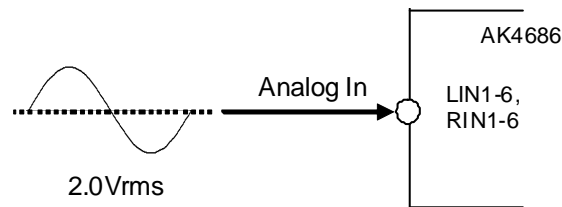
Figure 19. External Circuit Example1

4. Analog Outputs

The analog outputs are also single-ended and centered on 0V (typ). The output signal range scales with the supply voltage and nominally 2 x AVDD2(AVDD3)/3.3 Vrms at each analog output pins. The DAC1(DAC2) input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal output is 0V for 000000H(@24bit). The internal analog filters (SCF and CTF) remove most of the noise generated by the delta-sigma modulator of DAC1(DAC2) beyond the audio passband.

The DC offsets on analog outputs are typically 0V.
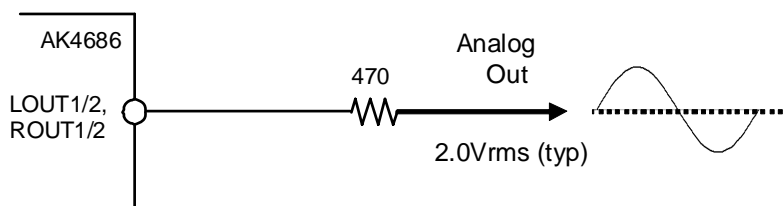
Figure 20. External Circuit Example1

5. Attention to the PCB Wiring

Attention should be given to avoid coupling with other signals on each analog input/output pins. Unused input pins among LIN1-6 and RIN1-6 pins must be left open.

PACKAGE

48pin LQFP(Unit: mm)
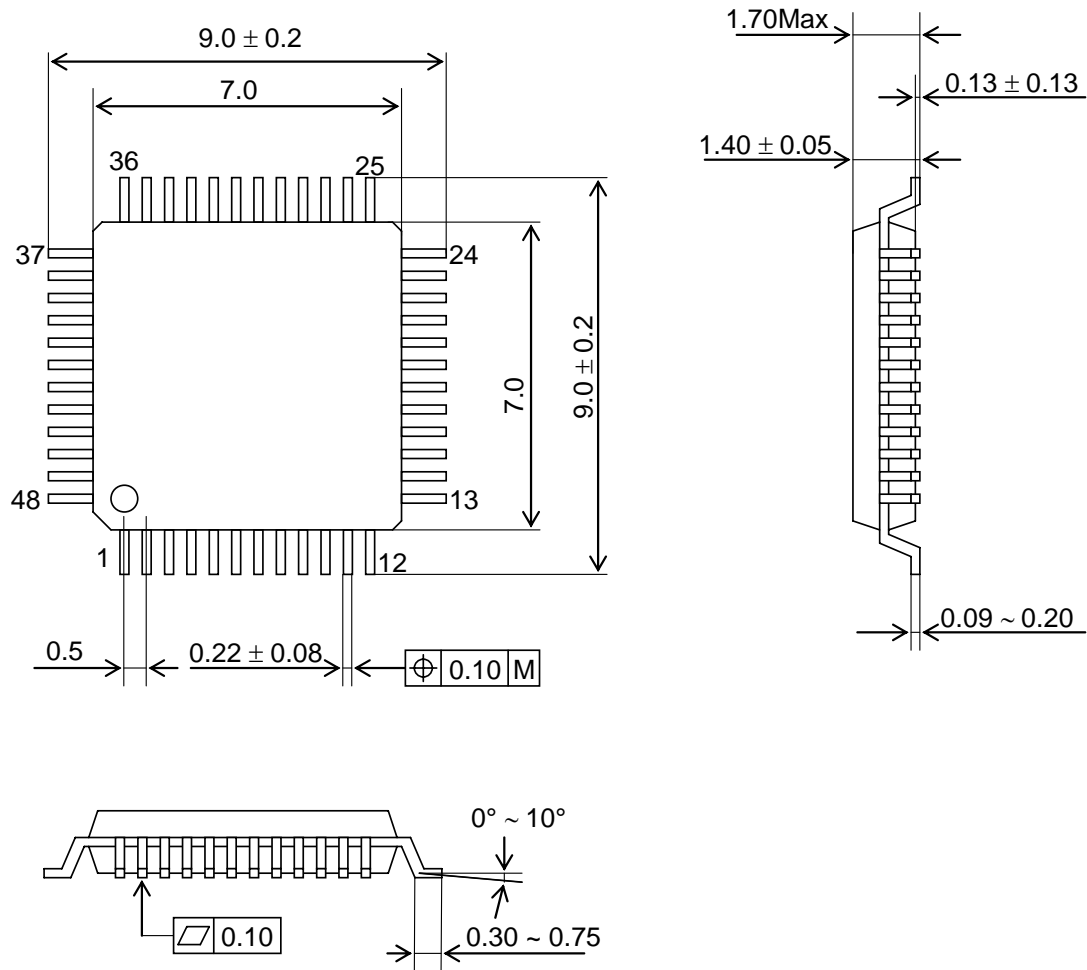
■ Material & Lead Finish

Package molding compound: Epoxy, Halogen (Bromine and Chlorine) free
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING
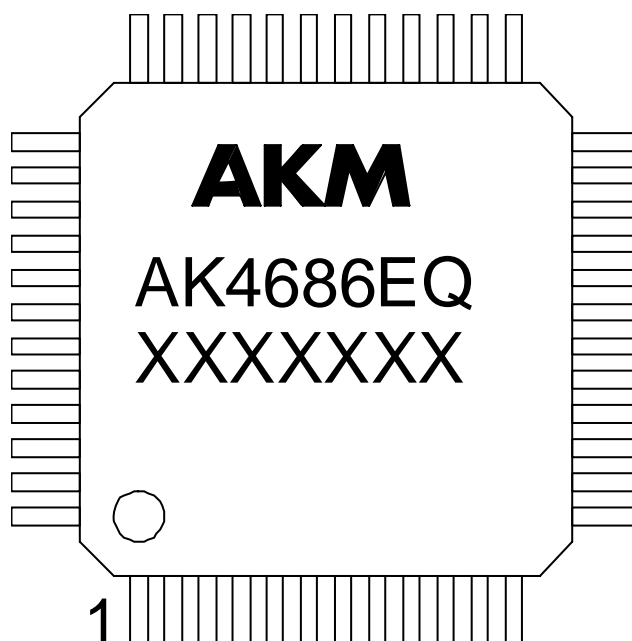
1) Pin #1 indication
2) Asahi Kasei Logo
3) Marking Code: AK4686EQ
4) Date Code: XXXXXXX (7 digits)

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
10/10/05	00	First Edition		

10/10/25	01	Specification Change	7	Analog Characteristics
				  DAC to Analog Output
				   Output Voltage: 1.85 → 1.90Vrms (min)

IMPORTANT NOTICE