Ordering number : EN7441B

STK672-060-E

ON Semiconductor®

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Thick-Film Hybrid IC

Unipolar Constant-current Chopper (external excitation PWM) Circuit with Built-in Microstepping Controller Stepping Motor Driver (sine wave drive) Output Current 1.2A (no heat sink*)

Overview

The STK672-060-E is a stepping motor driver hybrid IC that uses power MOSFETs in the output stage. It includes a built-in microstepping controller and is based on a unipolar constant-current PWM system. The STK672-060-E supports application simplification and standardization by providing a built-in 4 phase distribution stepping motor controller. It supports five excitation methods: 2 phase, 1-2 phase, W1-2 phase, 2W1-2 phase, and 4W1-2 phase excitations, and can provide control of the basic stepping angle of the stepping motor divided into 1/16 step units. It also allows the motor speed to be controlled with only a clock signal.
The use of this hybrid IC allows designers to implement systems that provide high motor torques, low vibration levels, low noise, fast response, and high-efficiency drive.

Applications

- Facsimile stepping motor drive (send and receive)
- Paper feed and optical system stepping motor drive in copiers
- Laser printer drum drive
- Printer carriage stepping motor drive
- X-Y plotter pen drive
- Other stepping motor applications

Note*: Conditions: $V_{CC}1$ = 24V, I_{OH} = 1.2A, 2W1-2 excitation mode.

Features

- Can implement stepping motor drive systems simply by providing a DC power supply and a clock pulse generator.

<Control Block Features>

- One of five drive types can be selected with the drive mode settings (M1, M2, and M3)
  1) 2 phase excitation drive
  2) 1-2 phase excitation drive
  3) W1-2 phase excitation drive
  4) 2W1-2 phase excitation drive
  5) 4W1-2 phase excitation drive

- Provides four freely selectable modes for the vector locus during microstepping drive: circular mode, one inside mode, and two outside modes.
- Phase retention even if excitation is switched.
- The excitation phase state can be verified in real time using the MO1, MO2, and MOI signal output pins.
- The CLK input counter block can be selected to be one of the following by the high/low setting of the M3 input pin.
  1) Rising edge only
  2) Both rising and falling edges
- The CLK and $\overline{\text{RETURN}}$ input pins include built-in malfunction prevention circuits for external pulse noise.
- ENABLE and $\overline{\text{RESET}}$ pins provided. These are Schmitt trigger inputs with built-in 20kΩ (typical) pull-up resistors.
- No noise generation due to the difference between the A and B phase time constants during motor hold since external excitation is used.
- Microstepping operation supported even for small motor currents, since the reference voltage Vref can be set to any value between 0V and 1/2V_{CC}2.

<Driver Block>

- External excitation PWM drive allows a wide operating supply voltage range (V_{CC}1 = 10 to 45V) to be used.
- Current detection resistor (0.22Ω) built-in the hybrid IC itself.
- Power MOSFETs adopted for low drive loss.
- Provides a motor output drive current of I_{OH} = 1.2A.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	V_{CC}1 max	No signal	52	V
Maximum supply voltage 2	V_{CC}2 max	No signal	-0.3 to +7.0	V
Input voltage	V_{IN} max	Logic input pins	-0.3 to +7.0	V
Output current	I_{OH} max	0.5s, 1 pulse, when V_{CC}1 applied	1.6	A
Repeated avalanche capacity	Ear max		25	mJ
Allowable power dissipation	Pd max	θc-a = 0	7	W
Operating substrate temperature	Tc max		105	°C
Junction temperature	Tj max		150	°C
Storage temperature	Tstg		-40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC}1	With signals applied	10 to 45	V
Supply voltage 2	V_{CC}2	With signals applied	5 ± 5%	V
Input voltage	V_{IH}		0 to V_{CC}2	V
Phase driver withstand voltage	V_{DSS}	Tr1, 2, 3, and 4 (the A, $\overline{\text{A}}$, B, and $\overline{\text{B}}$ outputs)	100 (min)	V
Output current	I_{OH}	Duty 50%	1.2	A

Electrical Characteristics at Tc = 25°C, $V_{CC}1$ = 24V, $V_{CC}2$ = 5V

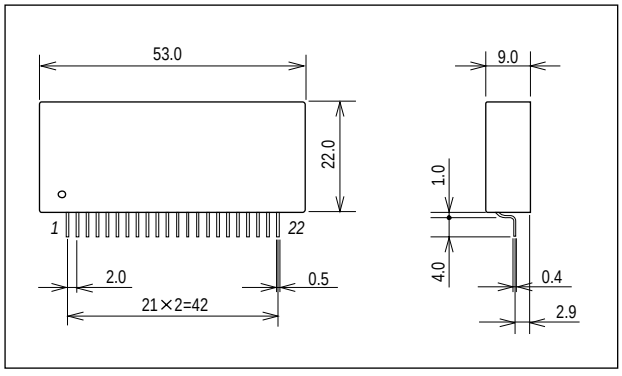
Parameters	Symbols	Conditions	Rating			unit
			min	typ	max	
Control supply current	I_{CC}	Pin 7, with ENABLE pin held low.		2.5	14	mA
Output saturation voltage	Vsat	R_L = 23Ω (I ≈ 1A)		0.8	1.1	V
Average output current	Ioave	Load: R = 3.5Ω / L = 3.8mH For each phase, Vref ≈ 1.69V	0.470	0.524	0.580	A
FET diode forward voltage	Vdf	If = 1A		1.2	1.8	V
[Control Inputs]						
Input voltage	V_{IH}	Except for the Vref pin	4			V
	V_{IL}	Except for the Vref pin			1	V
Input current	I_{IH}	Except for the Vref pin	0	1	10	μA
	I_{IL}	Except for the Vref pin	125	250	510	μA
[Vref Input Pin]						
Input voltage	V_I	Pin 8	0		2.5	V
Input current	I_I	Pin 8, V_I = 2.5V	330	415	545	μA
[Control Outputs]						
Output voltage	V_{OH}	I = –3mA, pins MOI, MO1, MO2	2.4			V
	V_{OL}	I = +3mA, pins MOI, MO1, MO2			0.4	V
[Current Distribution Ratio (A·B)]						
2W1-2, W1-2, 1-2	Vref	θ = 1/8		100		%
2W1-2, W1-2	Vref	θ = 2/8		92		%
2W1-2	Vref	θ = 3/8		83		%
2W1-2, W1-2, 1-2	Vref	θ = 4/8		71		%
2W1-2	Vref	θ = 5/8		55		%
2W1-2, W1-2	Vref	θ = 6/8		40		%
2W1-2	Vref	θ = 7/8		21		%
2	Vref			100		%
PWM frequency	fc		37	47	57	kHz

Note: A constant-voltage power supply must be used.
The design target value is shown for the current distribution ratio.

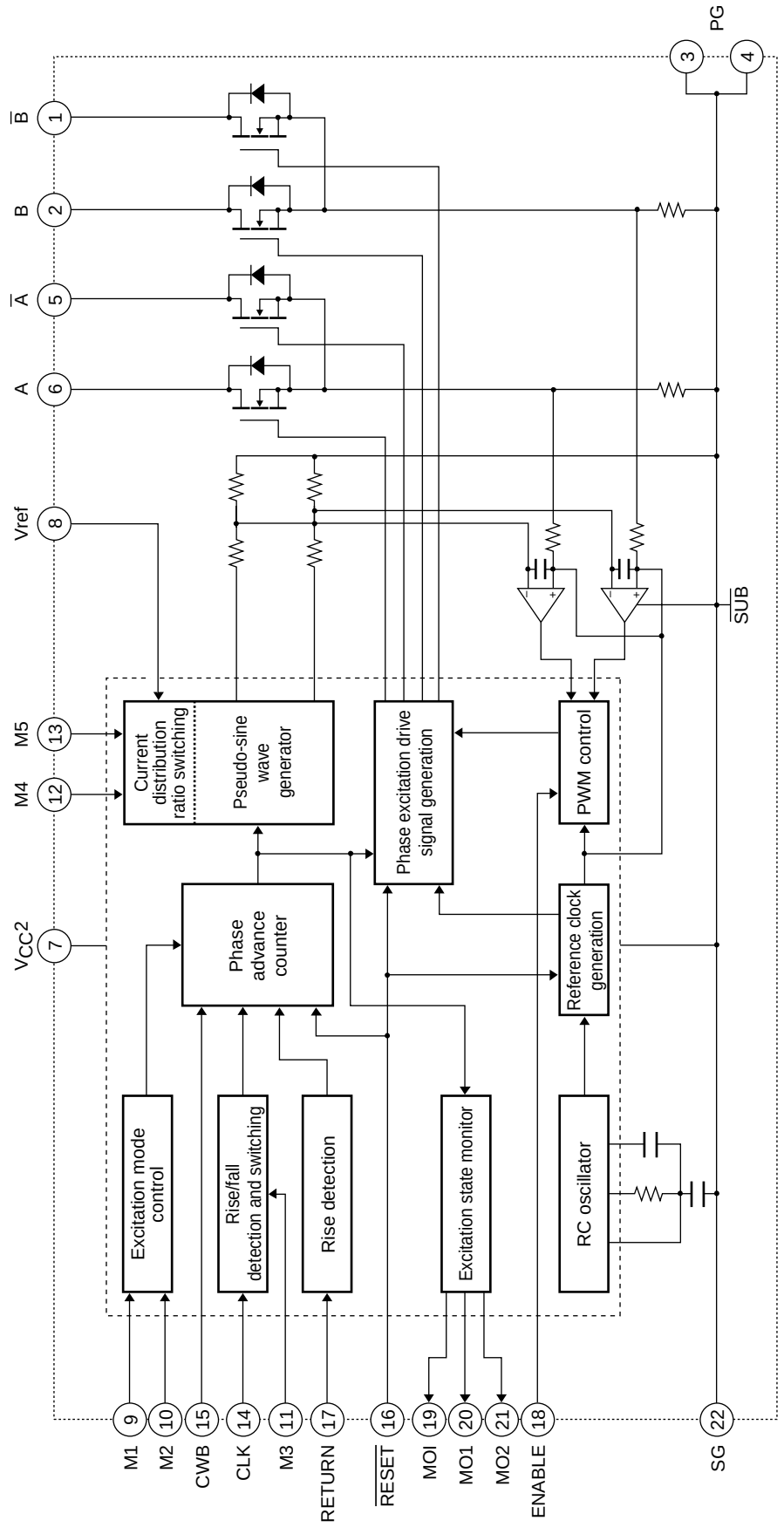
Package Dimensions

unit:mm (typ)

4161

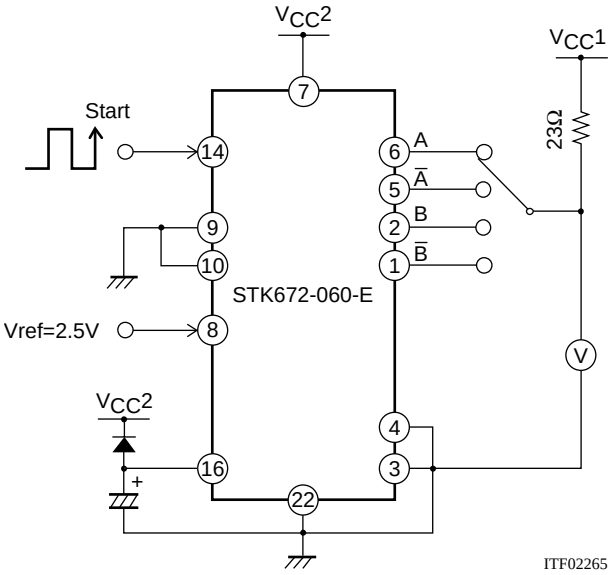


Internal Block Diagram

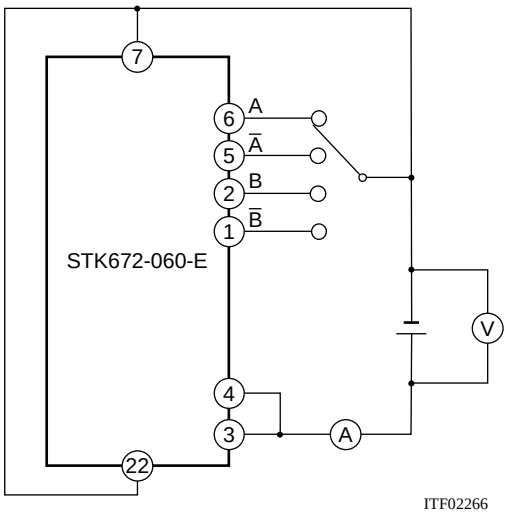


Test Circuit Diagrams

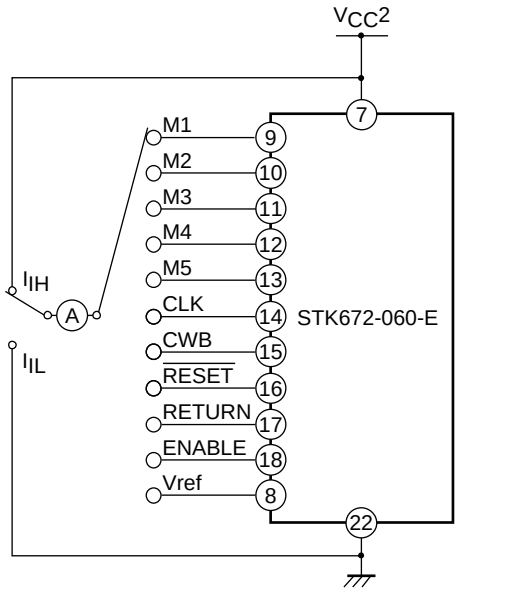
Vsat



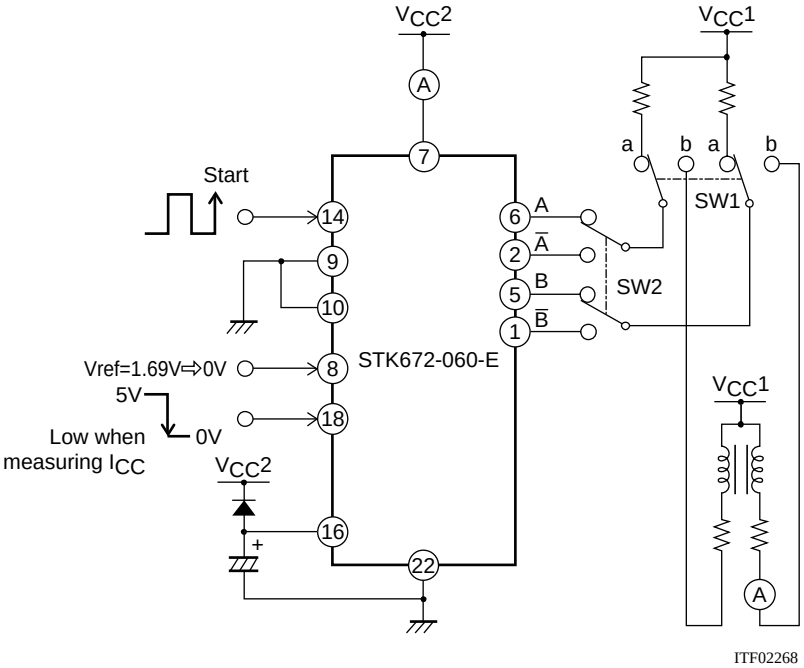
Vdf



I_{IH}, I_{IL}



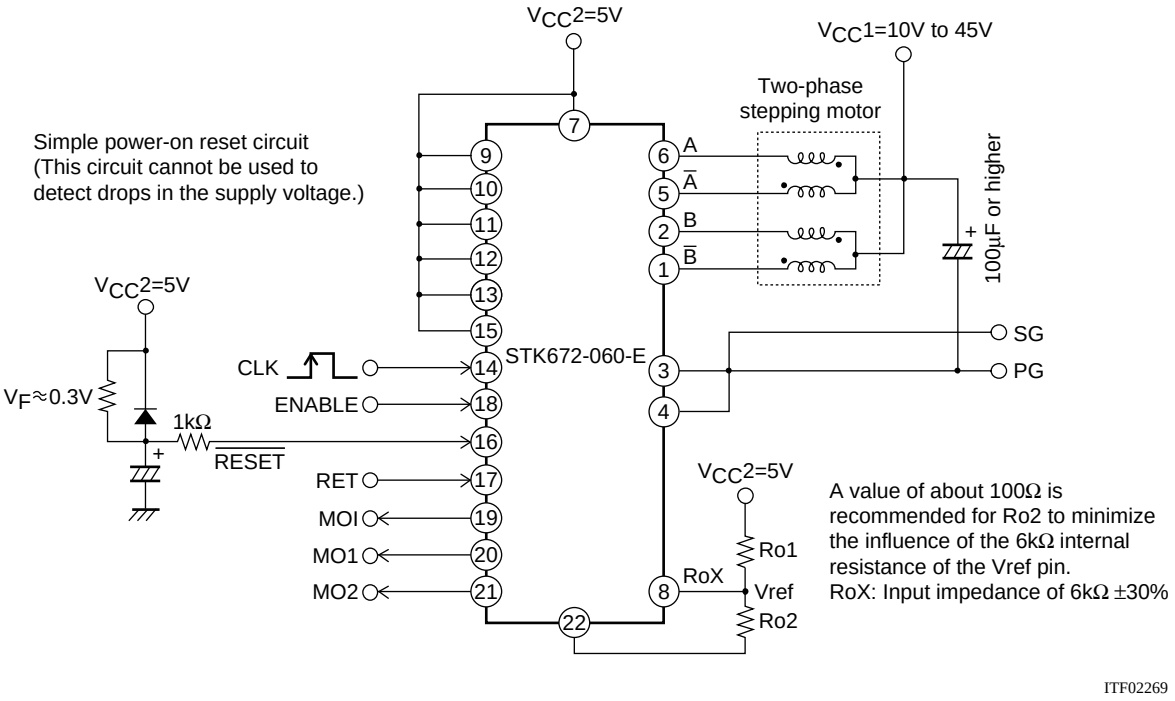
Ioave, I_{CC}, fc



When measuring Ioave: With SW1 set to ‘b’, Vref = 1.69V
When measuring fc: With SW1 set to ‘a’, Vref = 0V
When measuring I_{CC}: Set ENABLE low

Power-on Reset

The application must perform a power-on reset operation when $V_{CC}2$ power is first applied to this hybrid IC.
Application circuit that used 2W1-2 phase excitation (microstepping operation) mode.



Setting the Motor Current

The motor current I_{OH} is set by the Vref voltage on the hybrid IC pin 8. The following formula gives the relationship between I_{OH} and Vref.

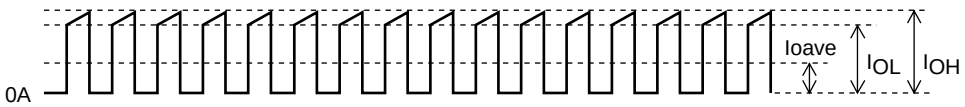
$$RoX = (Ro2 \times 6k\Omega) \div (Ro2 + 6k\Omega) \quad (1)$$

$$Vref = V_{CC}2 \times RoX \div (Ro1 + RoX) \quad (2)$$

$$I_{OH} = \frac{1}{K} \times \frac{Vref}{Rs} \quad (3)$$

K: 7.66 (voltage divider ratio),
Rs: 0.22Ω (This is the hybrid IC's internal current detection resistor. It has a tolerance of ±3%.)

Applications can use motor currents from the current (0.05 to 0.1A) set by the duty of the frequency set by the oscillator up to the limit of the allowable operating range, I_{OH} = 1.2A



Motor current waveform A13262

Function Table

M2	0	0	1	1	Phase switching clock edge timing
M1 / M3	0	1	0	1	
1	2 phase excitation	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	Rising edge only
0	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	4W1-2 phase excitation	Rising and falling edges

	Forward	Reverse
CWB	0	1

ENABLE	Motor current is cut off when low
$\overline{RESET}$	Active low

	A	$\overline{A}$	B	$\overline{B}$
MO1	1	0	0	1
MO2	0	0	1	1

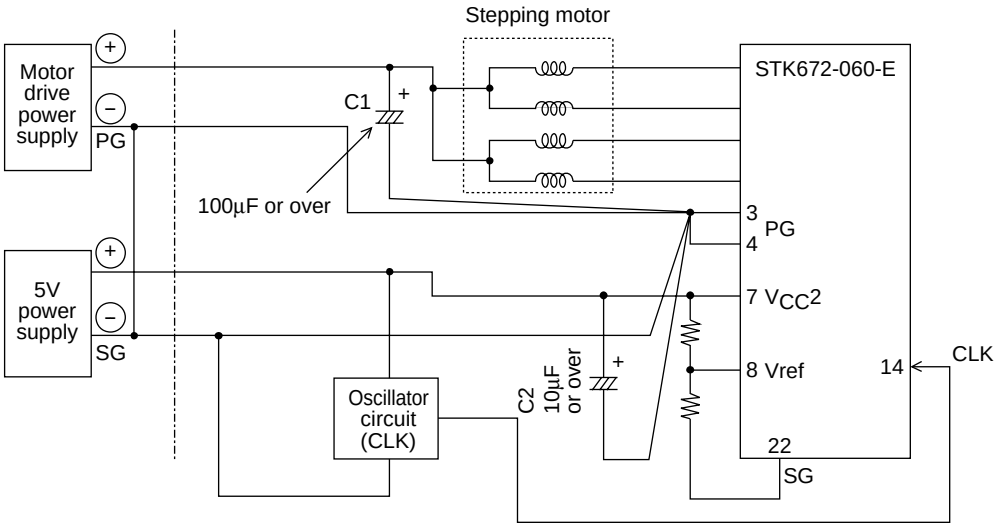
Printed Circuit Board Design Recommendations

This hybrid IC has two grounds, the PG pins (pins 3 and 4) and the SG pin (pin 22). These are connected internally in the hybrid IC.

Two power supplies are required: a motor drive supply and a 5V supply for the hybrid IC itself. If the ground connections for these supplies are not good, the motor current waveforms may become unstable, motor noise may increase, and vibration levels may increase. Use appropriate wiring for these grounds. Here we present two methods for implementing these ground connections.

If the grounds for the motor drive supply and the hybrid IC 5V supply are connected in the immediate vicinity of the power supplies:

- If PG and SG are shorted at the power supply, connect only the PG line to pins 3 and 4 on the hybrid IC. Also, be sure that no problems occur due to voltage drops due to common impedances. In the specifications, this must be $V_{CC}2$ ±5%.
- The current waveforms will be more stable if the Vref ground is connected to pin 22.
- For initial values, use 100µF or over for C1 and 10µF or over for C2.
  Locate C1 as close to the hybrid IC as possible, and the capacitor ground line must be as short as possible.



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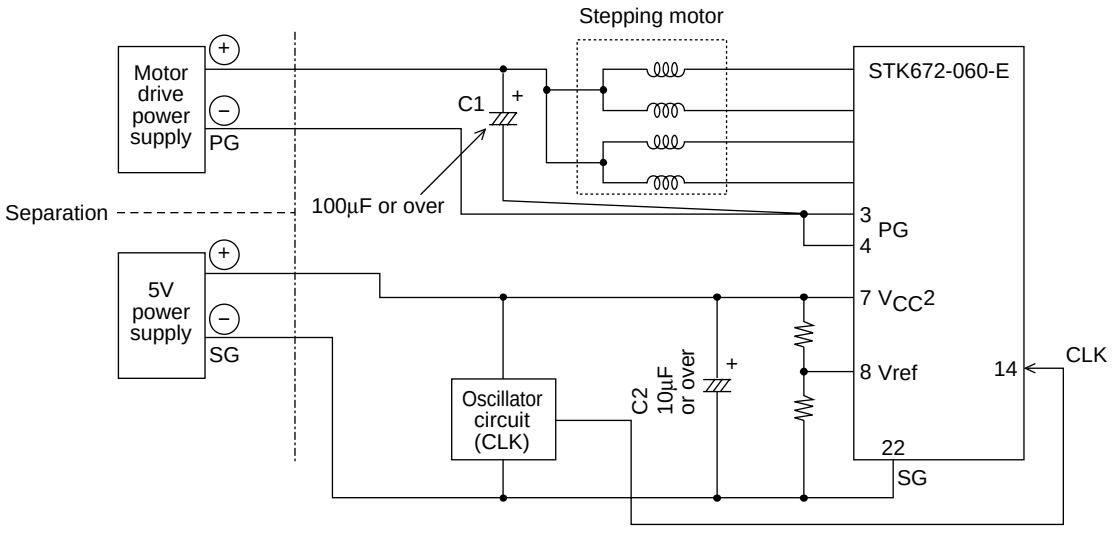
If the grounds for the motor drive supply and the hybrid IC 5V supply are separated:

- Insert a capacitor (C1) of 100µF or over as close as possible to the hybrid IC. The capacitor ground line must be as short as possible.
  The capacitor C2 may be included if necessary. Its ground line should also be as short as possible.



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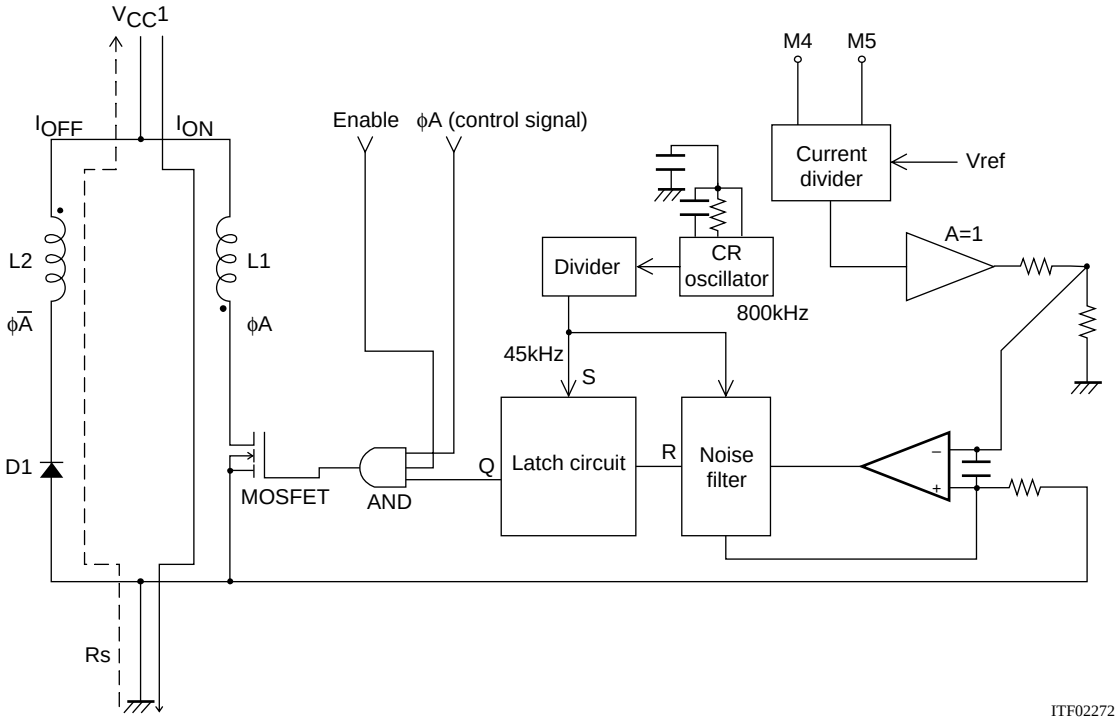
Functional Description

External Excitation Chopper Drive Block Description



Driver Block Basic Circuit Structure

Since this hybrid IC adopts an external excitation method, no external oscillator circuit is required.
When a high level is input to ϕA in the basic driver block circuit shown in the figure and the MOSFET is turned on, the comparator + input will go low and the comparator output will go low. Since a set signal with the PWM period will be input, the Q output will go high, and the MOSFET will be turned on as its initial value.
The current I_{ON} flowing in the MOSFET passes through L1 and generates a potential difference in Rs. Then, when the Rs potential and the Vref potential become the same, the comparator output will invert, and the reset signal Q output will invert to the low level. Then, the MOSFET will be turned off and the energy stored in L1 will be induced in L2 and the current I_{OFF} will be regenerated to the power supply. This state will be maintained until the time when an input to the latch circuit set pin occurs.
In this manner, the Q output is turned off and on repeatedly by the reset and set signals, thus implementing constant current control. The resistor and capacitor on the comparator input are spike removal circuit elements and synchronize with the PWM frequency. Since this hybrid IC uses a fixed frequency due to the external excitation method and at the same time also adopts a synchronized PWM technique, it can suppress the noise associated with holding a position when the motor is locked.

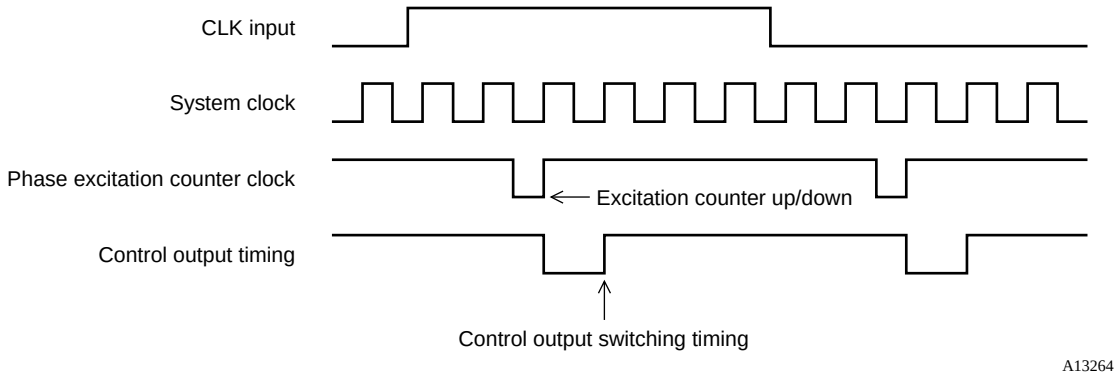
Input Pin Functions

Pin No.	Symbol	Function	Pin circuit type
14	CLK	Phase switching clock	Built-in pull-up resistor CMOS Schmitt trigger input
15	CWB	Rotation direction setting (CW/CCW)	Built-in pull-up resistor CMOS Schmitt trigger input
17	RETURN	Forced phase origin return	Built-in pull-up resistor CMOS Schmitt trigger input
18	ENABLE	Output cutoff	Built-in pull-up resistor CMOS Schmitt trigger input
9, 10, 11	M1, M2, M3	Excitation mode setting	Built-in pull-up resistor CMOS Schmitt trigger input
12, 13	M4, M5	Vector locus setting	Built-in pull-up resistor CMOS Schmitt trigger input
16	$\overline{\text{RESET}}$	System reset	Built-in pull-up resistor CMOS Schmitt trigger input
8	Vref	Current setting	Operational amplifier input

Input Signal Functions and Timing

- CLK (phase switching clock)
  1) Input frequency range: DC to 50kHz
  2) Minimum pulse width: 10μs
  3) Duty: 40 to 60% (However, the minimum pulse width takes precedence when M3 is high.)
  4) Pin circuit type: Built-in pull-up resistor (20kΩ, typical) CMOS Schmitt trigger structure
  5) Built-in multi-stage noise rejection circuit
  6) Function:
     - When M3 is high or open: The phase excited (driven) is advanced one step on each CLK rising edge.
     - When M3 is low: The phase is advanced one step by both rising and falling edges, for a total of two steps per cycle.

CLK Input Acquisition Timing (M3 = Low)



- CWB (Method for setting the rotation direction)
  1) Pin circuit type: Built-in pull-up resistor (20kΩ, typical) CMOS Schmitt trigger structure
  2) Function:
     - When CWB is low: The motor turns in the clockwise direction.
     - When CWB is high: The motor turns in the counterclockwise direction.
  3) Notes: When M3 is low, the CWB input must not be changed for about 6.25μs before or after a rising or falling edge on the CLK input.

- RETURN (Forcible return to the origin for the currently excited phase)
  1) Pin circuit type: Built-in pull-up resistor (20kΩ, typical) CMOS Schmitt trigger structure
  2) Built-in noise rejection circuit
  3) Notes: The currently excited (driven) phase can be forcibly moved to the origin by switching this input from low to high. Normally, if this input is unused, it must be left open or connected to $V_{CC}2$.

- ENABLE (Controls the on/off state of the A, $\overline{A}$, B, and $\overline{B}$ excitation drive outputs and selects either operating or hold as the internal state of this hybrid IC.)
  1) Pin circuit type: Built-in pull-up resistor (20kΩ, typical) CMOS Schmitt trigger structure
  2) Function:
     - When ENABLE is high or open: Normal operating state
     - When ENABLE is low: This hybrid IC goes to the hold state and excitation drive output (motor current) is forcibly turned off. In this mode, the hybrid IC system clock is stopped and no inputs other than the reset input have any effect on the hybrid IC state.

• M1, M2, and M3 (Excitation mode and CLK input edge timing selection)

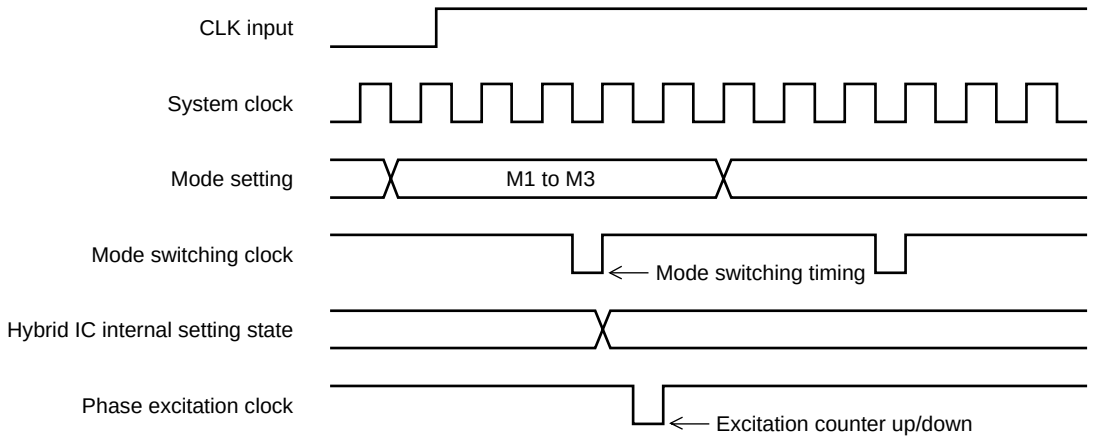
1) Pin circuit type: Built-in pull-up resistor (20kΩ, typical) CMOS Schmitt trigger structure

2) Function:

M2	0	0	1	1	Phase switching clock edge timing
M1 / M3	0	1	0	1	
1	2 phase excitation	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	Rising edge only
0	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	4W1-2 phase excitation	Rising and falling edges

3) Valid mode setting timing: Applications must not change the mode in the period 5µs before or after a CLK signal rising or falling edge.

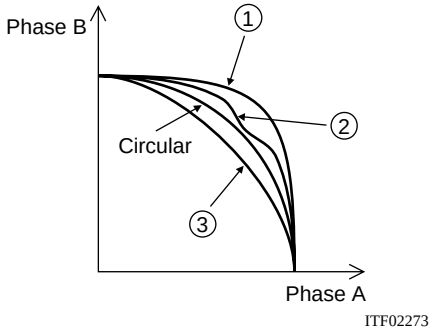
Mode Setting Acquisition Timing



• M4 and M5 (Microstepping mode rotation vector locus setting)

M4	1	0	1	0
M5	1	0	0	1
Mode	Circular	①	②	③

See page 11 for details on the current division ratio.



• $\overline{\text{RESET}}$ (Resets all parts of the system.)

1) Pin circuit type: Built-in pull-up resistor (20kΩ, typical) CMOS Schmitt trigger structure

2) Function:

- All circuit states are set to their initial values by setting the $\overline{\text{RESET}}$ pin low. (Note that the pulse width must be at least 10µs.)
  At this time, the A and $\overline{\text{B}}$ phases are set to their origin, regardless of the excitation mode. The output current goes to about 71% after the reset is released.

3) Notes: When power is first applied to this hybrid IC, Vref must be established by applying a reset. Applications must apply a power on reset when the $V_{CC}2$ power supply is first applied.

• Vref (Sets the current level used as the reference for constant-current detection.)

1) Pin circuit type: Analog input structure

2) Function:

- Constant-current control can be applied to the motor excitation current at 100% of the rated current by applying a voltage less than the control system power supply voltage $V_{CC}2$ minus 2.5V.
- Applications can apply constant-current control proportional to the Vref voltage, with this value of 2.5V as the upper limit.

Output Pin Functions

Pin No.	Symbol	Function	Pin circuit type
19	MOI	Phase excitation origin monitor	Standard CMOS structure
20, 21	MO1, MO2	Phase excitation state monitor	Standard CMOS structure

Output Signal Functions and Timing

- A, $\overline{A}$, B, and $\overline{B}$ (Motor phase excitation outputs)
  1) Function:
     - In the 4 phase and 2 phase excitation modes, a 3.75μs (typical) interval is set up between the A and $\overline{A}$ and B and $\overline{B}$ output signal transition times.

- MO1, MO2, and MOI (Phase excitation state monitors)
  1) Pin circuit type: Standard CMOS structure
  1) Function:
     - Output of the current phase excitation output state.

Phase coordinate	Phase A	Phase B	Phase $\overline{A}$	Phase $\overline{B}$
MO1	1	0	0	1
MO2	0	1	0	1

MOI outputs a 0 when each phase is at the origin, and outputs a 1 otherwise.

- Current division ratios set by M3, M4, and M5 ····· Values provided for reference purposes.

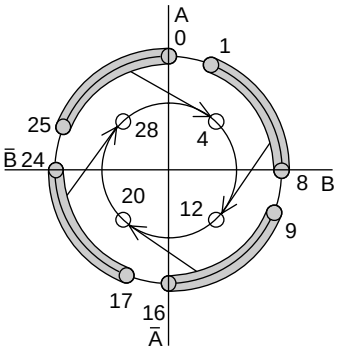
Mode			Circular	①	②	③	Units	Number of steps	
Setting	M3 = 0	M3 = 1	M4 = 1 M5 = 1	M4 = 0 M5 = 0	M4 = 1 M5 = 0	M4 = 1 M5 = 1			
Current division ratio	4W1-2		15	16	16	15	%		1/16
		2W1-2	21	25	24	20		1/8	2/16
			31	34	33	28			3/16
		2W1-2	40	44	41	38		2/8	4/16
			47	50	49	44			5/16
		2W1-2	55	59	56	53		3/8	6/16
			63	67	63	60			7/16
		2W1-2	71	75	70	67		4/8	8/16
			76	81	76	73			9/16
		2W1-2	83	87	84	81		5/8	10/16
			87	92	88	84			11/16
		2W1-2	92	95	95	91		6/8	12/16
			96	98	98	93			13/16
		2W1-2	100	100	100	100		7/8	14/16

[Load conditions]
$V_{CC}1$ = 24V, $V_{CC}2$ = 5V, R/L = 3.5/3.8mH

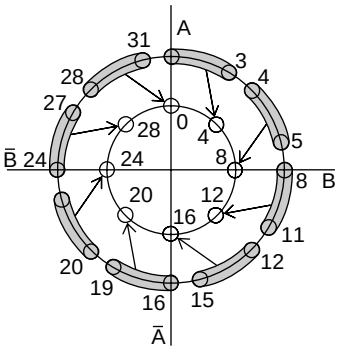
Phase States During Excitation Switching

• Excitation phases before and after excitation mode switching <clockwise direction>

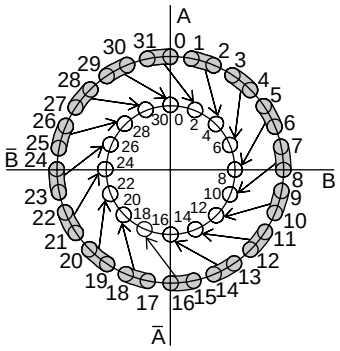
2W1-2 phase → 2 phase



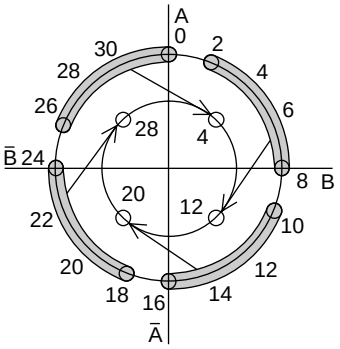
2W1-2 phase → 1-2 phase



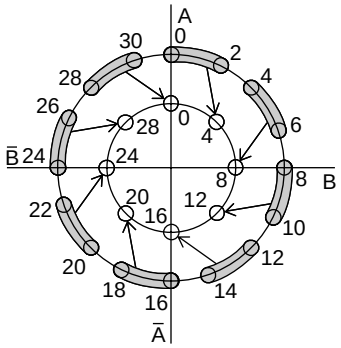
2W1-2 phase → W1-2 phase



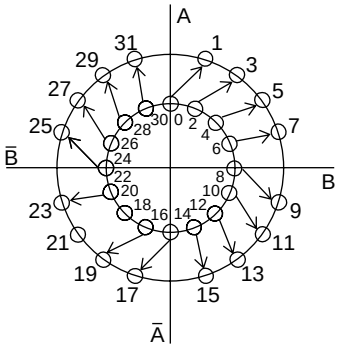
W1-2 phase → 2 phase



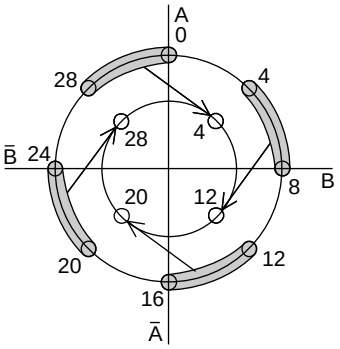
W1-2 phase → 1-2 phase



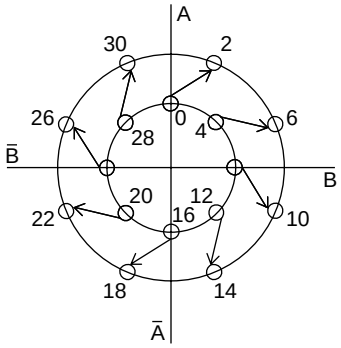
W1-2 phase → 2W1-2 phase



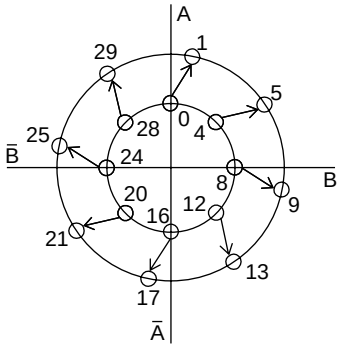
1-2 phase → 2 phase



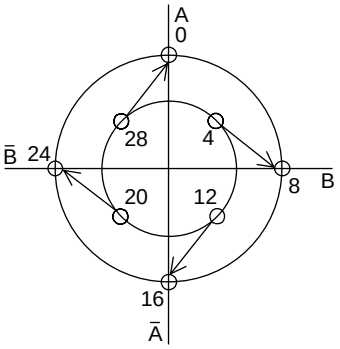
1-2 phase → W1-2 phase



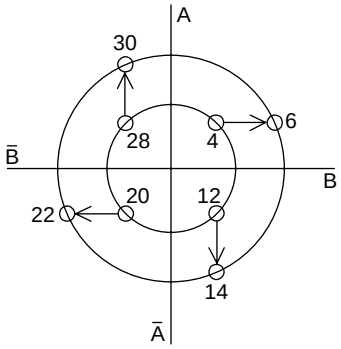
1-2 phase → 2W1-2 phase



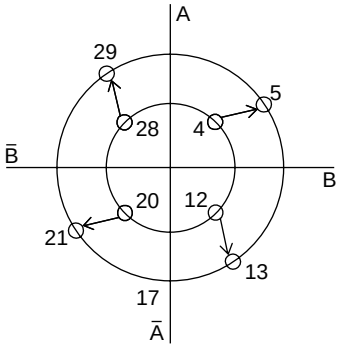
2 phase → 1-2 phase



2 phase → W1-2 phase



2 phase → 2W1-2 phase



Excitation phase developed by the first CLK internal pulse after the change in the excitation mode setting with M1 and M

Excitation phase immediately prior to the excitation mode setting

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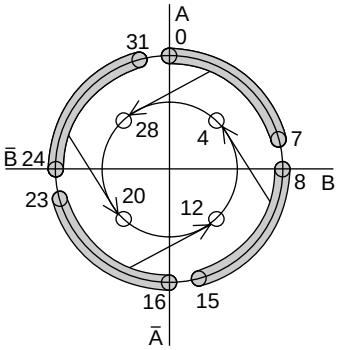
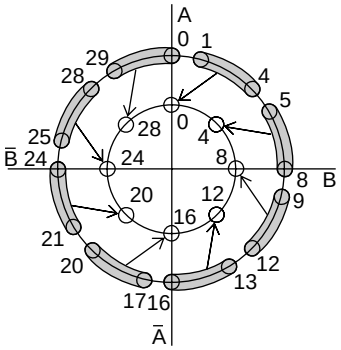
• Excitation phases before and after excitation mode switching <counterclockwise direction>

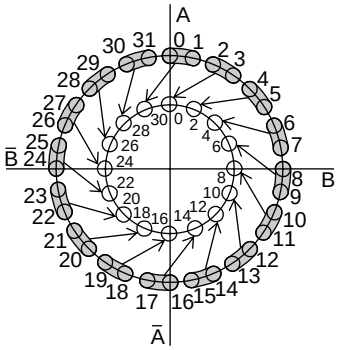
2W1-2 phase → 2 phase



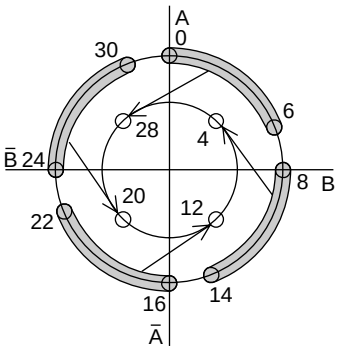
2W1-2 phase → 1-2 phase



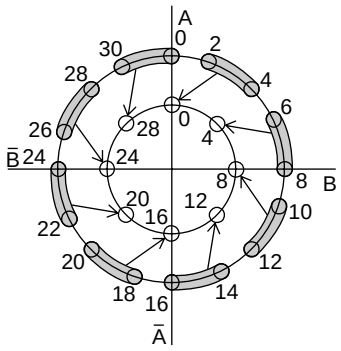
2W1-2 phase → W1-2 phase



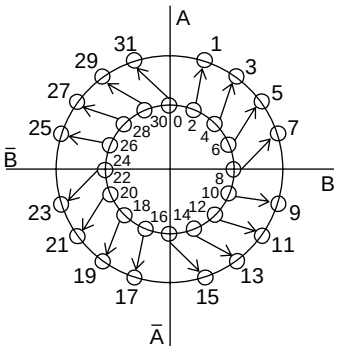
W1-2 phase → 2 phase



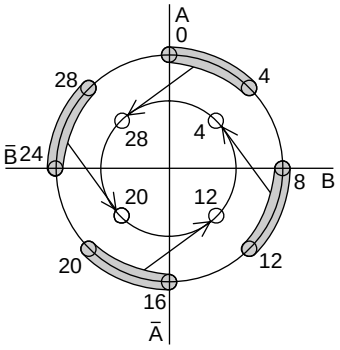
W1-2 phase → 1-2 phase



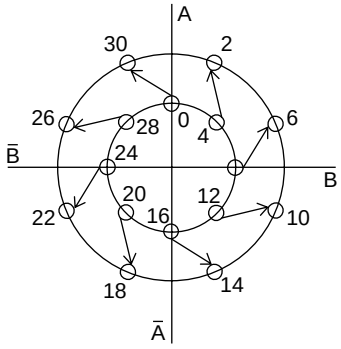
W1-2 phase → 2W1-2 phase



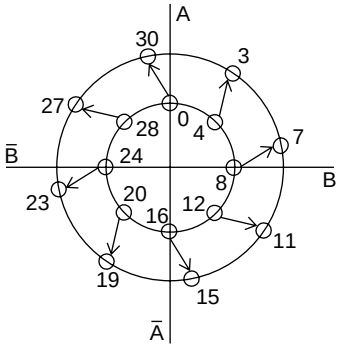
1-2 phase → 2 phase



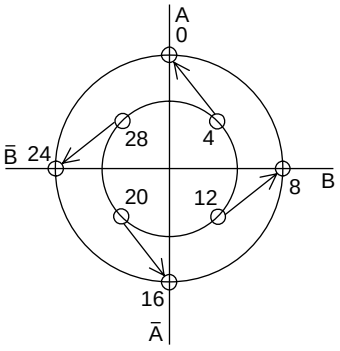
1-2 phase → W1-2 phase



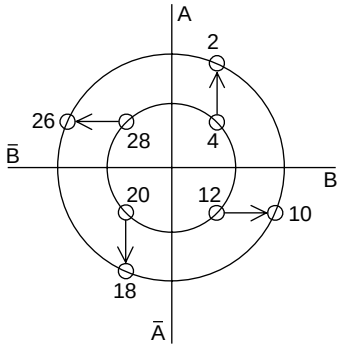
1-2 phase → 2W1-2 phase



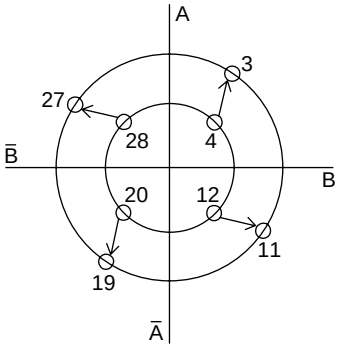
2 phase → 1-2 phase



2 phase → W1-2 phase



2 phase → 2W1-2 phase



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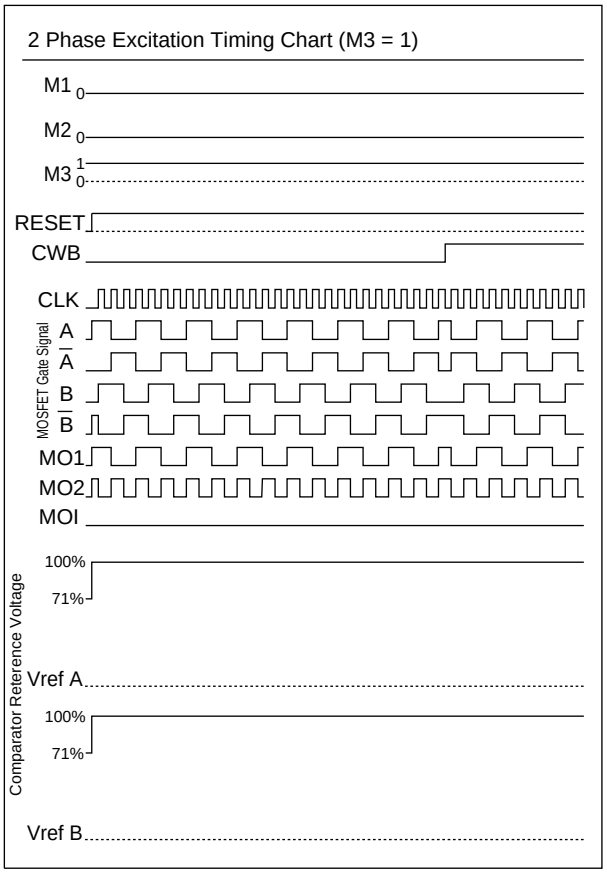
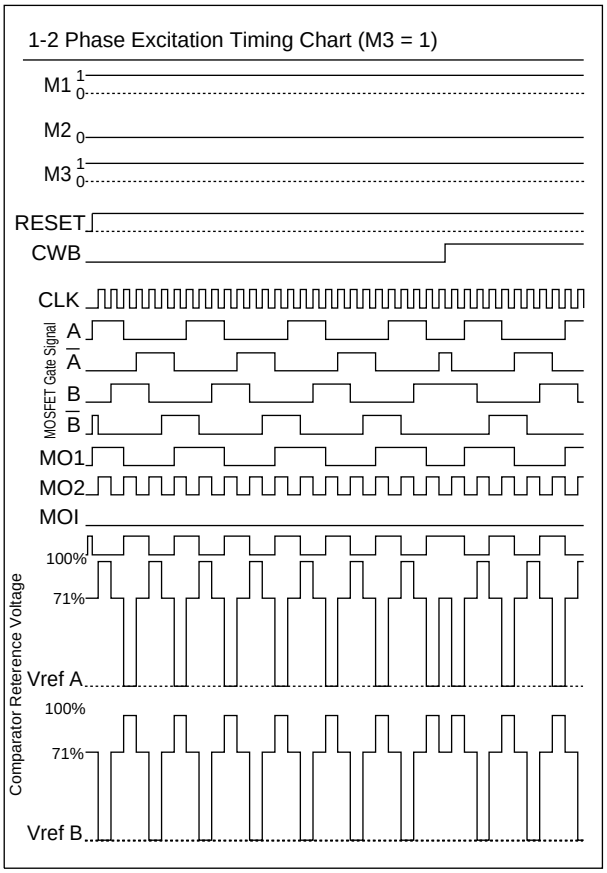
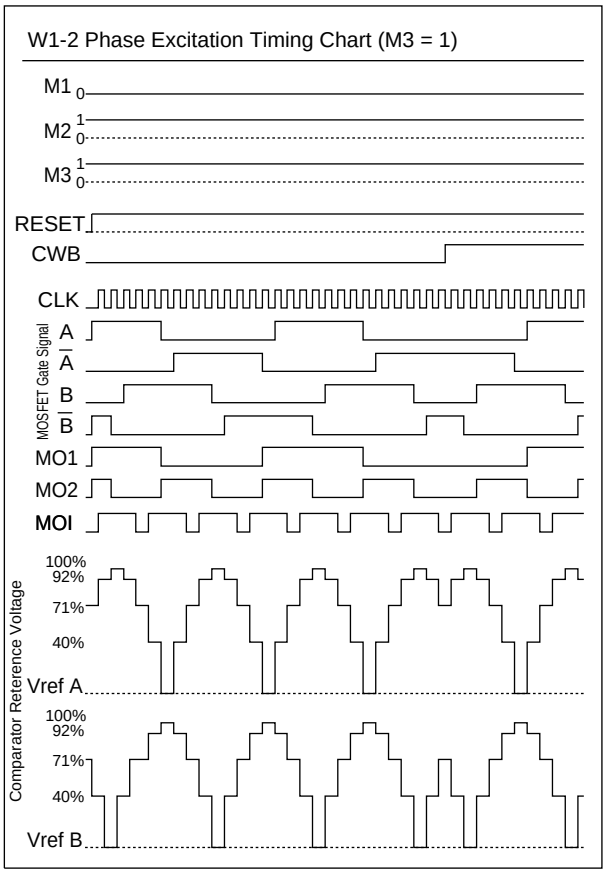
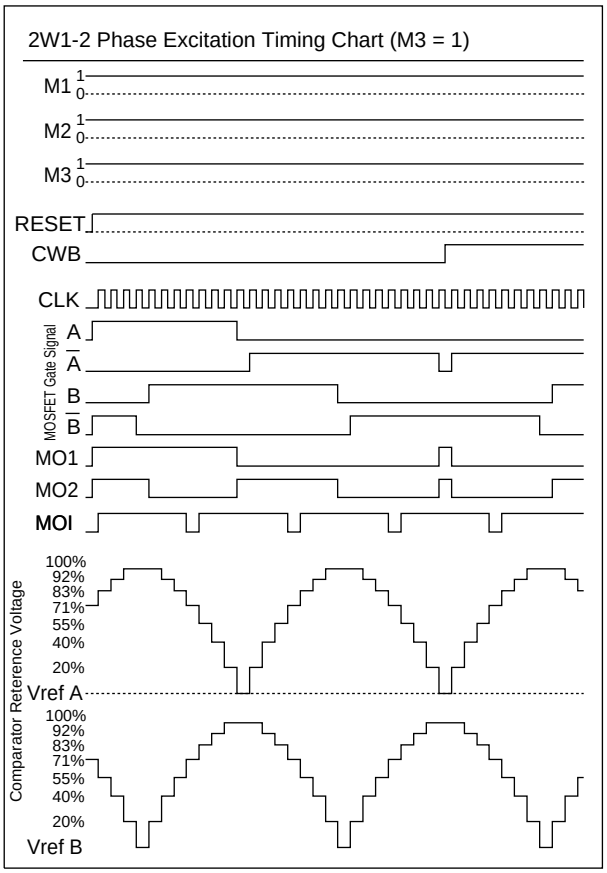
Excitation Time and Timing Charts

• CLK rising edge operation



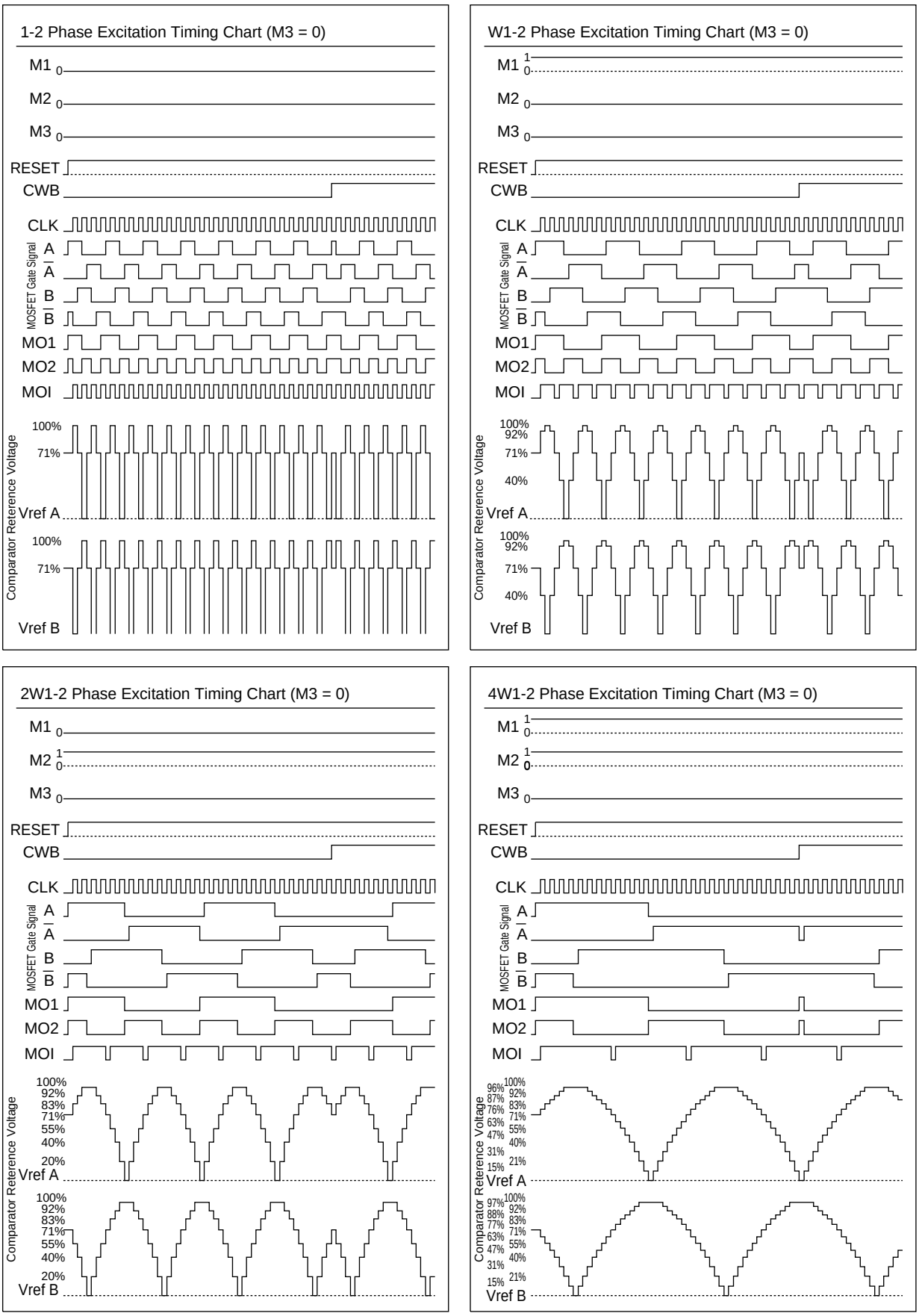






ITF02274

• CLK rising and falling edge operation



ITF02275

Thermal Design

<Hybrid IC Average Internal Power Loss Pd>

The main elements internal to this hybrid IC with large average power losses are the current control devices, the regenerative current diodes, and the current detection resistor. Since sine wave drive is used, the average power loss during microstepping drive can be approximated by applying a waveform factor of 0.64 to the square wave loss during 2 phase excitation.

The losses in the various excitation modes are as follows.

2 phase excitation $Pd_{2EX} = (Vsat+Vdf) \cdot \frac{fclock}{2} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{2} \cdot (Vsat \cdot t1+Vdf \cdot t3)$

1-2 phase excitation $Pd_{1\text{-}2EX} = 0.64 \cdot \{(Vsat+Vdf) \cdot \frac{fclock}{4} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{4} \cdot (Vsat \cdot t1+Vdf \cdot t3)\}$

W1-2 phase excitation $Pd_{W1\text{-}2EX} = 0.64 \cdot \{(Vsat+Vdf) \cdot \frac{fclock}{8} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{8} \cdot (Vsat \cdot t1+Vdf \cdot t3)\}$

2W1-2 phase excitation $Pd_{2W1\text{-}2EX} = 0.64 \cdot \{(Vsat+Vdf) \cdot \frac{fclock}{16} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{16} \cdot (Vsat \cdot t1+Vdf \cdot t3)\}$

4W1-2 phase excitation $Pd_{4W1\text{-}2EX} = 0.64 \cdot \{(Vsat+Vdf) \cdot \frac{fclock}{16} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{16} \cdot (Vsat \cdot t1+Vdf \cdot t3)\}$

Here, t1 and t3 can be determined from the same formulas for all excitation methods.

$$t1 = \frac{-L}{R+0.7} \cdot \ell n \left(1 - \frac{R+0.7}{V_{CC}1} \cdot I_{OH}\right) \qquad t3 = \frac{-L}{R} \cdot \ell n \left(\frac{V_{CC}1+0.7}{I_{OH} \cdot R + V_{CC}1+0.7}\right)$$

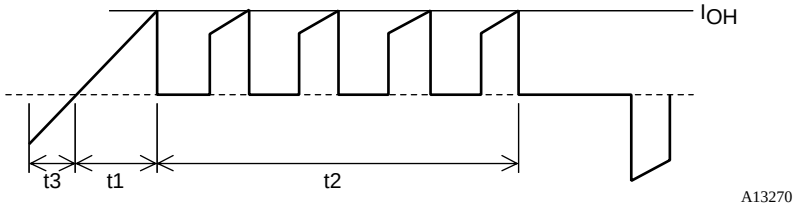
However, the formula for t2 differs with the excitation method.

2 phase excitation $t2 = \frac{2}{fclock} - (t1+t3)$

1-2 phase excitation $t2 = \frac{3}{fclock} - t1$

W1-2 phase excitation $t2 = \frac{7}{fclock} - t1$

2W1-2 phase excitation
4W1-2 phase excitation $t2 = \frac{15}{fclock} - t1$



Motor Phase Current Model Figure (2 Phase Excitation)

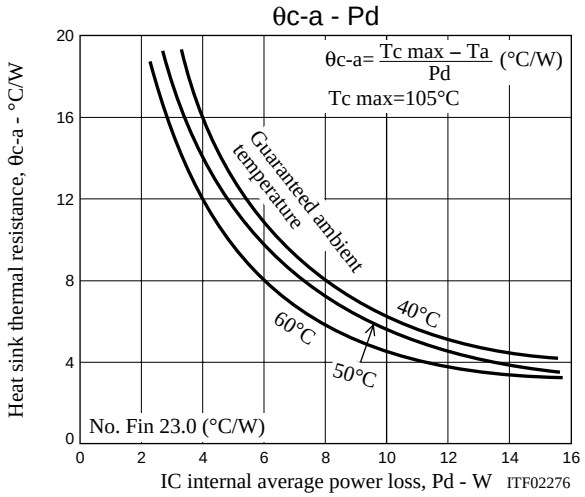
fclock : CLK input frequency (Hz)
Vsat : The voltage drop of the power MOSFET and the current detection resistor (V)
Vdf : The voltage drop of the body diode and the current detection resistor (V)
I_{OH} : Phase current peak value (A)
t1 : Phase current rise time (s)
t2 : Constant-current operating time (s)
t3 : Phase switching current regeneration time (s)
$V_{CC}1$: Supply voltage applied to the motor (V)
L : Motor inductance (H)
R : Motor winding resistance (Ω)

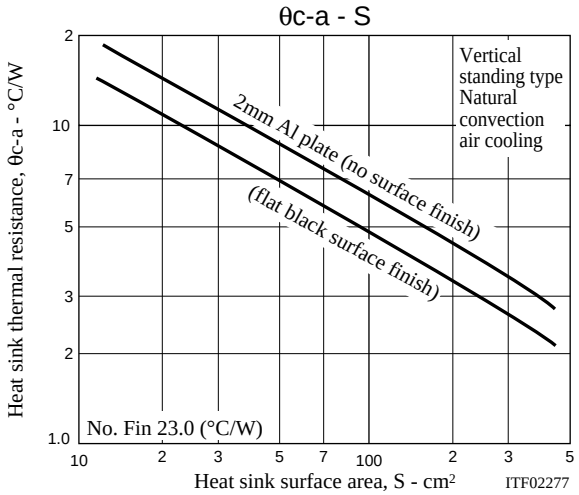
<Determining the Size of the Hybrid IC Heat Sink>
Determine θc-a for the heat sink from the average power loss determined in the previous item.

$$\theta c\text{-}a = \frac{Tc\ max - Ta}{Pd_{EX}}\ [°C/W]$$

Tc max: Hybrid IC substrate temperature (°C)
Ta: Application internal temperature (°C)
Pd_{EX}: Hybrid IC internal average loss (W)

Determine θc-a from the above formula and then size S (in cm^2) of the heat sink from the graphs shown below.
The ambient temperature of the device will vary greatly according to the air flow conditions within the application. Therefore, always verify that the size of the heat sink is adequate to assure that the Hybrid IC back surface (the aluminum plate side) will never exceed a Tc max of 105°C, whatever the operating conditions are.





Next we determine the usage conditions with no heat sink by determining the allowable hybrid IC internal average loss from the thermal resistance of the hybrid IC substrate, namely 23°C/W.

For a Tc max of 105°C at an ambient temperature of 50°C $\quad Pd_{EX} = \frac{105 - 50}{23} = 2.3W$

For a Tc max of 105°C at an ambient temperature of 40°C $\quad Pd_{EX} = \frac{105 - 40}{23} = 2.8W$

This hybrid IC can be used with no heat sink as long as it is used at operating conditions below the losses listed above. (See ΔTc – Pd curve in the graph on page 19.)

<Hybrid IC internal power element (MOSFET) junction temperature calculation>
The junction temperature, Tj, of each device can be determined from the loss Pds in each transistor and the thermal resistance θj-c.

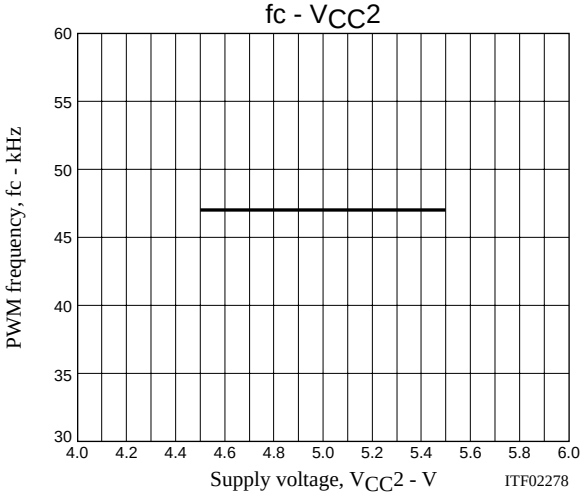
$$Tj = Tc + \theta j\text{-}c \times Pds\ (°C)$$

Here, we determine Pds, the loss for each transistor, by determining Pd_{EX} in each excitation mode.

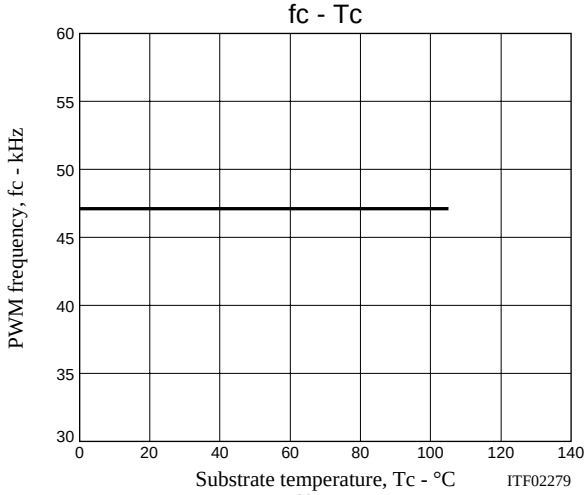
$$Pds = Pd_{EX}/4$$

The steady-state thermal resistance θj-c of a power MOSFET is 18°C/W.

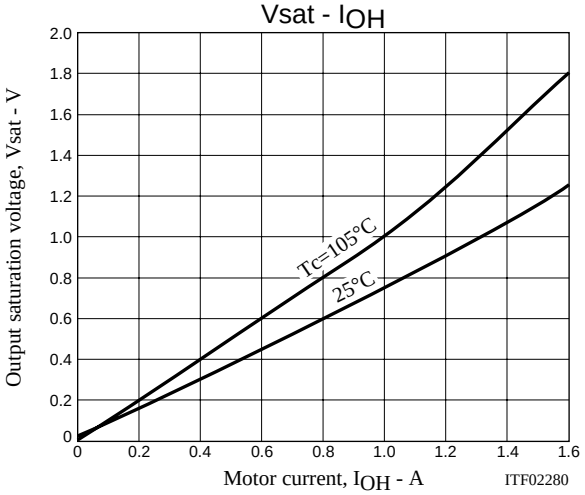
fc - $V_{CC}2$



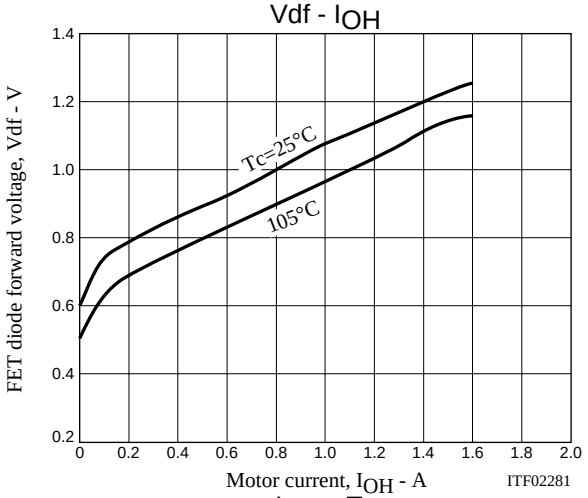
fc - Tc



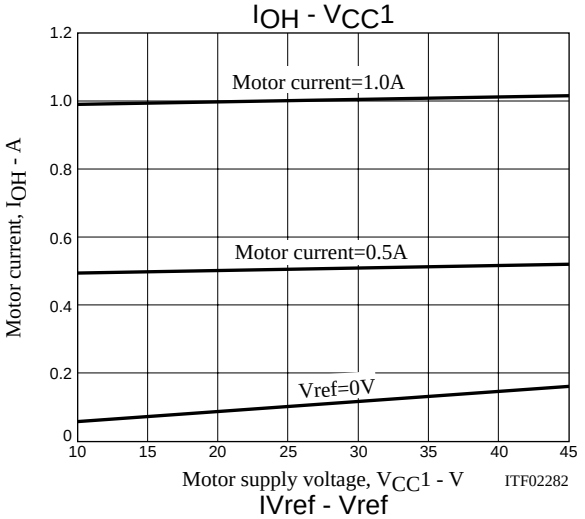
Vsat - I_{OH}



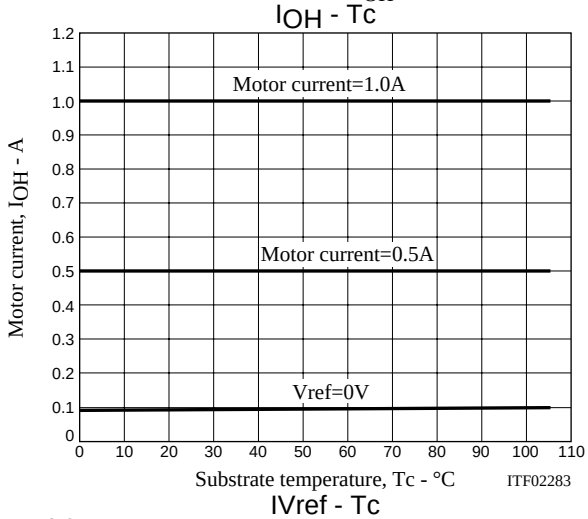
Vdf - I_{OH}



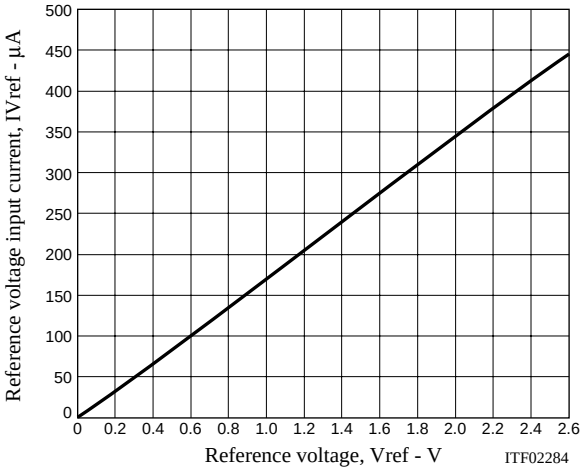
I_{OH} - $V_{CC}1$



I_{OH} - Tc



IVref - Vref



IVref - Tc