PerFET™ Power Transistor

FEATURES

- Excellent FOM
- AEC-Q101 Qualified
- Wettable Flank leads for Enhanced AOI
- 100% UIS and Rg tested
- 175°C Operating Junction Temperature
- RoHS Compliant
- Halogen-Free

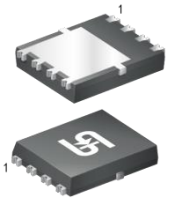
PRODUCT SUMMARY			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		40	V
$R_{DS(on)}$ (max)	V_{GS} = 10V	4.3	mΩ
	V_{GS} = 4.5V	6	
Q_g	V_{GS} = 4.5V	20	nC

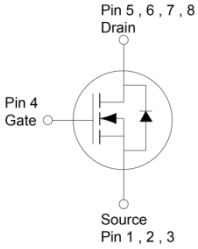
APPLICATIONS

- Automotive Applications
- Solenoid and Motor Drivers
- DC-DC Converters

Pb-Free RoHS COMPLIANT HALOGEN FREE

PDFN56U





Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±16	V
Continuous Drain Current, Silicon limited	T_C = 25°C	I_D	113	A
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	54	A
	T_C = 100°C		54	
	T_A = 25°C		20	
Pulsed Drain Current		I_{DM}	216	A
Single Pulse Avalanche Current (Note 2)		I_{AS}	25.6	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	98.3	mJ
Total Power Dissipation	T_C = 25°C	P_D	100	W
	T_C = 125°C		33	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +175	°C

THERMAL RESISTANCE			
PARAMETER	**SYMBOL**	**MAXIMUM**	**UNIT**
Thermal Resistance – Junction to Case	$R_{\Theta JC}$	1.5	°C/W
Thermal Resistance – Junction to Ambient	$R_{\Theta JA}$	50	°C/W

Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JC}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 1mA	BV_{DSS}	40	--	--	V
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(TH)}$	1.4	1.8	2.2	V
Gate-Source Leakage Current	V_{GS} = ±16V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = 40V	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance (Note 3)	V_{GS} = 10V, I_D = 27A	$R_{DS(on)}$	--	2.9	4.3	mΩ
	V_{GS} = 4.5V, I_D = 27A		--	3.7	6	
Forward Transconductance (Note 3)	V_{DS} = 10V, I_D = 7A	g_{fs}	--	83	--	S
Dynamic						
Total Gate Charge	V_{GS} = 4.5V, V_{DS} = 25V, I_D = 20A	Q_g	--	20	--	nC
Total Gate Charge	V_{GS} = 10V, V_{DS} = 25V, I_D = 20A	Q_g	--	42	--	
Gate-Source Charge		Q_{gs}	--	8	--	
Gate-Drain Charge		Q_{gd}	--	6	--	
Input Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz	C_{iss}	--	2480	--	pF
Output Capacitance		C_{oss}	--	476	--	
Reverse Transfer Capacitance		C_{rss}	--	37	--	
Gate Resistance	f = 1.0MHz	R_g	--	0.7	--	Ω
Switching (Note 4)						
Turn-On Delay Time	V_{GS} = 10V, V_{DS} = 25V, I_D = 20A, R_G = 0.7Ω	$t_{d(on)}$	--	10	--	ns
Rise Time		t_r	--	59	--	
Turn-Off Delay Time		$t_{d(off)}$	--	27	--	
Fall Time		t_f	--	13	--	
Source-Drain Diode						
Diode Forward Voltage (Note 3)	V_{GS} = 0V, I_S = 27A	V_{SD}	--	--	1.1	V
Reverse Recovery Time	I_S = 20A, di/dt = 100A/μs	t_{rr}	--	37	--	ns
Reverse Recovery Charge		Q_{rr}	--	31	--	nC

Notes:
1. Package current limit.
2. L = 0.3mH, V_{GS} = 10V, R_G = 25Ω, Starting T_J = 25°C.
3. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
4. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

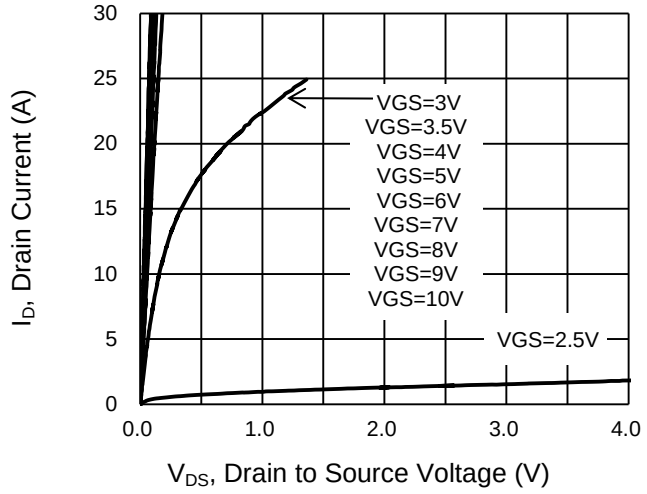
ORDERING CODE	PACKAGE	PACKING
TQM043NH04LCR RLG	PDFN56U	2,500pcs / 13” Reel
TQM043NH04LCR-V RLG	PDFN56U	2,500pcs / 13” Reel

Notes:
V：Hot test.

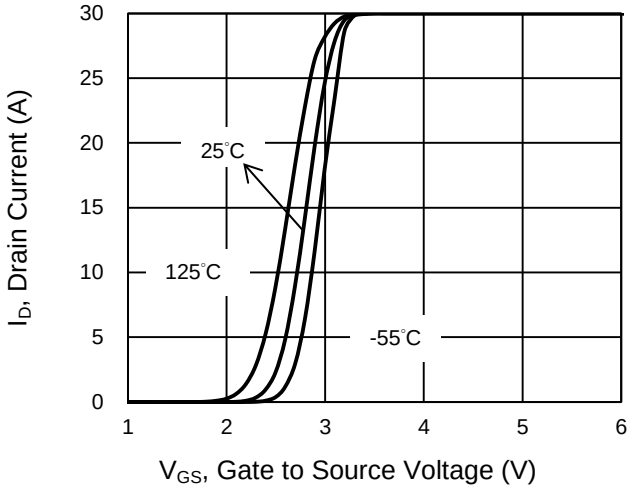
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

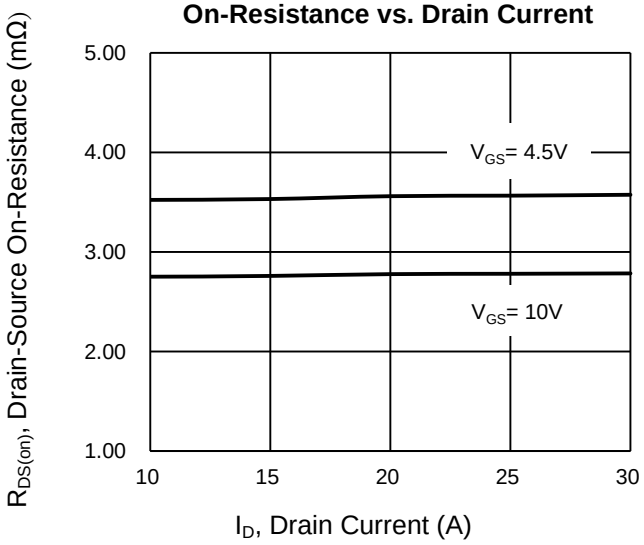
Output Characteristics



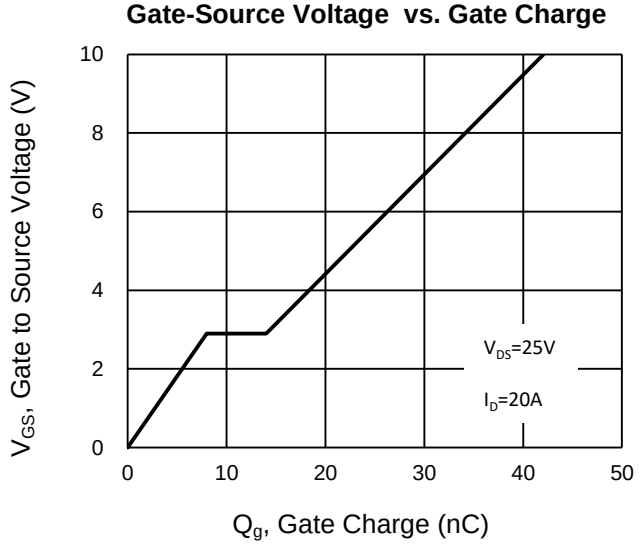
Transfer Characteristics



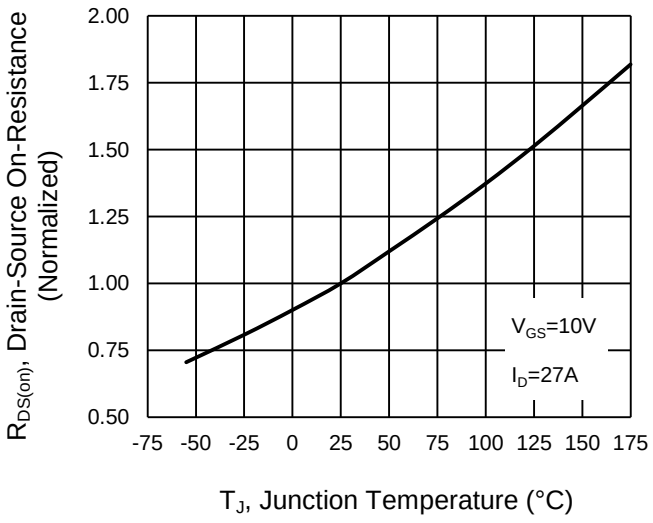
On-Resistance vs. Drain Current



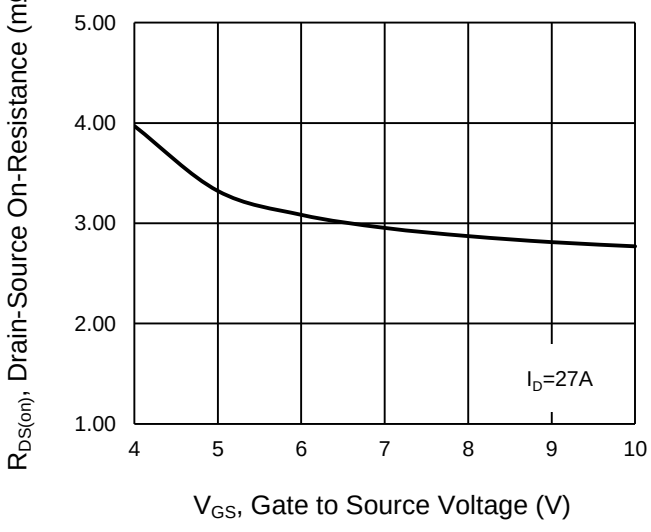
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



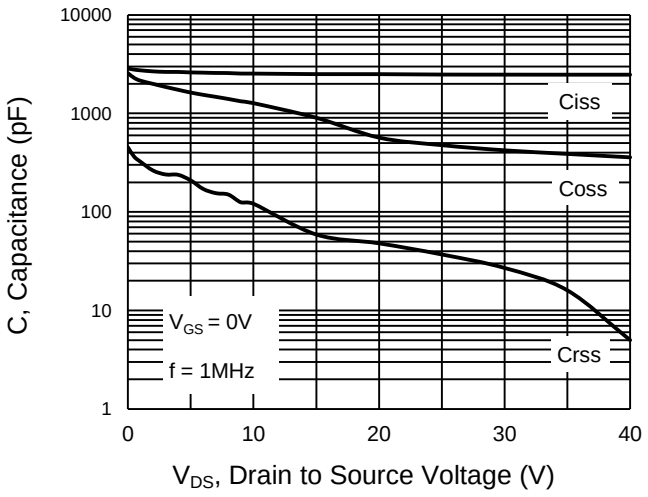
On-Resistance vs. Gate-Source Voltage



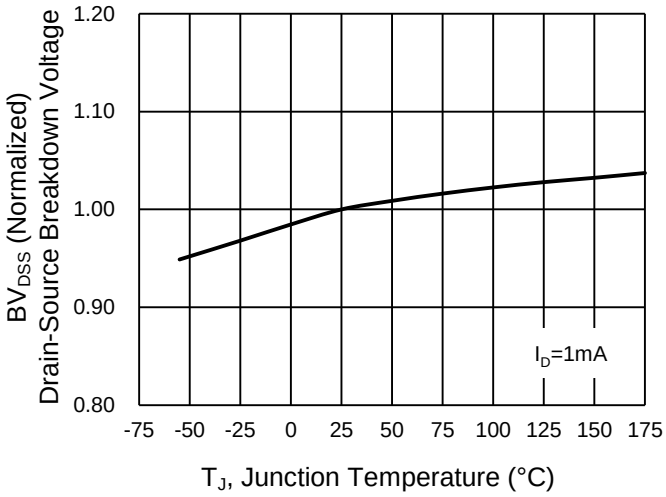
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

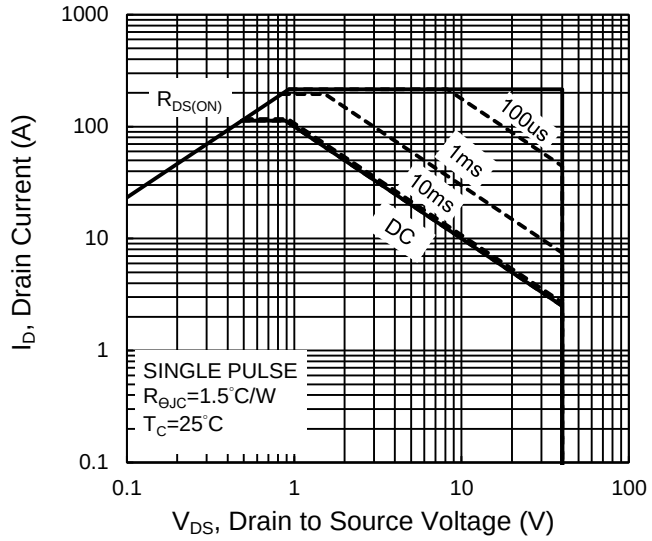
Capacitance vs. Drain-Source Voltage



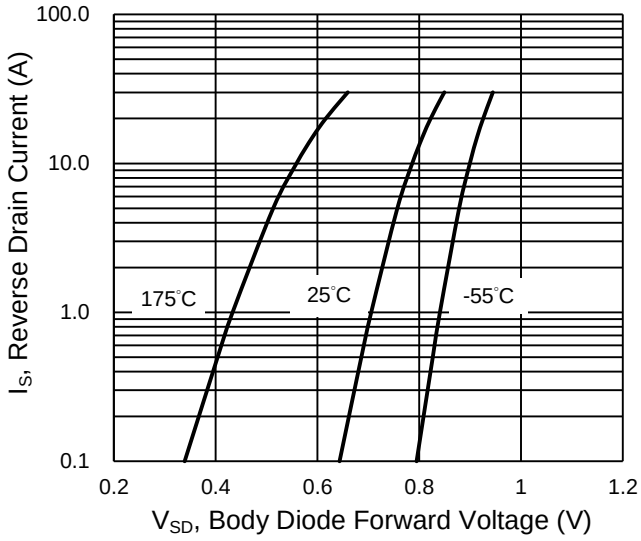
BV_{DSS} vs. Junction Temperature



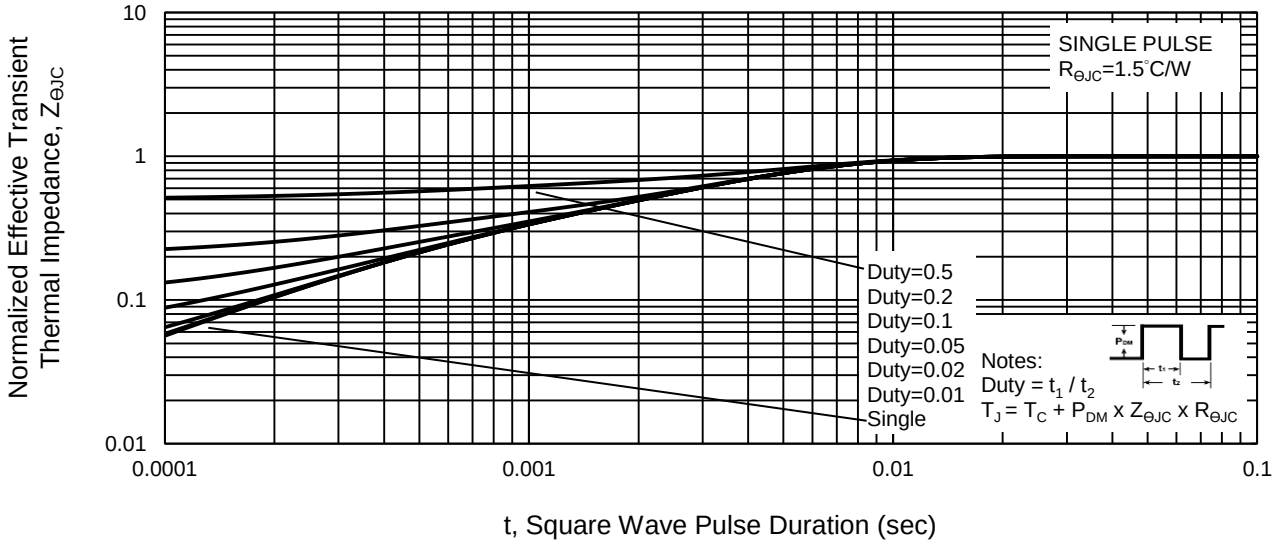
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



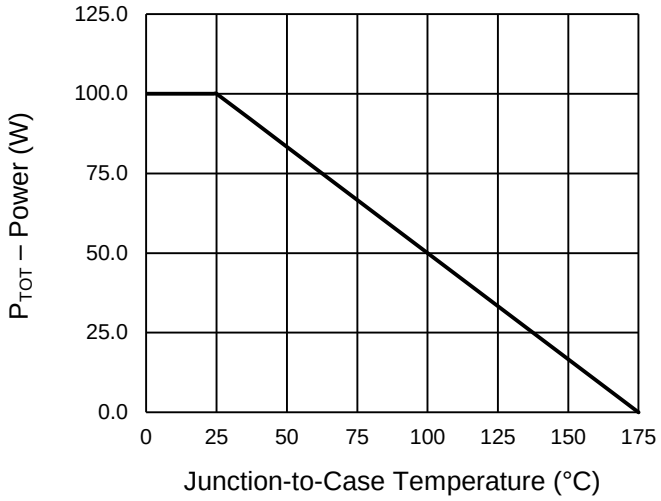
Normalized Thermal Transient Impedance, Junction-to-Case



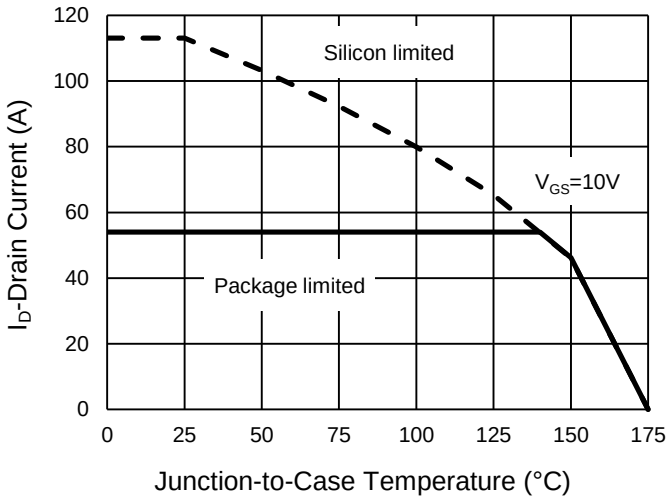
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

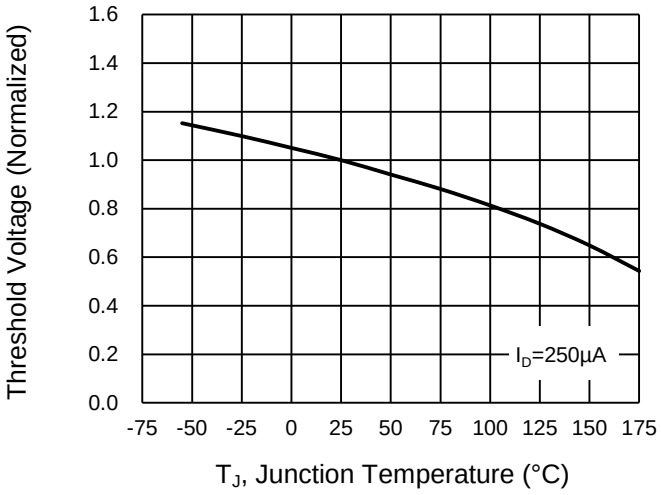
Power Dissipation



Drain Current

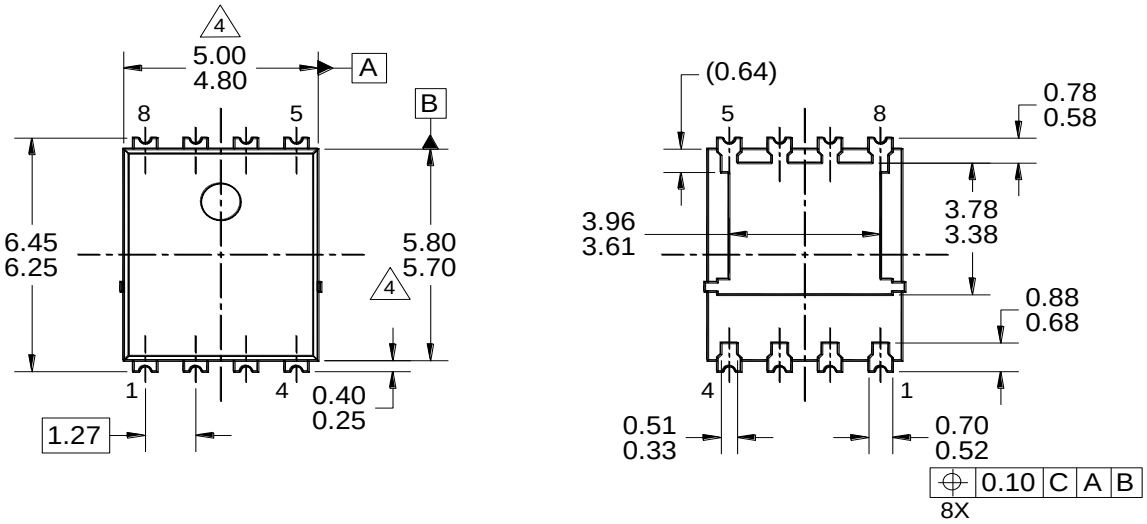


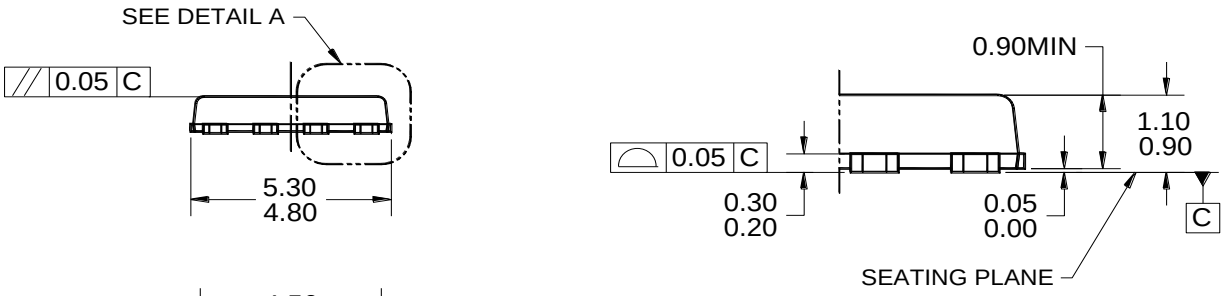
Normalized gate threshold voltage vs Temperature



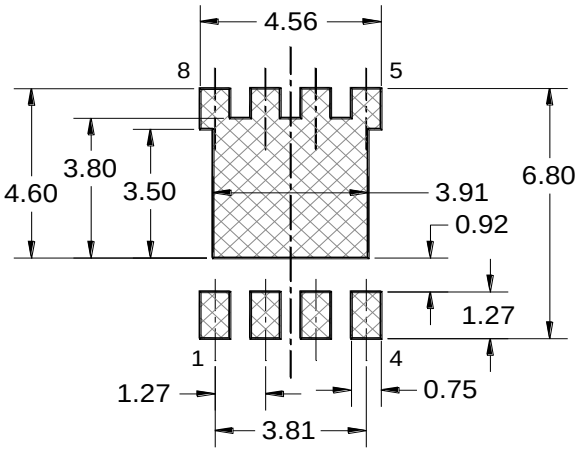
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56U

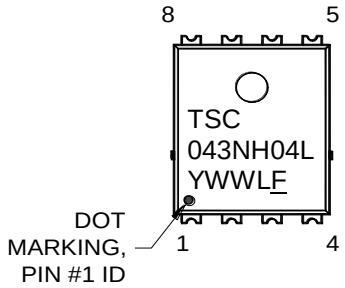




DETAIL A
(SCALE 2:1)



SUGGESTED PAD LAYOUT



MARKING DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEITA ED-7500B, EIAJ SC-111BB.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-PDFN56U-023 REV A.

P/N	=	MARKING CODE
Y	=	YEAR CODE
WW	=	WEEK CODE (01~52)
L	=	LOT CODE (1~9, A~Z)
F	=	FACTORY CODE
_	=	AEC-Q101 QUALIFIED

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