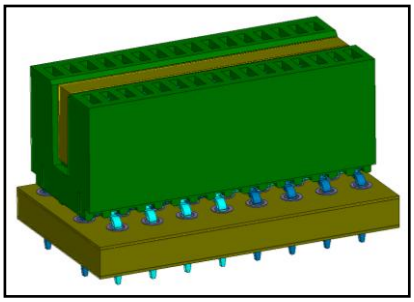
ELECTRICAL MODEL DOCUMENTATION

MODEL DESCRIPTION



This is an s-parameter model for DDR4 vertical through-hole DIMM mated connector.

Main board includes through-hole drilled vias of 0.762mm diameter on 1.4mm thick board and includes 1.27mm of microstrip with width of 6.5 mils. Anti-pad diameter is 1.2192mm.

Module card includes edge finger size of 2.3mm X 0.6mm on 1.4 mm thick board and includes 1.27mm of microstrip with width of 6.5 mils. All internal ground layers are 100% recessed underneath gold-fingers.

Both main and module board have 4 layers and a dielectric constant of 4.4 was used for the modeled board material.

APPLICABLE SERIES NUMBER:

78726

MODEL FILENAME: SP-78726-002_revA.s24p	**MODEL FORMAT:** Touchstone (*.sNp)
MODEL TYPE: S-parameter	**DATA FORMAT:** Magnitude/Phase
MODEL BASIS: Analytical 3D Field Solution	**MODEL SOURCE:** Ansys HFSS ver. 15.0.0
BANDWIDTH: DC – 15 GHz	**RESOLUTION:** 10 MHz Steps
REFERENCE: 50 ohms	**NUMBER OF POINTS:** 1501 (1500 + 1 DC)
NUMBER OF PORTS : 24 Single-Ended	**VALIDATION:** No

TERMINAL TO MODEL PORT MAPPING TABLE

AVAILABLE MODEL SIGNAL PATHS

TERMINAL	INPUT PORT (MAIN BOARD SIDE)	DESCRIPTION	OUTPUT PORT (MODULE BOARD SIDE)	DESCRIPTION
Front Side Outer Row P2	1	in_F1	13	out_F1
Front Side Outer Row P4	2	in_F2	14	out_F2
Front Side Outer Row P6	3	in_F3	15	out_F3
Front Side Outer Row P8	4	in_F4	16	out_F4
Front Side Inner Row P9	5	in_F5	17	out_F5
Front Side Inner Row P11	6	in_F6	18	out_F6
Front Side Inner Row P13	7	in_F7	19	out_F7
Front Side Inner Row P15	8	in_F8	20	out_F8
Back Side Inner Row P150	9	in_B1	21	out_B1
Back Side Inner Row P152	10	in_B2	22	out_B2
Back Side Inner Row P154	11	in_B3	23	out_B3
Back Side Inner Row P156	12	in_B4	24	out_B4

PRE-DEFINED MODEL RETURN PATHS

TERMINAL	DESCRIPTION
Front Side Inner Row P1	G
Front Side Inner Row P3	G
Front Side Inner Row P5	G
Front Side Inner Row P7	G
Front Side Outer Row P10	G
Front Side Outer Row P12	G
Front Side Outer Row P14	G
Front Side Outer Row P16	G

TERMINAL	DESCRIPTION
Back Side Outer Row P143	G
Back Side Inner Row P144	G
Back Side Outer Row P145	G
Back Side Inner Row P146	G
Back Side Outer Row P147	G
Back Side Inner Row P148	G
Back Side Outer Row P149	G
Back Side Outer Row P151	G
Back Side Outer Row P153	G
Back Side Outer Row P155	G
Back Side Outer Row P157	G
Back Side Inner Row P158	G

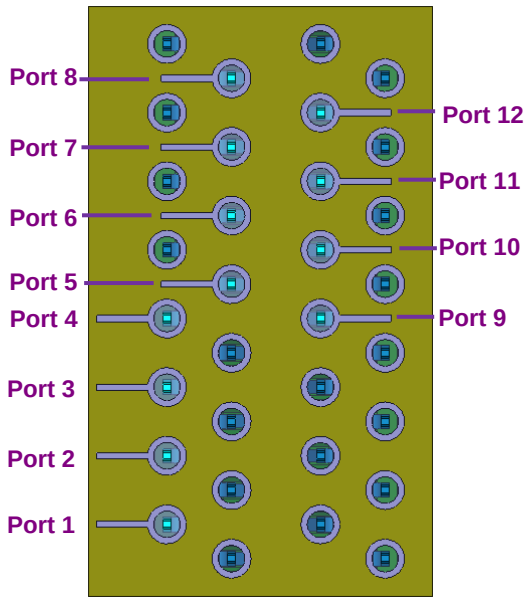
REFERENCE LAYER STACK

MAIN BOARD & MODULE CARD LAYER STACK

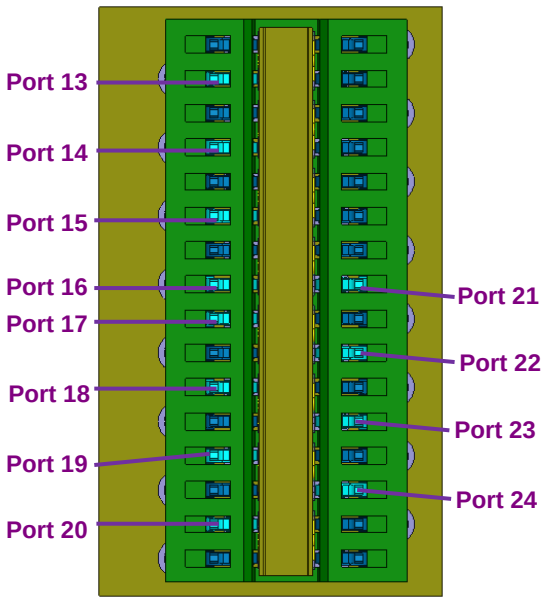
		Thickness (mm)
Signal	Layer 1	0.04
	FR4	0.102
Ground	Layer 2	0.03
	FR4	1.056
Ground	Layer 3	0.03
	FR4	0.102
Signal	Layer 4	0.04
	Total	1.40

PART ILLUSTRATIONS

Main Board (Bottom View)

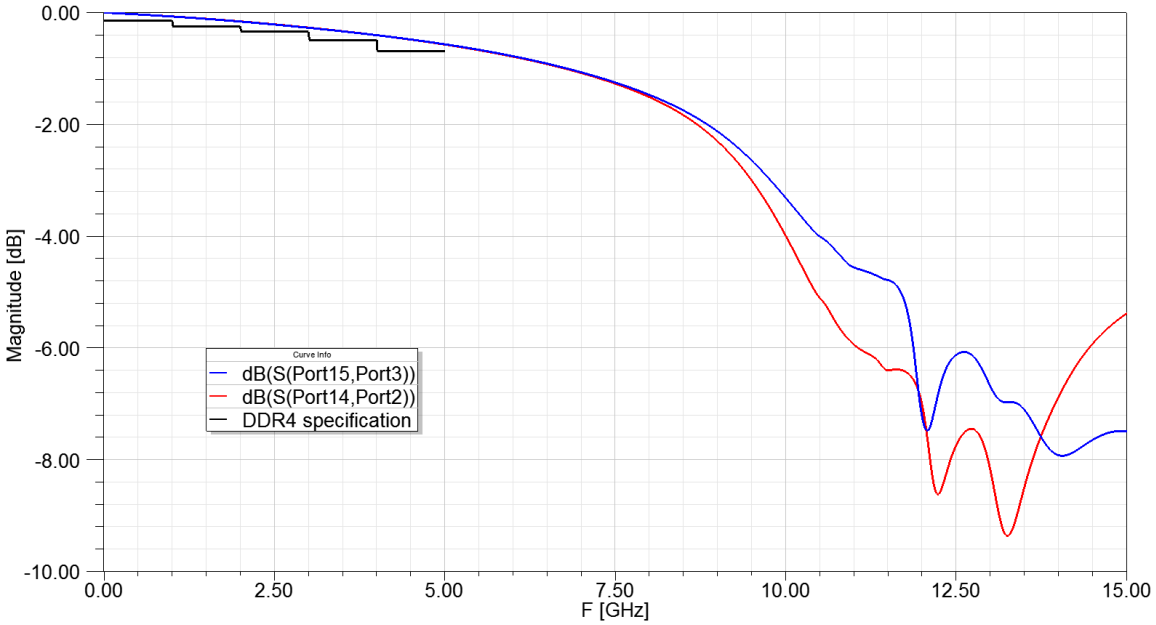


Connector (Top View)

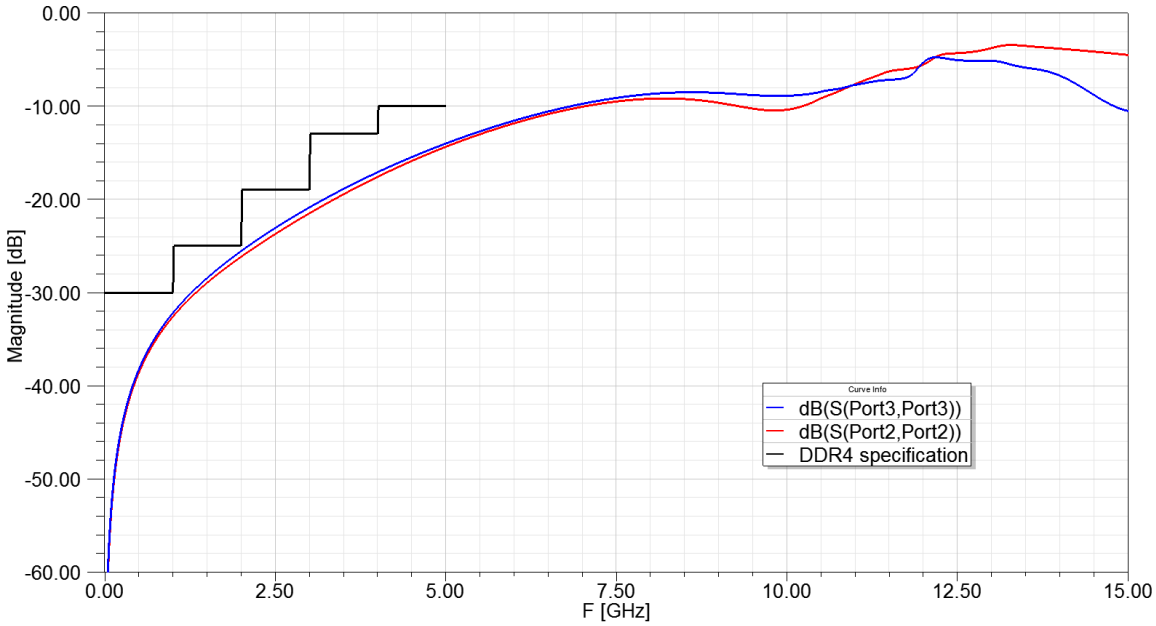


REFERENCE RESULTS

Frequency Domain: Insertion Loss



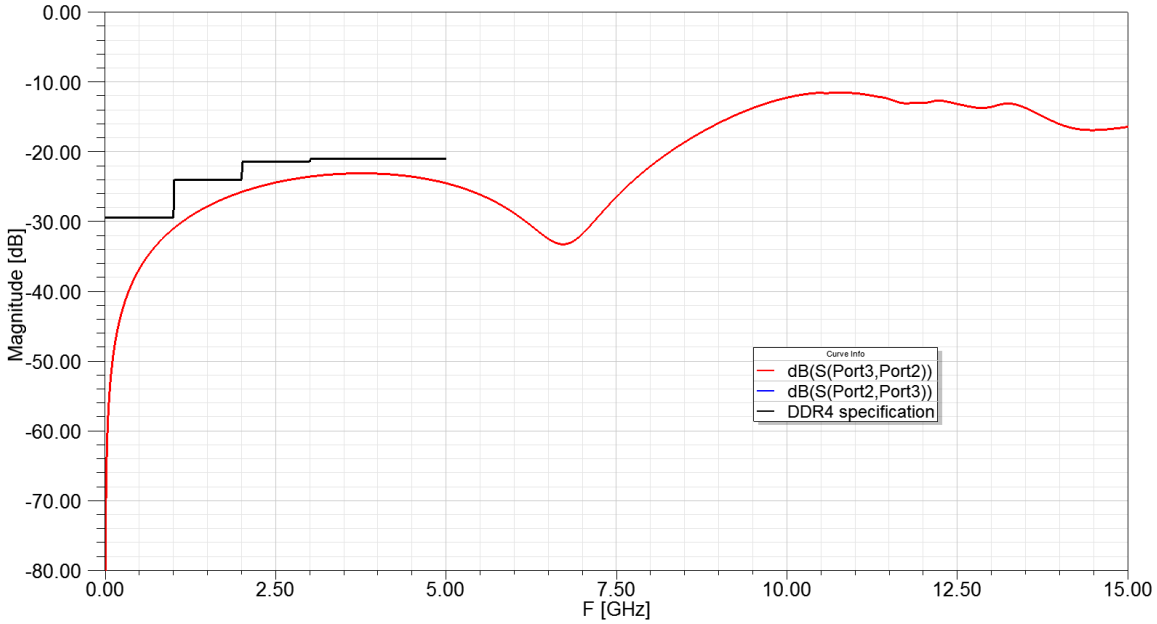
Frequency Domain: Return Loss



REFERENCE RESULTS

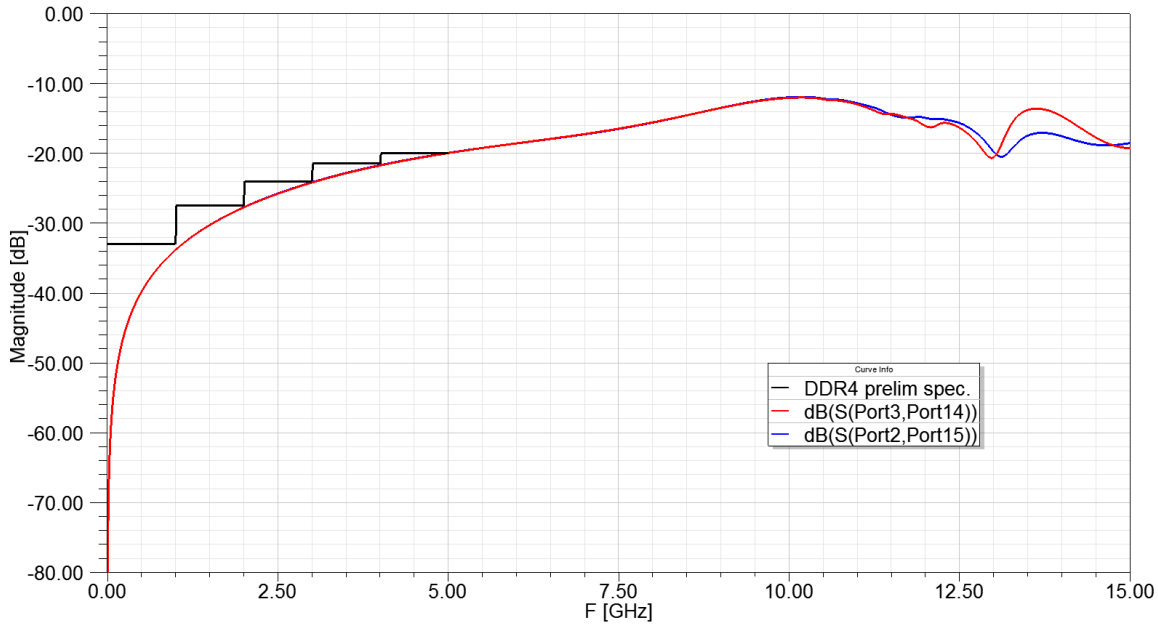
Frequency Domain: Near End Crosstalk

- 1:1 S/G ratio
- Both victim and aggressor located at outer row



Frequency Domain: Far End Crosstalk

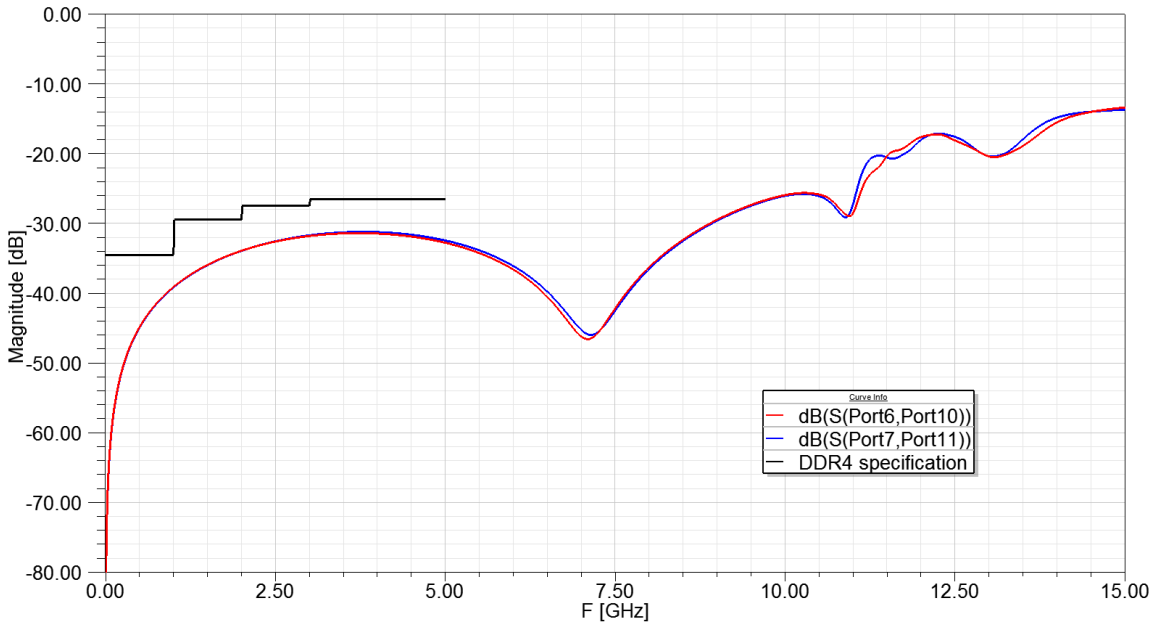
- 1:1 S/G ratio
- Both victim and aggressor located at outer row



REFERENCE RESULTS

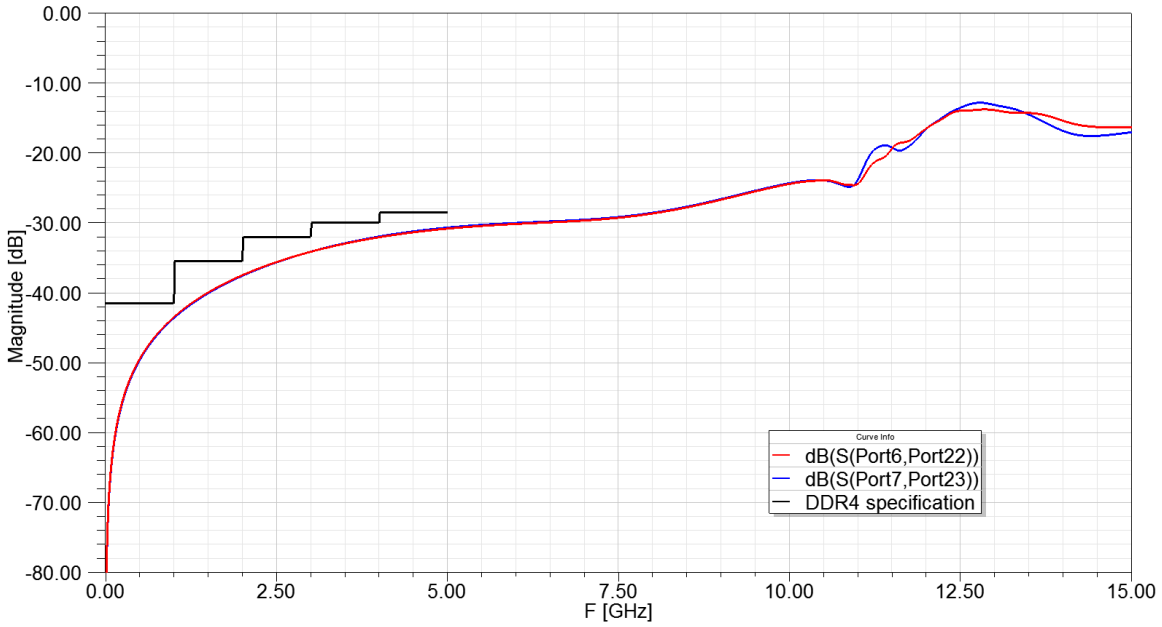
Frequency Domain: Near End Crosstalk

- 1:1 S/G ratio
- Victim locates at inner row from front side
- Aggressor locates at inner row from back side.



Frequency Domain: Far End Crosstalk

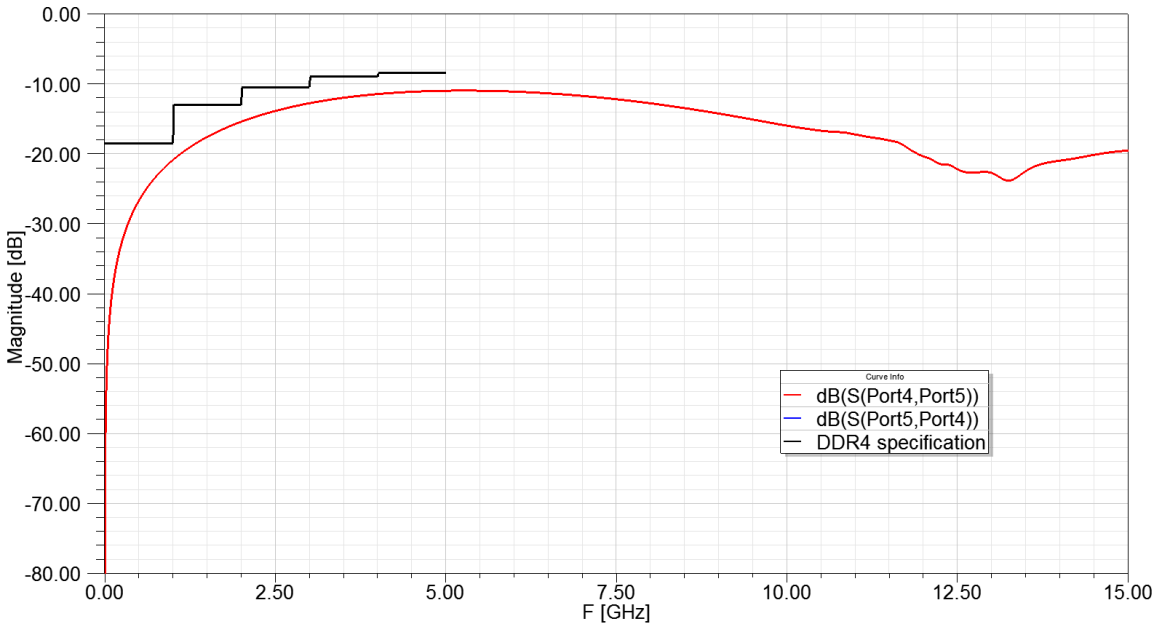
- 1:1 S/G ratio
- Victim locates at inner row from front side
- Aggressor locates at inner row from back side.



REFERENCE RESULTS

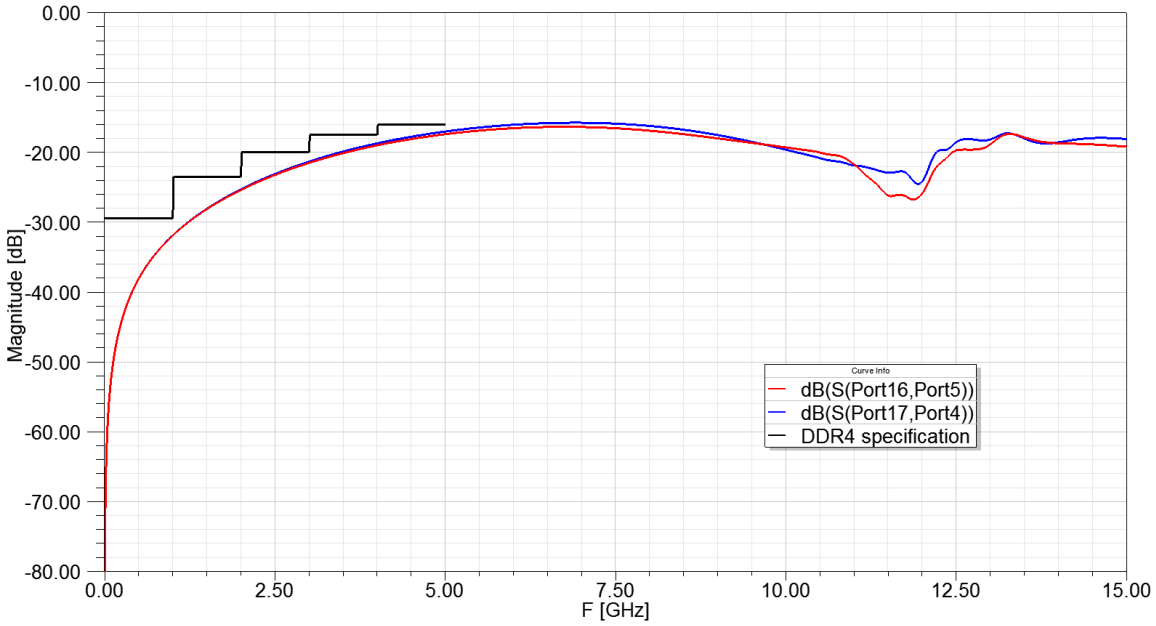
Frequency Domain: Near End Crosstalk

- 2:1 S/G ratio



Frequency Domain: Far End Crosstalk

- 2:1 S/G ratio



REFERENCE RESULTS

Time Domain: TDR Impedance

- Rise-time of 100ps [10%~90%] at connector launch