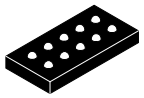
Auto Focus (AF) Controller & Driver

LC898217XC



WLCSP10, 1.04x2.04
CASE 567LF

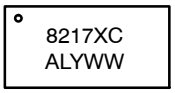
Overview

LC898217XC is an AF control LSI. It consists of 1 system of feedback circuit for AF control.

Features

- Built−in Equalizer Circuit Using Digital Operation
  - AF Control Equalizer Circuit
  - Any Coefficient can be Specified by 2−wire Serial I/F (TWIF)
- 2−wire Serial Interface
  (The Communication Protocol is Compatible with I^2C)
- Built−in A/D Converter
  - Input 1 Channel
- Built−in D/A Converter
  - Output 2 Channel (Hall Offset, Constant Current Bias)
- Built−in VGA
  - Hall Amp
  - 1 Channel
- Built−in EEPROM
  - 128 Byte (16 Byte/Page)
- Built−in OSC
- Built−in Constant Current Driver
  - 110 mA
  - 1 Channel
- Package
  - WLCSP 10−pin
- Supply Voltage
  - V_{DD} (2.6 V to 3.3 V)
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant

MARKING DIAGRAM



8217XC = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
LC898217XC−MH	WLCSP10	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PIN DESCRIPTION

Table 1. PIN DESCRIPTION

Pin Name	Description
I	Input
P	Power Supply, GND
NC	Not Connect
O	Output
B	Bidirection

- 2−wire serial interface
  - SCL I 2−wire serial interface clock pin
  - SDA B 2−wire serial interface data pin
- Hall interface
  - BIASO O D/A output (to Hall element)
  - OPINP I VGA input (from Hall element)
  - OPINM I VGA input (from Hall element)
- Driver interface
  - OUT1 O Driver output (to Actuator)
  - OUT2 O Driver output (to Actuator)
- Power supply pin
  - V_{DD} P Power Supply
  - V_{SS} P GND
- Test pin
  - PORT B Analog test signal input/output
    Convergence detection monitor output
    VSYNC input

**Process when pins are not used*

PIN TYPE “O” – Ensure that it is set to OPEN.

PIN TYPE “I” – OPEN is inhibited. Ensure that it is connected to the V_{DD} or V_{SS} even when it is unused. (Please contact **onsemi** for more information about selection of V_{DD} or V_{SS}.)

PIN TYPE “B” – If you are unsure about processing method on the pin description of pin layout table, please contact us.

Note that incorrect processing of unused pins may result in defects.

**In case of connecting PORT pin with HOST CPU*

When LC898217XC is power off and HOST CPU is power on, a HOST CPU pin connected with PORT pin have to be fixed “L” level.

PIN LAYOUT

Table 2. PIN LAYOUT

Circuit Name	Number of PINs	Circuit Name	Number of PINs
Analog	4	Driver	2
Logic	2	Power	2

"PORT" pin has analog function and digital function.

	A	B
1	OUT2	OUT1
2	VSS	VDD
3	PORT	SCL
4	BIASO	SDA
5	OPINM	OPINP

BOTTOM VIEW

Figure 1. Pin Layout

BLOCK DIAGRAM

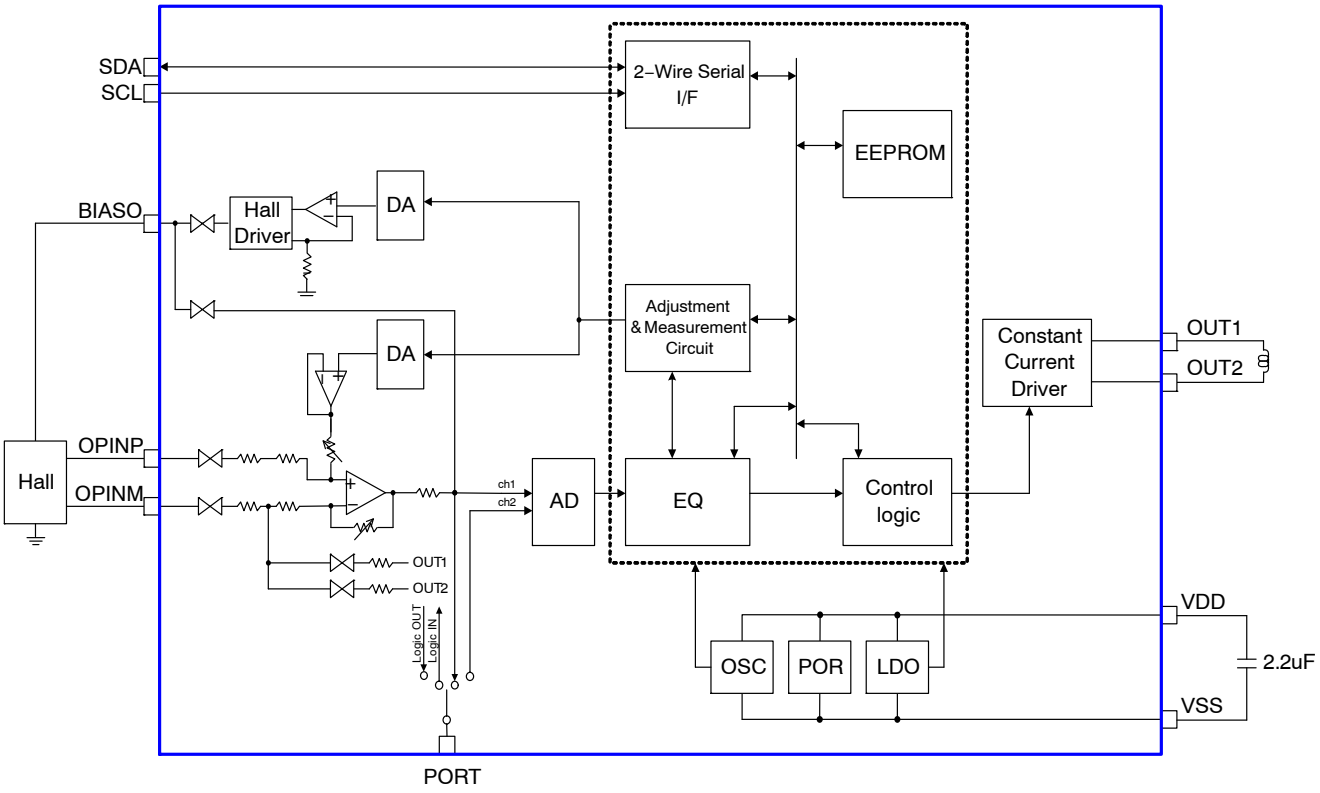


Figure 2. Block Diagram

ELECTRICAL CHARACTERISTICS

Table 3. ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

Symbol	Item	Condition	Rating	Unit
$V_{DD}33$ max	Supply voltage	Ta ≤ 25°C	−0.3 to 4.6	V
V_I33, V_O33	Input/output voltage	Ta ≤ 25°C	−0.3 to $V_{DD}33$ + 0.3	V
Tstg	Storage ambient temperature		−55 to 125	°C
Topr	Operating ambient temperature		−30 to 70	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. ALLOWABLE OPERATING RATINGS (Ta = −30 to 70°C, VSS = 0 V, 3 V power supply (V_{DD}))

Symbol	Item	Min	Typ	Max	Unit
$V_{DD}33$	Supply voltage	2.6	2.8	3.3	V
V_{IN}	Input voltage range	0		$V_{DD}33$	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. DC CHARACTERISTICS (Input / output level at V_{SS} = 0 V, V_{DD} = 2.6 to 3.6 V, Ta = −30 to 70°C)

Symbol	Item	Condition	Min	Typ	Max	Unit	Applicable Pins
V_{IH}	High−level input voltage	CMOS compliant Schmitt	1.4			V	SCL, SDA, PORT
V_{IL}	Low−level input voltage				0.4	V	
V_{OH}	High−level output voltage	IOH = −2 mA	V_{DD}−0.4			V	PORT
V_{OL}	Low−level output voltage	IOL = 2 mA			0.4	V	SDA, PORT
Rdn	Pulldown resistor		50		220	kΩ	PORT

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 6. DRIVER OUTPUT (OUT1, OUT2) (V_{SS} = 0 V, V_{DD} = 2.8 V, Ta = 25°C)

Symbol	Item	Condition	Min	Typ	Max	Unit	Applicable Pins
Ifull	Maximum current		105		115	mA	OUT1, OUT2
Ioleak	Output leak current			1		μA	

Table 7. NON−VOLATILE MEMORY CHARACTERISTICS

Symbol	Item	Condition	Min	Typ	Max	Unit	Applicable Circuit
EN	Endurance				1000	Cycles	EEPROM
RT	Data retention		10			Years	
tWT	Write time				20	ms	

AC CHARACTERISTICS

V_{DD} Supply Timing

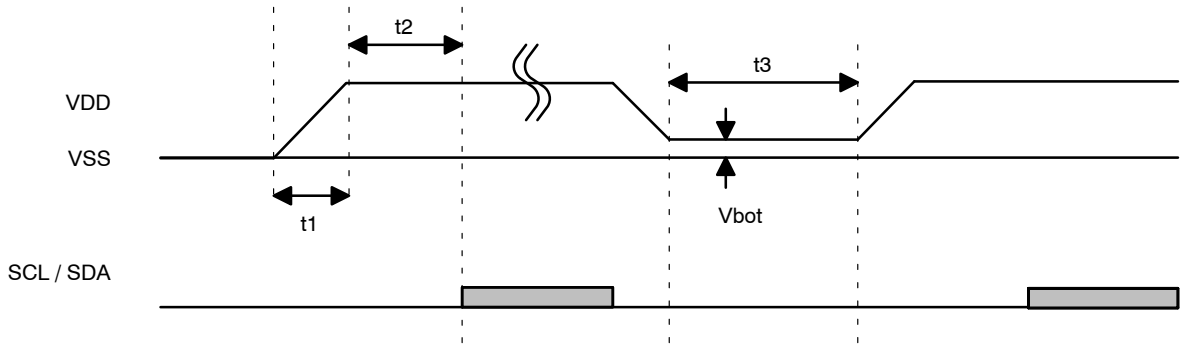


Figure 3. V_{DD} Supply Timing

It is available to use 2−wire serial interface 5 ms later for Power On Reset of V_{DD}.

Table 8. VDD SUPPLY TIMING

Symbol	Item	Min	Typ	Max	Unit
t1	V_{DD} turn on time			3	ms
t2	2−wire serial interface start time from V_{DD} on	5			ms
t3	V_{DD} off time	100			ms
Vbot	Bottom Voltage			0.1	V

AC Specification

Figure 4 shows interface timing definition and Table 9 shows electric characteristics.

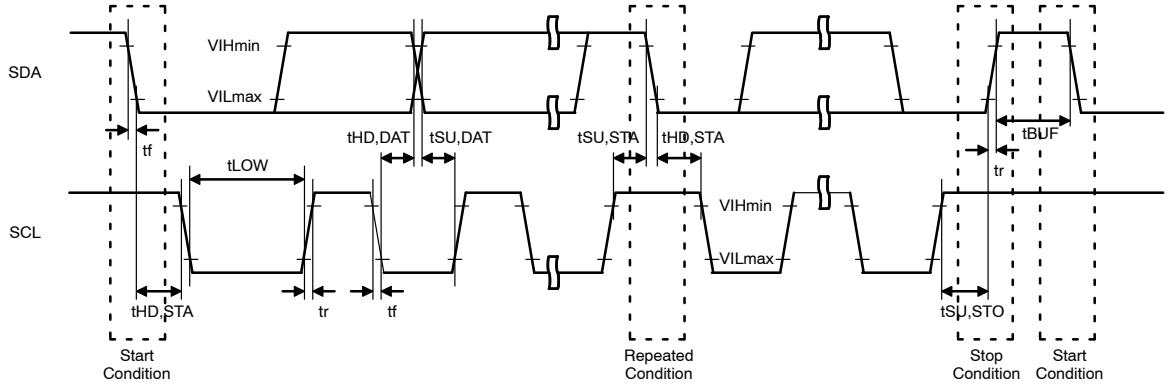


Figure 4. 2−wire Serial Interface Timing Definition

Table 9. ELECTRICAL CHARACTERISTICS FOR 2−WIRE SERIAL INTERFACE (AC CHARACTERISTICS)

Symbol	Item	Pin Name	Fast−mode			Fast−mode Plus			Unit
			Min	Typ	Max	Min	Typ	Max	
FSCL	SCL clock frequency	SCL			400			1000	kHz
tHD,STA	START condition hold time	SCL SDA	0.6			0.26			μs
tLOW	SCL clock Low period	SCL	1.3			0.5			μs
tHIGH	SCL clock High period	SCL	0.6			0.26			μs
tSU,STA	Setup time for repetition START condition	SCL SDA	0.6			0.26			μs
tHD,DAT	Data hold time	SCL SDA	0 (Note 1)		0.9	0 (Note 1)			μs
tSU,DAT	Data setup time	SCL SDA	100			50			ns
tr	SDA, SCL rising time	SCL SDA			300			120	ns
tf	SDA, SCL falling time	SCL SDA			300			120	ns
tSU,STO	STOP condition setup time	SCL SDA	0.6			0.26			μs
tBUF	Bus free time between STOP and START	SCL SDA	1.3			0.5			μs

1. LC898217XC is designed for a condition with typ. 20 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

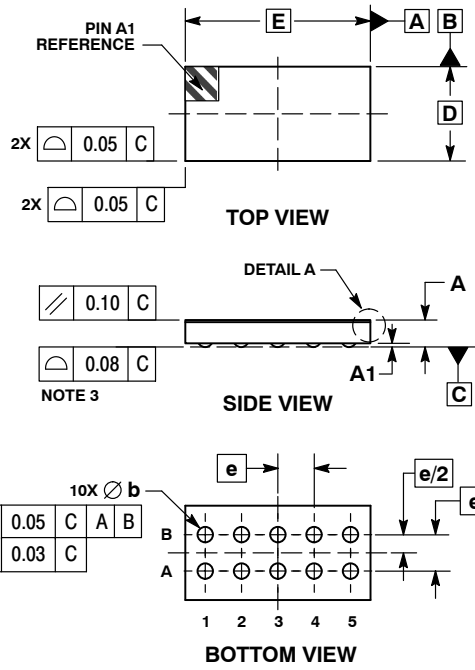
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

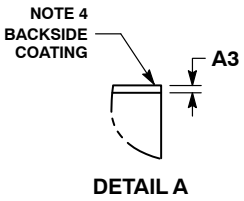
ON Semiconductor®

SCALE 4:1

WLCSP10, 1.04x2.04
CASE 567LF
ISSUE B

DATE 03 JUN 2015

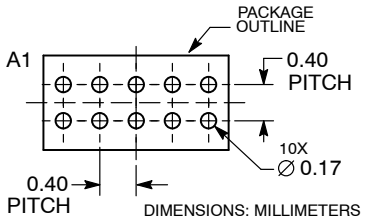




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. BACKSIDE COATING IS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	0.27	0.33
A1	0.04 REF	
A3	0.025 REF	
b	0.12	0.22
D	1.04 BSC	
E	2.04 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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