PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/14/8339
Dated 17 Feb 2014

ADDENDUM to PCN 8202

Table 1. Change Implementation Schedule

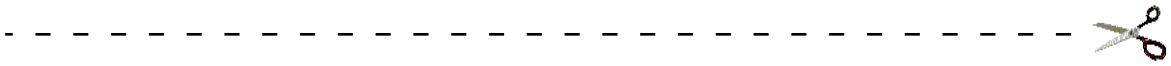
Forecasted implementation date for change	10-Feb-2014
Forecasted availability date of samples for customer	21-Mar-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	10-Feb-2014
Estimated date of changed product first shipment	19-May-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	M93C46, M93C56, M93C66, M93C76, M93C86 products
Type of change	Waferfab technology change
Reason for change	Line up to state-of-the-art of process
Description of the change	Redesign and upgrade to the new CMOSF8H Process technology.
Change Product Identification	Process Technology identifier "K"
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MMS-MMY/14/8339**
Please sign and return to STMicroelectronics Sales Office	**Dated 17 Feb 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Leduc, Hubert	Marketing Manager
Rodrigues, Benoit	Product Manager
Pavano, Rita	Q.A. Manager

ADDENDUM TO PCN 8202

M93C46, M93C56, M93C66, M93C76, M93C86,
1-Kbit, 2-Kbit, 4-Kbit, 8-Kbit, 16-Kbit
MICROWIRE serial access EEPROM / Industrial grade
Redesign and upgrade to the CMOSF8H process technology

What is the purpose of this addendum?

The purpose of this addendum is to add M93C76-RDW6TP to the list of the concerned commercial part numbers (was missing when generating MMS-MMY138202 PCN).

PRODUCT / PROCESS CHANGE NOTIFICATION

M93C46, M93C56, M93C66, M93C76, M93C86, 1-Kbit, 2-Kbit, 4-Kbit, 8-Kbit, 16-Kbit MICROWIRE serial access EEPROM / Industrial grade Redesign and upgrade to the CMOSF8H process technology

What is the change?

The **M93C46, M93C56, M93C66, M93C76 & M93C86**, 1-Kbit, 2-Kbit, 4-Kbit, 8-Kbit and 16-Kbit MICROWIRE serial access EEPROM product families for industrial grade, currently produced using the CMOSF6SP 36% process technology at ST Ang Mo Kio (Singapore) 6" or at GLOBALFOUNDRIES (Singapore) 8" wafer diffusion plants, have been **redesigned** and will be **upgraded** to the **CMOSF8H** process technology at **ST Rousset** (France) 8" wafer diffusion plant.

This upgraded version in CMOSF8H allows offering:

- Write cycles up to 4 millions
- Data retention up to 200 years

The new M93C46, M93C56, M93C66, M93C76 and M93C86 in CMOSF8H version are functionally compatible with the current CMOSF6SP 36% version as per common datasheet rev. 13 – April 2013, attached.

These new M93C46, M93C56, M93C66, M93C76 and M93C86 are described in a common datasheet for M93**C**xx with following differences versus previous common datasheet:

- DC characteristic: I_{CC1} standby supply current:
  - Max 1 µA at V_{CC} = 1.8 V (was 2 µA for previous version)
  - Max 2 µA at V_{CC} = 2.5 V (was 5 µA for previous version)
- DC characteristic: f_C lock frequency:
  - Max 2 MHz for V_{CC} = 1.8 V (was 1 MHZ for previous version)

Concurrent to this change, the new M93C46, M93C56, M93C66, M93C76 and M93C86 in CMOSF8H will be assembled with 0.8 mil Copper wire when packaged in SO8N or in UFDFPN8 (MLP8).

Why?

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the M93C46, M93C56, M93C66, M93C76 and M93C86 in the new CMOSF8H process technology will increase the production capacity throughput and consequently improve the service to our customers.

When?

The production of the upgraded new M93C46, M93C56, M93C66, M93C76 and M93C86 in CMOSF8H with the new CMOSF8H will ramp up from November 2013 and shipments can start from end of January 2014 onward (or earlier upon customer approval).

How will the change be qualified?

The new version of the new M93C46, M93C56, M93C66, M93C76 and M93C86 in CMOSF8H has been qualified using the standard ST Microelectronics Corporate Procedures for Quality & Reliability.

Qualification Report QRMMY1317 rev. 2 is available and included inside this document.

What is the impact of the change?

- Form: Marking change (see **Device marking** paragraph)

- Fit: No change

- Function:

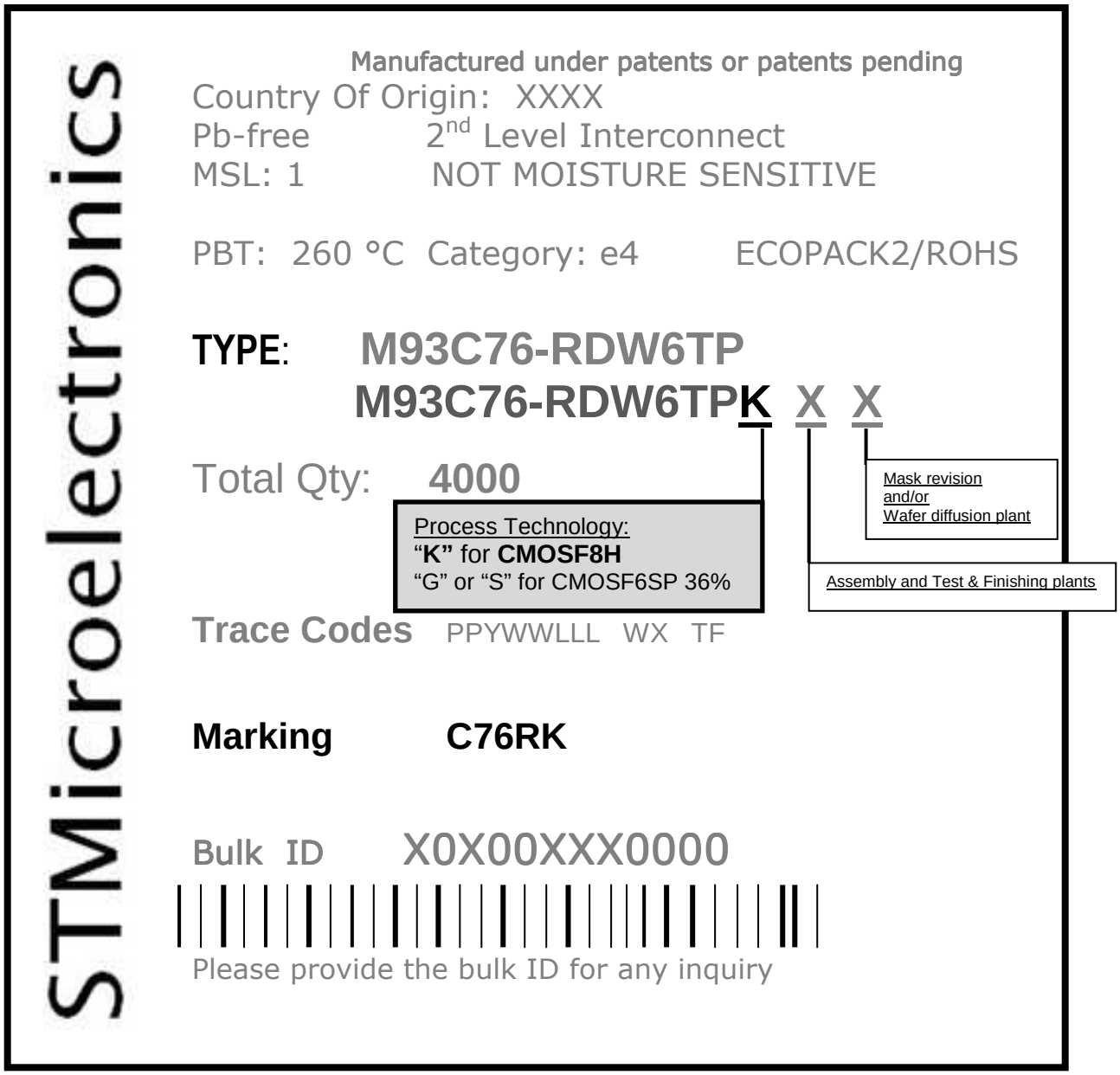
- Change on DC characteristic **I_{CC1} standby supply current**
- Change on AC characteristic **f_C Clock frequency for 1.8 V**

How can the change be seen?

- ***BOX LABEL MARKING***

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: the **process technology** identifier is "K" for the **upgraded version** in **CMOSF8H**, this identifier being "G" or "S" for the current version in CMOSF6SP 36%.

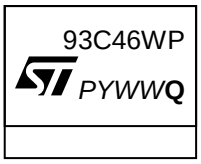
➔ *Example for M93C76-RDW6TP*



How can the change be seen?

- DEVICE MARKING

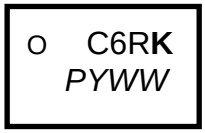
For the **SO8N** package, the difference is visible inside the trace code (*PYWWT*) where the last digit is "**K**" for the **upgraded version** in **CMOSF8H**, this digit being "G", "S" or "Q" for current versions.

	Upgraded CMOSF8H (ST Rousset)	Current CMOSF6SP 36% **(ST Ang Mo Kio or GLOBALFOUNDRIES)**
SO8N Example: M93C46-WMN6TP		

For the **TSSOP8** package, the difference is visible inside the product name where the last digit is "**K**" for the **upgraded version** in **CMOSF8H**, this digit being "P" for current version.

	Upgraded CMOSF8H (ST Rousset)	Current CMOSF6SP 36% **(ST Ang Mo Kio or GLOBALFOUNDRIES)**
TSSOP8 Example: M93C76-RDW6TP		

For the **UFDFPN8** package, the difference is visible inside the product name: **upgraded version** in **CMOSF8H** is **C6RK**, current version is C66R.

	Upgraded CMOSF8H (ST Rousset)	Current CMOSF6SP 36% **(ST Ang Mo Kio or GLOBALFOUNDRIES)**
UFDFPN8 M93C66-RMC6TG		

Appendix A- Product Change Information

Product family / Commercial products:	M93C46, M93C56, M93C66, M93C76, M93C86 products families / Industrial grade
Customer(s):	All
Type of change:	Wafer fab process technology change
Reason for the change:	Line up to state-of-the-art of process
Description of the change:	Redesign and upgrade to the new CMOSF8H Process technology.
Forecast date of the change: **(Notification to customer)**	Week 06 / 2014
Forecast date of **Qualification samples availability for customer(s):**	Week 12 / 2014 for **M93C76-RDW6TP**
Qualification Report availability:	**Qualification Report QRMMY1317** rev. 2 is available and included inside this document.
Marking to identify the changed product:	Process Technology identifier "K**"** for CMOSF8H for SO8N.
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	**M93C76-RDW6TP**
Manufacturing location:	Rousset 8 inch wafer fab
Estimated date of first shipment:	Week 19 / 2014

Appendix C: Qualification Report:

See following pages

QRMMY1317
Qualification report

New design / M93C76-R M93C76-W M93C76-A125 using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information		
Commercial product	M93C76-RDW6TP M93C76-WMN6TP	M93C76-RDW3TP/K M93C76-RMN3TP/K
Product description	8-Kbit (8-bit or 16-bit wide) MICROWIRE serial access EEPROM	
Product group	MMS	
Product division	MMY - Memory	
Silicon process technology	CMOSF8H	
Wafer fabrication location	RS8F - ST Rousset 8”, France	
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore Subcontractor Ardentec, Singapore	

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
	Subcontractor Amkor, Philippines	Subcontractor Amkor, Philippines
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
	Subcontractor Amkor, Philippines	Subcontractor Amkor, Philippines

Reliability / Qualification assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new design M93C76-R, M93C76-W and M93C76-A125 using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The CMOSF8H is a new advanced silicon process technology that is already qualified in the ST Rousset 8” fab, and in production for M24M02/M95M02, M24M01/M95M01, M24512/M95512, M24256/M95256, M24128/M95128, M24C64/M95640, M24C32/M95320 , M95160 and M93C86 EEPROM general purpose products.

The CMOSF8H technology is also qualified for automotive grade using M95640-A125 and M95640-A145 as driver products.

This document serves for the qualification of the named product using the named silicon process technology in the named diffusion fab.

The voltage and temperature ranges covered by this document are:

- 2.5 to 5.5 V at –40 to 85 °C for M93C76-W devices
- 1.8 to 5.5 V at –40 to 85 °C for M93C76-R devices
- 1.8 to 5.5 V at –40 to 125 °C for M93C76-A125 devices (automotive grade 1)

1.2 Conclusion

The new design M93C76-R, M93C76-W and M93C76-A125 using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab have passed all the reliability requirements and all products described in *Table 1* are qualified.

Refer to *Section 3: Reliability test results* for details.

2 Device characteristics

The M93C76 (8 Kbit) is an Electrically Erasable PROgrammable Memory (EEPROM) device accessed through the MICROWIRE bus protocol. The memory array can be configured either in bytes (x8b) or in words (x16b).

The M93C76-W devices operate within a voltage supply range from 2.5 V to 5.5 V and the M93C76-R devices operate within a voltage supply range from 1.8 V to 5.5 V. All these devices operate with a clock frequency of 2 MHz (or less), over an ambient temperature range of -40 °C / +85 °C.

The M93C76-A125 is a 8-Kbit serial EEPROM Automotive grade device operating up to 125 °C. The M93C76-A125 is compliant with the high level of reliability defined by the Automotive standard AEC-Q100 grade 1.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy. The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The CMOSF8H process technology and EEPROM new design core have been qualified for Automotive products on 3 lots using the driver product M95640 (refer to qualification report QREE0921).

The M93C76 is designed with the same technology and similar architecture as the driver product M95640. Qualification of M93C76 benefits of the family approach (1 lot).

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicles used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M93C76	CMOSF8H	ST Rousset 8”	CDIP8	Engineering assy (1)

1. CDIP8 is a engineering ceramic package used only for die-oriented reliability trials.

The product vehicles used for package qualification are presented in *Table 4*.

Table 4. Product vehicles used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M93C76	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen
			TSSOP8	ST Shenzhen
M95640 / M95160 / M24C64 (1)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen
			TSSOP8	ST Shenzhen

1. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of driver products M95640/M95160/M24C64 are applicable to M93C76.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1)

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M93C76		
						Lot 1	Lot 2	Lot 3
EDR	High temperature operating life after endurance							
	AEC-Q100-005	400K E/W cycles at 150 °C then: HTOL 150 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80
	Data retention after endurance							
	AEC-Q100-005	400K E/W cycles at 150 °C then: HTSL at 150 °C	80	3	1008 hrs	0/80	0/80	0/80
LTOL	Low temperature operating life							
	JESD22-A108	–40 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80
HTSL	High temperature storage life							
	AEC-Q100-005 JESD22-A103	Retention bake at 200 °C	80	3	1008 hrs	0/80	0/80	0/80
WEB	Program/erase endurance cycling + bake							
	Internal spec.	5 Million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	3	5 Million cycles / 48 hrs	0/80 (2)	0/80 (2)	0/80 (2)
ESD HBM	Electrostatic discharge (human body model)							
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ohms	27	3	N/A	Pass 4000 V	Pass 4000 V	Pass 4000 V
ESD MM	Electrostatic discharge (machine model)							
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ohms	12	3	N/A	Pass 400 V	Pass 400 V	Pass 400 V
LU	Latch-up (current injection and overvoltage stress)							
	AEC-Q100-004 JESD78B	At maximum operating temperature (150 °C)	6	3	N/A	Class II - Level A	Class II - Level A	Class II - Level A

1. See *Table 8: List of terms* for a definition of abbreviations.
2. First rejects after 10 million E/W cycles + bake.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen)(1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95640			M93C76 (2)(3)
						Lot1	Lot2	Lot3	Lot1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1280	1	N/A	0/1280	0/1280	0/1280	0/1280
THB (4)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	0/80
TC (4)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80	0/80	0/80	0/80
TMSK (4)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	1	200 shocks	0/80	0/80	0/80	0/80
AC (4)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	240 hrs	0/80	0/80	0/80	0/80
HTSL (4)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	0/80
HTOL (4)	High temperature operating life								
	AEC-Q100-JESD22-A108	HTOL 150 °C, 6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	0/80
ELFR (4)	Early life failure rate								
	AEC-Q100-008	HTOL 150 °C, 6 V	800	1	48 hrs	0/800	0/800	0/800	0/800
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 8: List of terms* for a definition of abbreviations.
2. Qualification on 3 lots using the driver product M95640 - Qualification of M93C76 benefits of the family approach (1 lot).
3. Data obtained on M95160 (larger memory array), except for ESD CDM.
4. THB-, TC-, TMSK-, AC-, HTSL-, HTOL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen)(1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95640			M93C76 (2)(3)
						Lot1	Lot2	Lot3	Lot1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1280	1	N/A	0/1280	0/1280	0/1280	0/1280
THB (4)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	0/80
TC (4)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80	0/80	0/80	0/80
TMSK (4)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	1	200 shocks	0/80	0/80	0/80	0/80
AC (4)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	240 hrs	0/80	0/80	0/80	0/80
HTSL (4)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	0/80
HTOL (4)	High temperature operating life								
	AEC-Q100-JESD22-A108	HTOL 150 °C, 6 V	80	1	1008 hrs	0/80	0/80	0/80	0/80
					2008 hrs	0/80	0/80	0/80	0/80
ELFR (4)	Early life failure rate								
	AEC-Q100-008	HTOL 150 °C, 6 V	800	1	48 hrs	0/800	0/800	0/800	0/800
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 8: List of terms* for a definition of abbreviations.
2. Qualification on 3 lots using the driver product M95640 - Qualification of M93C76 benefits of the family approach (1 lot).
3. Data obtained on M95160 (larger memory array), except for ESD CDM.
4. THB-, TC-, TMSK-, AC-, HTSL-, HTOL- and ELFR- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management for product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 8. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
12-Dec-2013	1	Initial release.
04-Feb-2014	2	List of qualified commercial product in *Table 1* updated

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Document Revision History

Date	Rev.	Description of the Revision
October 27, 2013	1.0	*First draft creation*
January 31, 2014	1.1	*Addendum (add M93C76-RDW6TP)*

Source Documents & Reference Documents

Source document Title	**Rev.:**	**Date:**

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