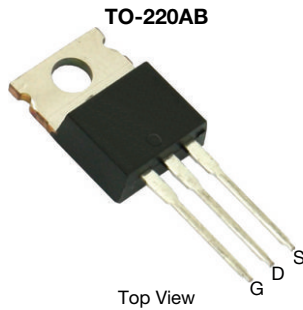


## P-Channel 100 V (D-S) 175 °C MOSFET



### FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- Maximum 175 °C junction temperature
- Low  $R_{DS(on)}$  minimizes power loss from conduction
- Compatible with logic-level gate driving
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

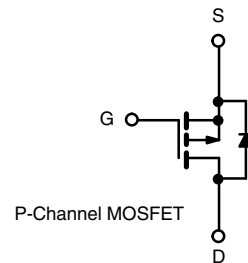


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

PRODUCT SUMMARY	
$V_{DS}$ (V)	-100
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = -10$ V	0.0101
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = -4.5$ V	0.0150
$Q_g$ typ. (nC)	125
$I_D$ (A)	-120
Configuration	Single

### APPLICATIONS

- Battery protection
- Motor drive control
- Load switch



ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free and halogen-free	SUP70101EL-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	-100	V
Gate-source voltage		$V_{GS}$	$\pm 20$	
Continuous drain current <sup>d</sup> ( $T_J = 175$ °C)	$T_C = 25$ °C	$I_D$	-120	A
	$T_C = 125$ °C		-78	
Pulsed drain current (100 $\mu$ s)		$I_{DM}$	-240	
Avalanche current	L = 0.1 mH	$I_{AS}$	-75	
Single pulse avalanche energy <sup>a</sup>		$E_{AS}$	281	mJ
Power dissipation	$T_C = 25$ °C <sup>c</sup>	$P_D$	375	W
	$T_C = 125$ °C <sup>b</sup>		125	
Operating junction and storage temperature range		$T_J, T_{stg}$	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	TYPICAL	UNIT
Junction-to-ambient	PCB mount <sup>b</sup>	$R_{thJA}$	40	°C/W
Junction-to-case		$R_{thJC}$	0.4	

#### Notes

- Duty cycle  $\leq 1$  %
- When mounted on 1" square PCB (FR4 material)
- See SOA curve for voltage derating
- Limited by package



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-100	-	-	V
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1.5	-	-2.5	
Gate-body leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = -100 V, V <sub>GS</sub> = 0 V	-	-	-1	μA
		V <sub>DS</sub> = -100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	-50	
		V <sub>DS</sub> = -100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C	-	-	-250	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -10 V	-120	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -30 A	-	0.0081	0.0101	Ω
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -20 A	-	0.0114	0.0150	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -25 A	-	60	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -50 V, f = 1 MHz	-	7000	-	pF
Output capacitance	C <sub>OSS</sub>		-	2180	-	
Reverse transfer capacitance	C <sub>rSS</sub>		-	170	-	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = -50 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -110 A	-	125	190	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>		-	29	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>		-	30	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	1.3	6.5	13	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -50 V, R <sub>L</sub> = 0.71 Ω I <sub>D</sub> ≅ -70 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω	-	20	30	ns
Rise time <sup>c</sup>	t <sub>r</sub>		-	40	60	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>		-	110	200	
Fall time <sup>c</sup>	t <sub>f</sub>		-	40	60	
<b>Drain-Source Body Diode Characteristics (T<sub>C</sub> = 25 °C <sup>b</sup>)</b>						
Continuous current	I <sub>S</sub>		-	-	-110	A
Pulsed current	I <sub>SM</sub>		-	-	-240	
Forward voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = -85 A, V <sub>GS</sub> = 0 V	-	-1	-1.5	V
Reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = -85 A, di/dt = 100 A/μs	-	110	170	ns
Peak reverse recovery charge	I <sub>RM(REC)</sub>		-	-7	-11	A
Reverse recovery charge	Q <sub>rr</sub>		-	0.38	0.57	μC

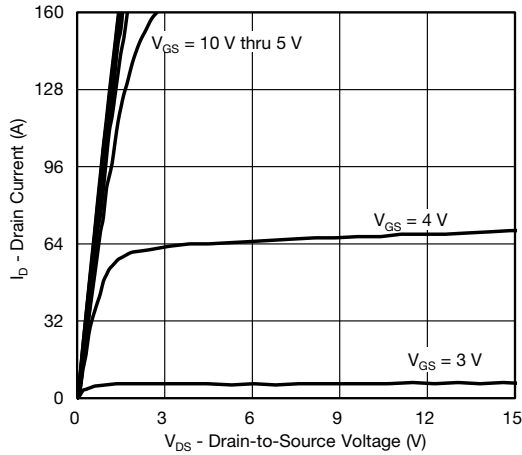
**Notes**

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- Guaranteed by design, not subject to production testing
- Independent of operating temperature

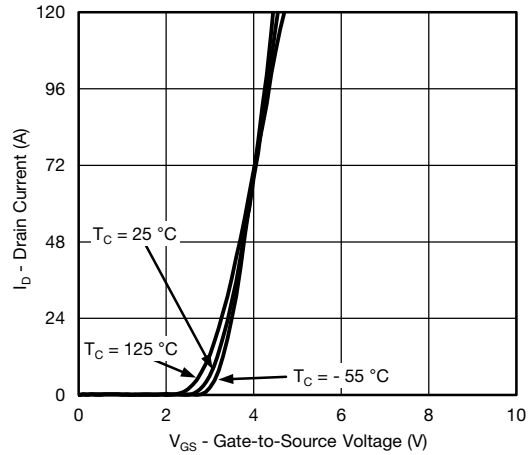
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



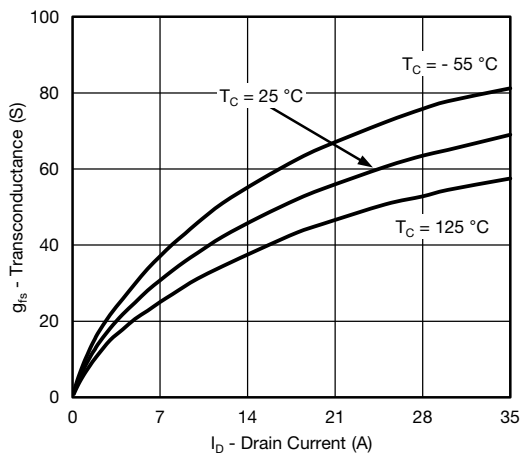
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



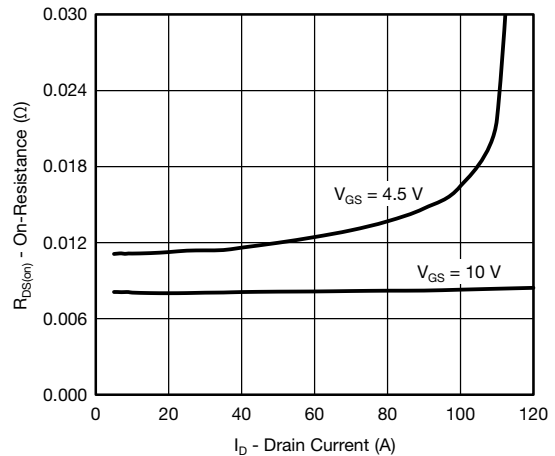
Output Characteristics



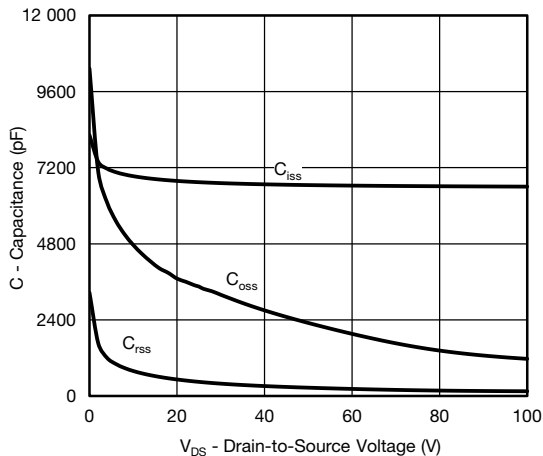
Transfer Characteristics



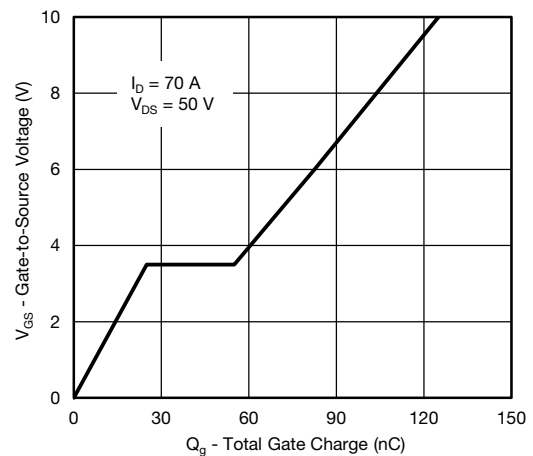
Transconductance



On-Resistance vs. Drain Current



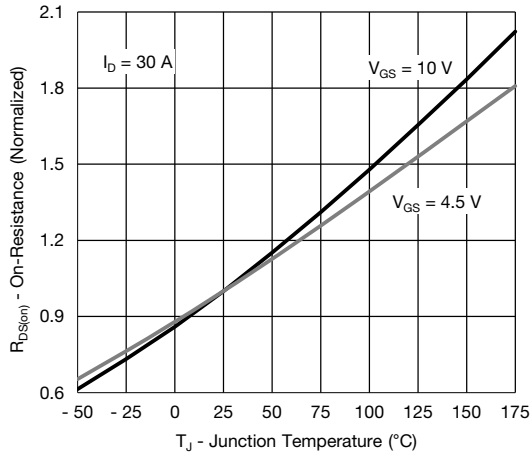
Capacitance



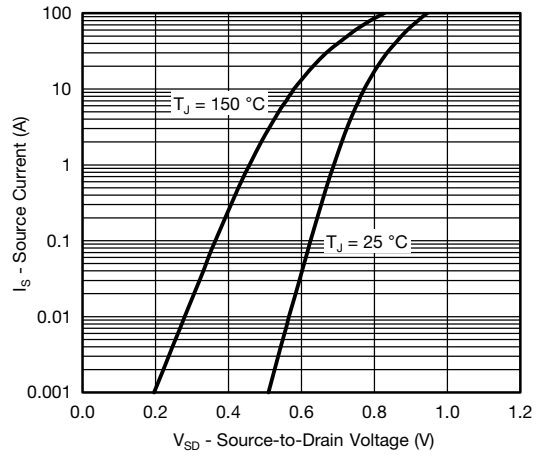
Gate Charge



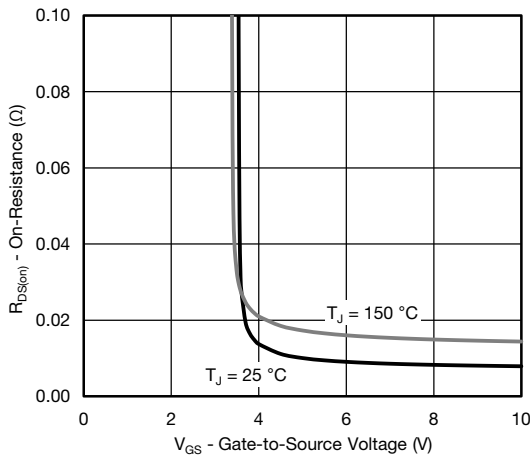
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



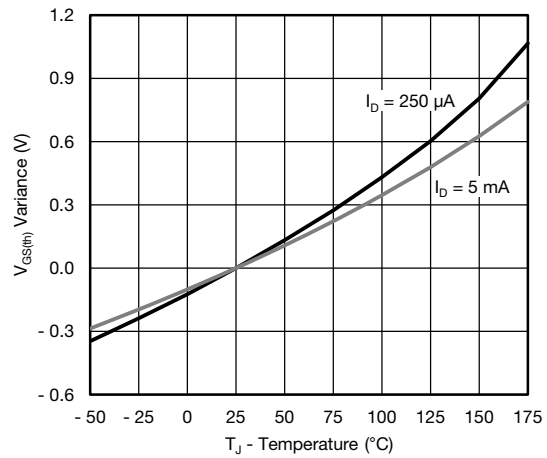
**On-Resistance vs. Junction Temperature**



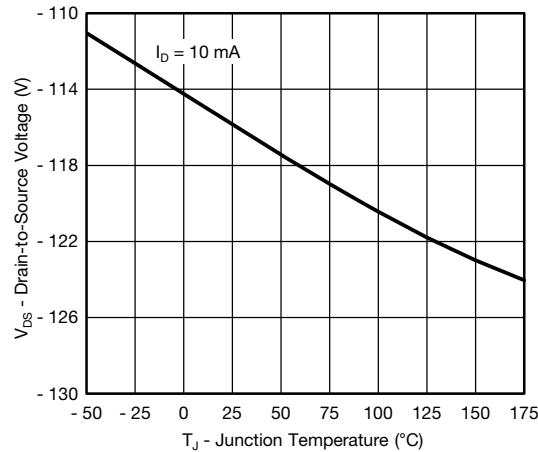
**Source Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



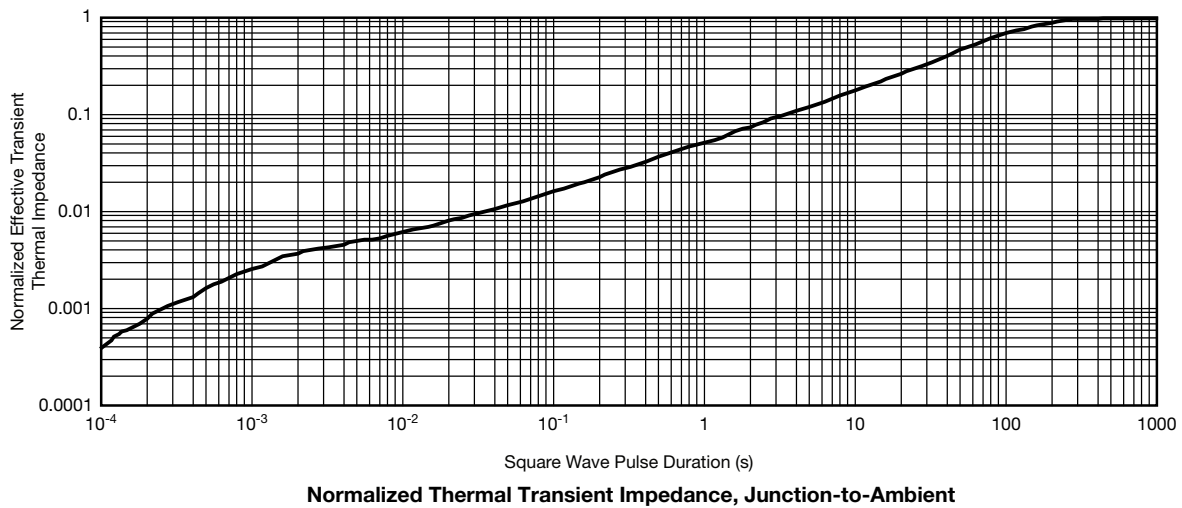
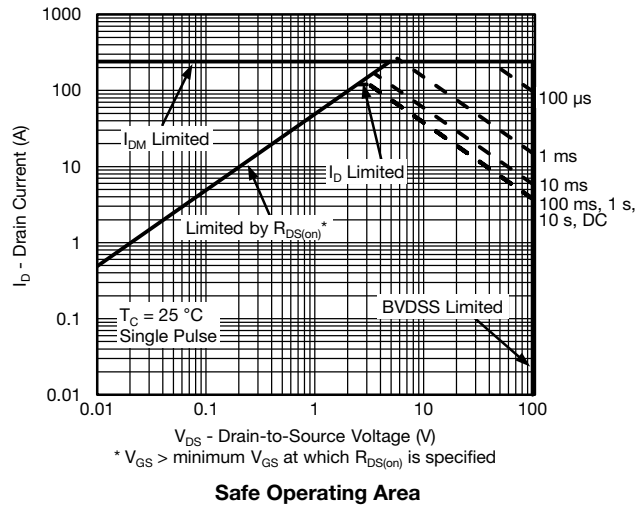
**Threshold Voltage**



**Drain Source Breakdown vs. Junction Temperature**

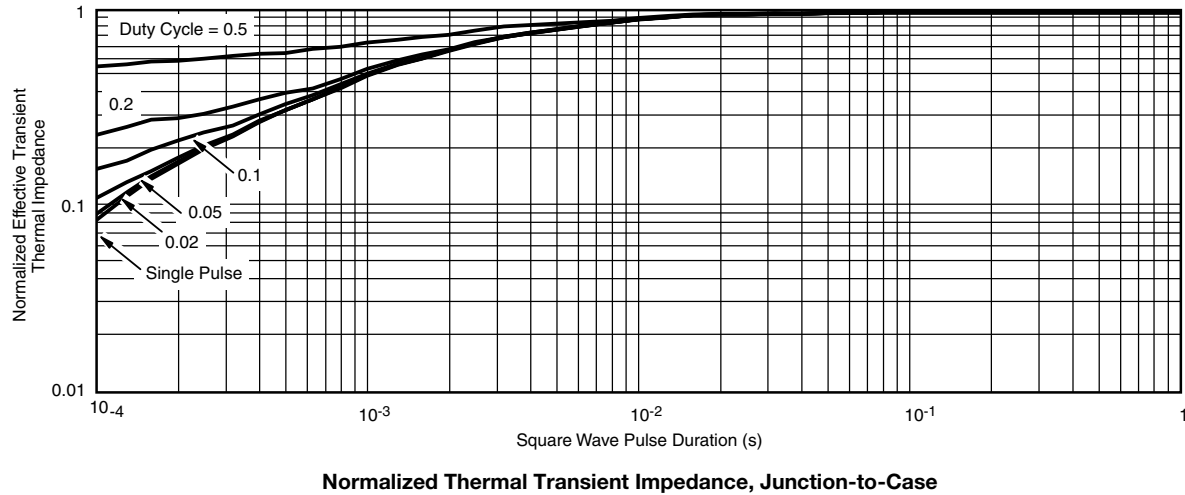


**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)





**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction to Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction to Case (25 °C)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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TO-220AB

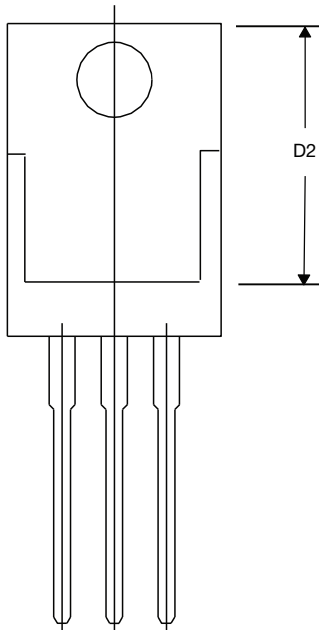


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
D2	12.19	12.70	0.480	0.500
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
$\varnothing P$	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: T14-0413-Rev. P, 16-Jun-14  
DWG: 5471

Note

\* M = 1.32 mm to 1.62 mm (dimension including protrusion)  
Heatsink hole for HVM





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