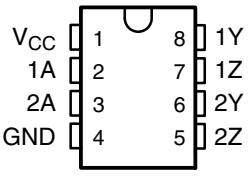
SLLS032B – DECEMBER 1987 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11**
- **Designed to Operate at 20 Mbaud or Higher**
- **TTL-and CMOS-Input Compatibility**
- **Single 5-V Supply Operation**
- **Output Short-Circuit Protection**
- **Improved Replacement for the μA9638**

D OR P PACKAGE
(TOP VIEW)



description

The SN75ALS191 is a dual, high-speed, differential line driver designed to meet ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11. The inputs are TTL- and CMOS-compatible and have input clamp diodes. Schottky-diode-clamped transistors minimize propagation delay time. This device operates from a single 5-V power supply and is supplied in eight-pin packages.

The SN75ALS191 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

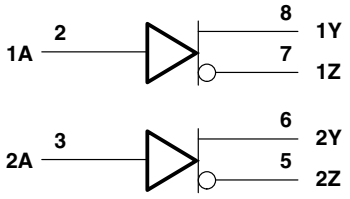
INPUTS A	OUTPUTS Y	OUTPUTS Z
H	H	L
L	L	H

H = high level, L = low level,
Z = high impedance

logic symbol†

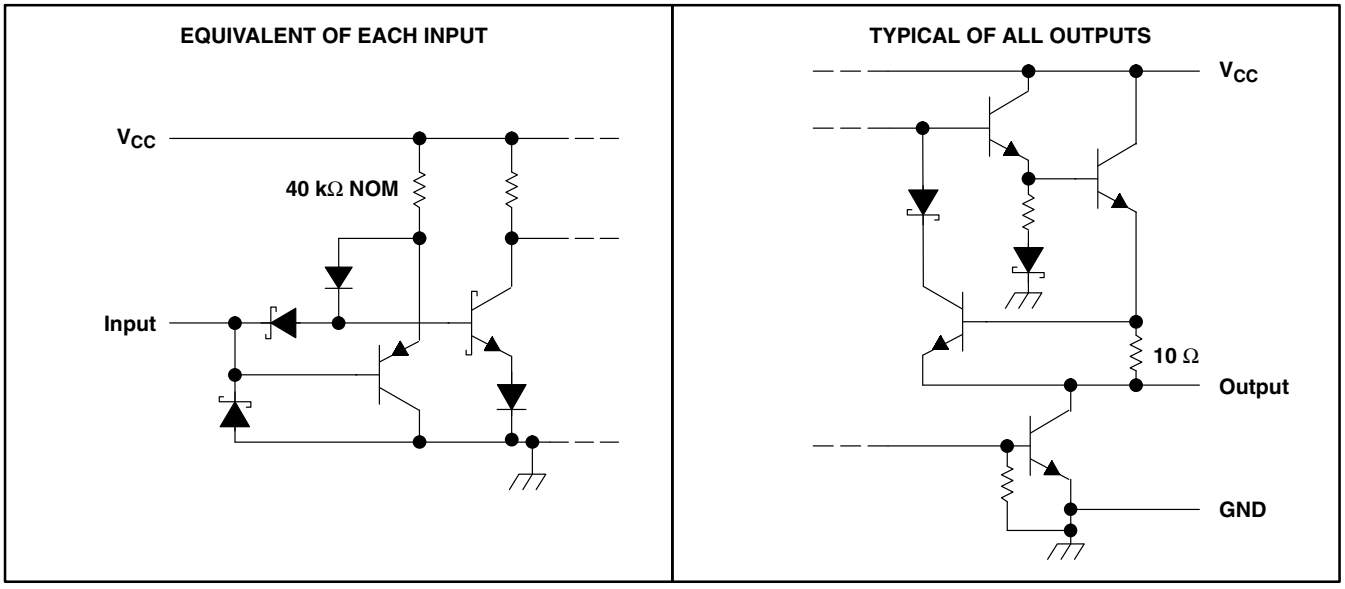
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential output voltage (V_{OD}) are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			– 50	mA
Low-level output current, I_{OL}			50	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = –18 mA			–1	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V	V_{IH} = 2 V,	I_{OH} = – 10 mA	2.5	3.3		V
				I_{OH} = – 40 mA	2			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 40 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,			0.5	V
$\|V_{OD1}\|$	Differential output voltage	V_{CC} = 5.25 V,	I_O = 0				2 V_{OD2}	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = 4.75 V to 5.25 V, See Figure 1		R_L = 100 Ω,	2			V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡						± 0.4	V
V_{OC}	Common-mode output voltage§						3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡						± 0.4	V
I_O	Output current with power off	V_{CC} = 0		V_O = 6 V		0.1	100	μA
				V_O = – 0.25 V		–0.1	–100	
				V_O = – 0.25 V to 6 V			±100	
I_I	Input current	V_{CC} = 5.25 V,	V_I = 5.5 V				50	μA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.5 V				200	μA
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V,	V_O = 0		–50		–150	mA
I_{CC}	Supply current (all drivers)	V_{CC} = 5.25 V,	No load,	All inputs at 0 V		32	40	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ | V_{OD} | and | V_{OC} | are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶ Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP#	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	C_L = 15 pF, R_L = 100 Ω, See Figure 2		3.5	7	ns
$t_{t(OD)}$	Differential-output transition time			3.5	7	ns
	Skew			1.5	4	ns

Typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

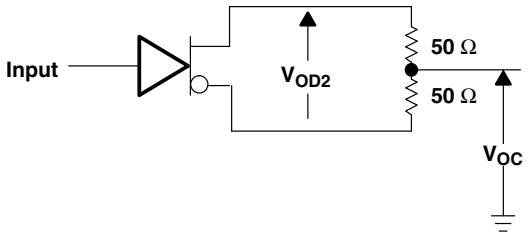
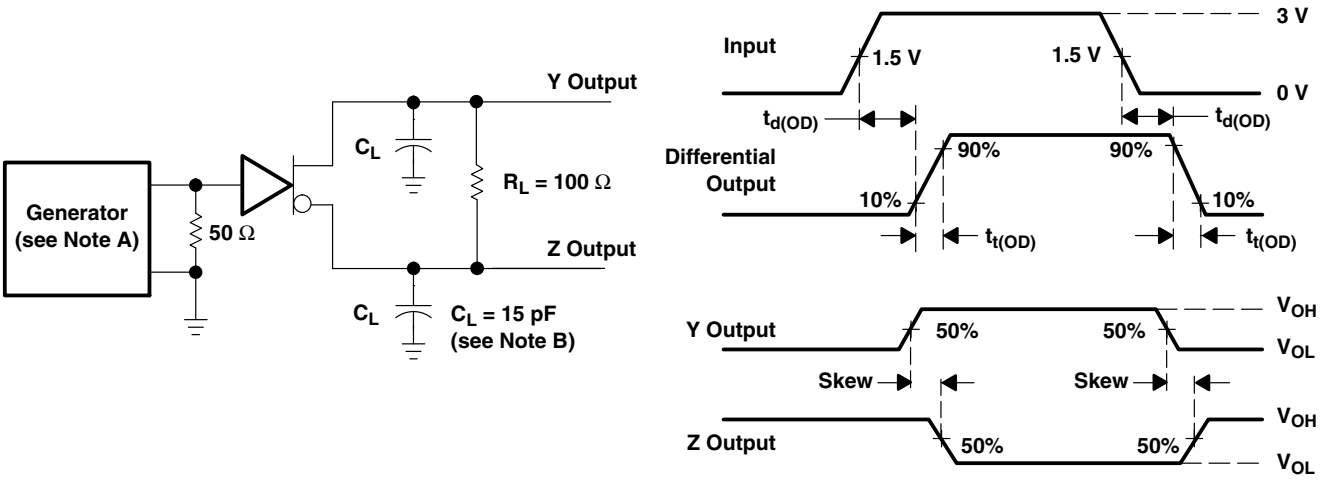


Figure 1. Differential and Common-Mode Output Voltages



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_w = 100 ns, t_r = ≤ 5 ns.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS191D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75A191	Samples
SN75ALS191DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75A191	Samples
SN75ALS191DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75A191	Samples
SN75ALS191P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75ALS191	Samples
SN75ALS191PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75ALS191	Samples
SN75ALS191PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	V191	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

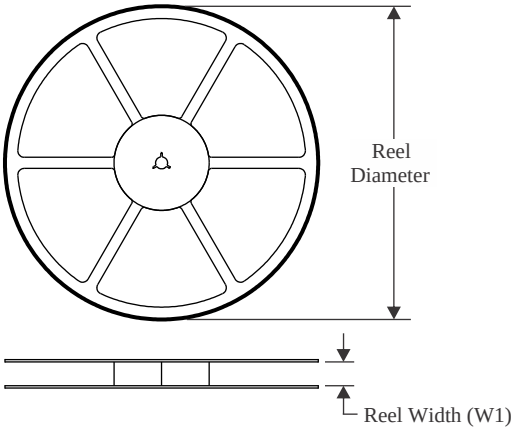
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

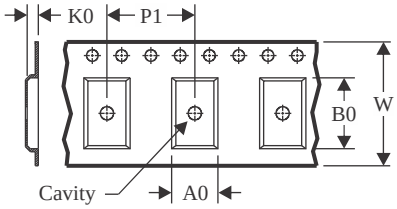
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

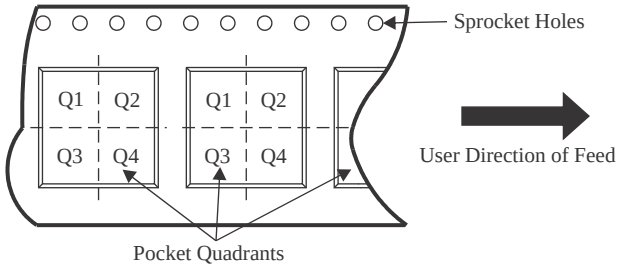


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

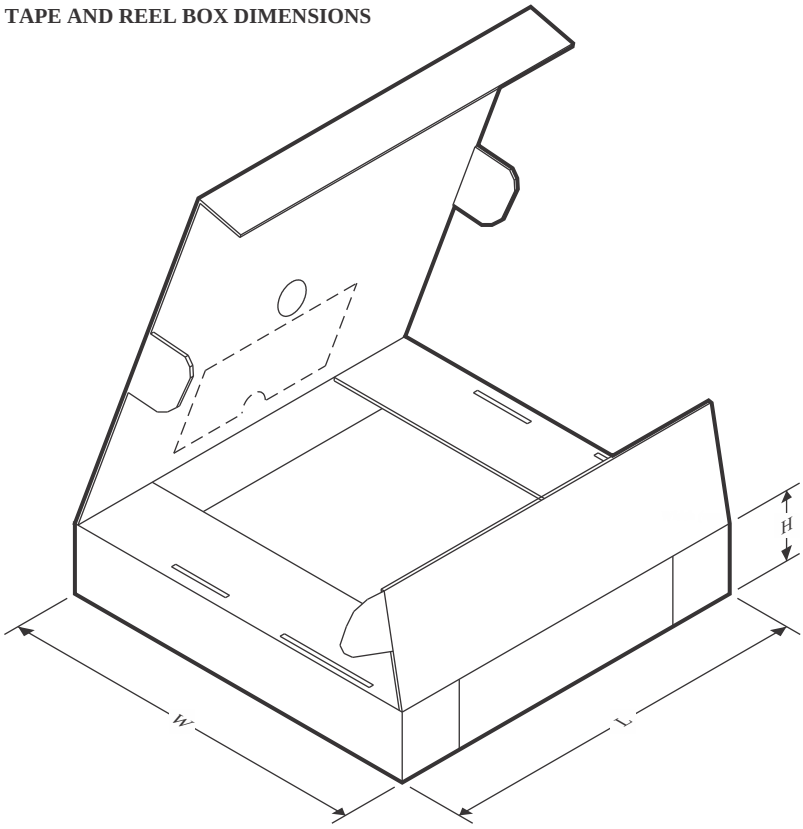
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS191DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75ALS191PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

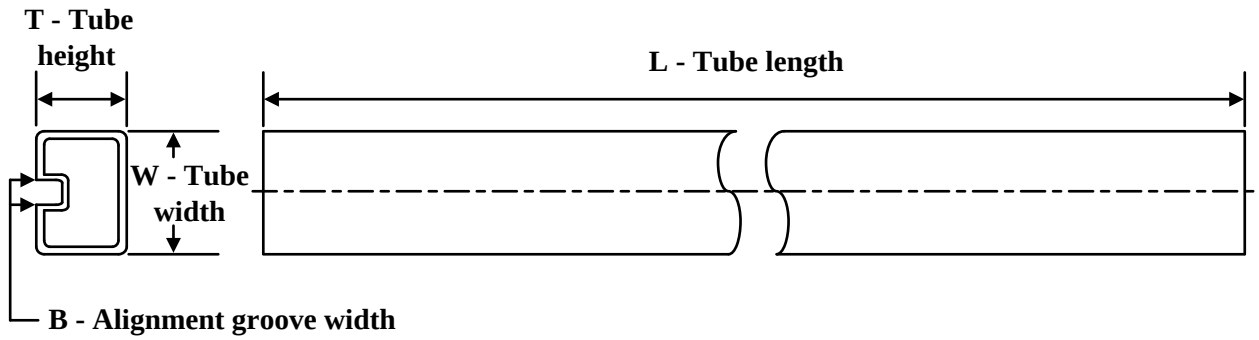
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

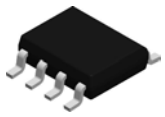
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS191DR	SOIC	D	8	2500	340.5	336.1	25.0
SN75ALS191PSR	SO	PS	8	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS191D	D	SOIC	8	75	507	8	3940	4.32
SN75ALS191DG4	D	SOIC	8	75	507	8	3940	4.32
SN75ALS191P	P	PDIP	8	50	506	13.97	11230	4.32
SN75ALS191PE4	P	PDIP	8	50	506	13.97	11230	4.32

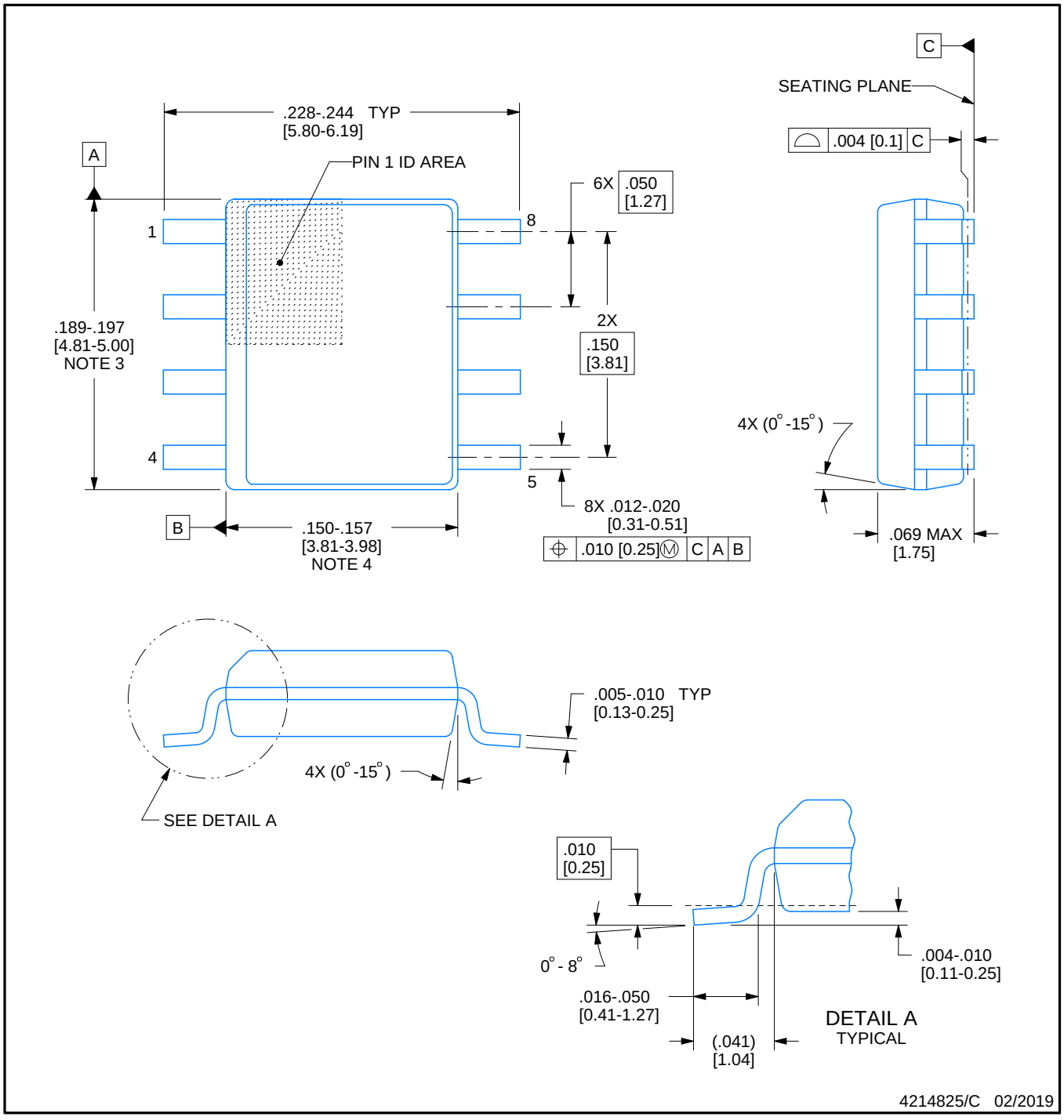


PACKAGE OUTLINE

D0008A

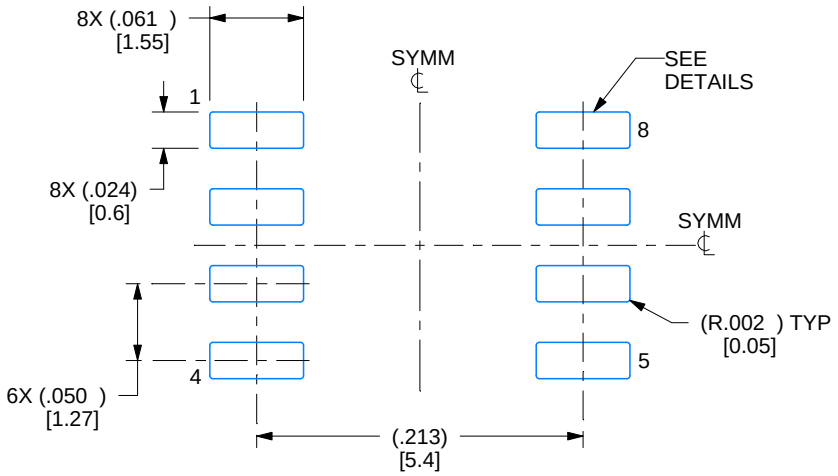
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

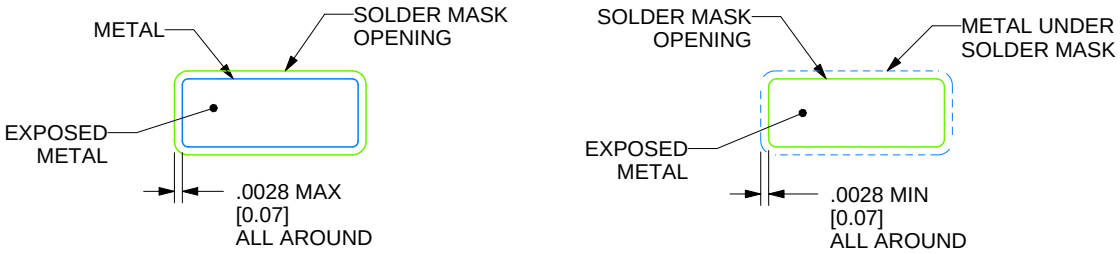


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

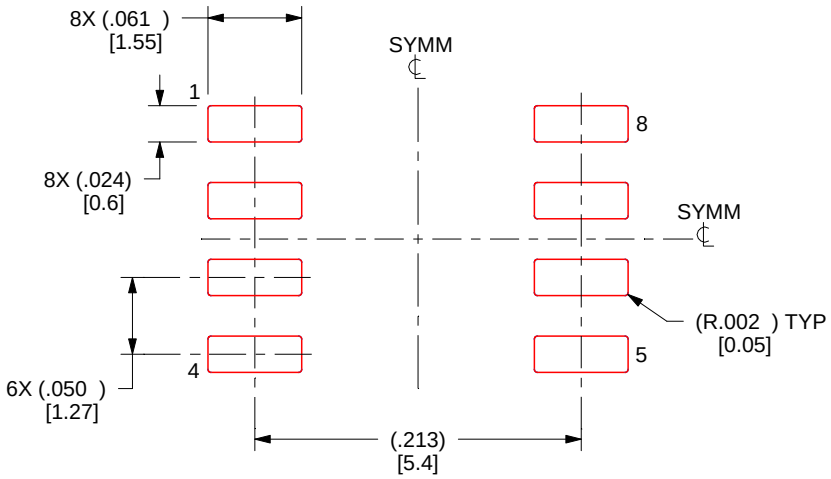
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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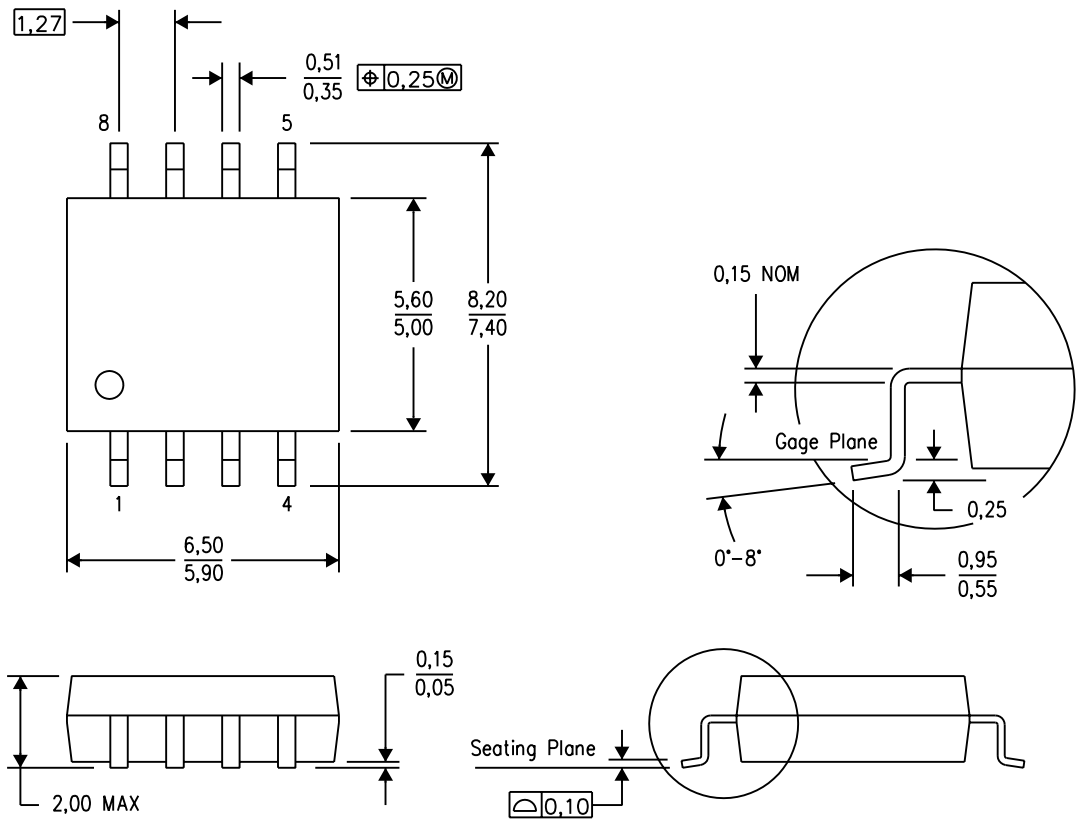
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

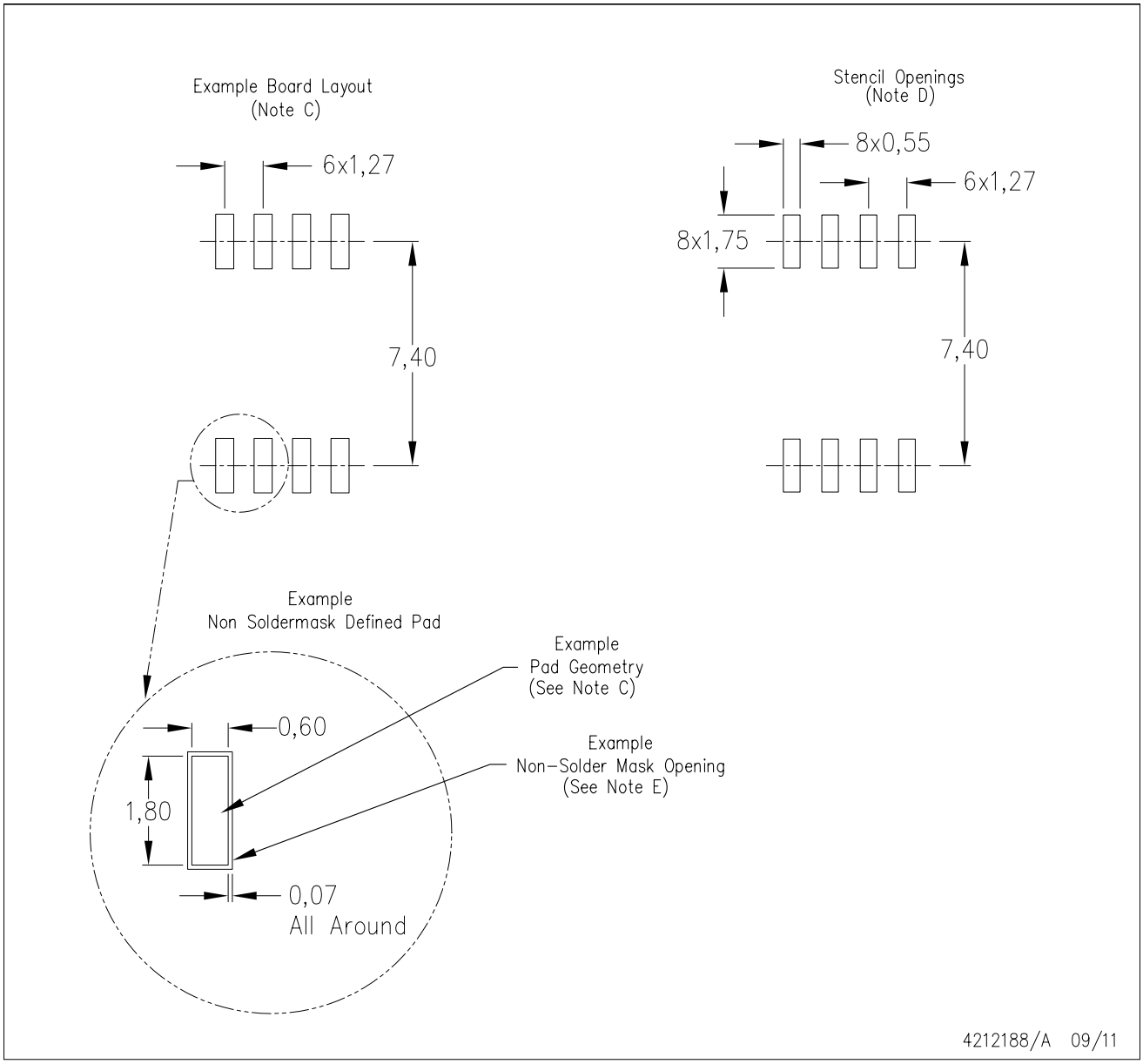
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

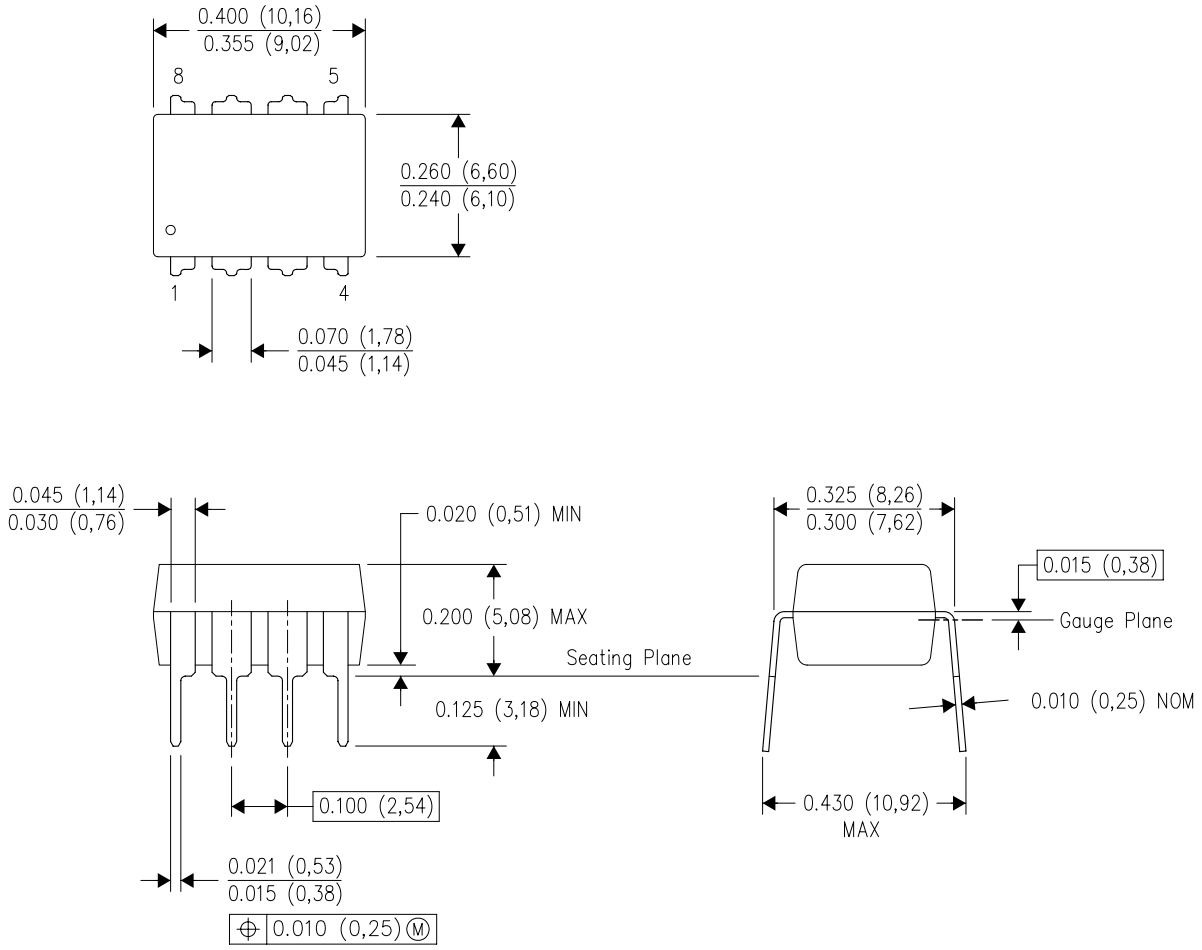
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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