User's Guide

The LP875761Q1EVM Evaluation Module

ABSTRACT

This user's guide describes the operation of the BMC043 evaluation module for the LP875761-Q1 multi-phase 4-core step-down converter from Texas Instruments (TI). The LP875761-Q1 is intended to be used in 4-phase output configuration (see Table 2-1). The user's guide also provides design information including the schematic and bill of materials (BOM).

	Warning	Warning Hot surface. Contact may cause burns. Do not touch!

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1 Trademarks

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2 Overview

The LP875761Q1EVM customer evaluation module demonstrates the integrated circuit LP875761-Q1 from TI. The LP875761-Q1 is a high-performance, multi-phase step-down converter designed to meet the power management requirements of the latest applications processors and platform needs in automotive infotainment and cluster applications and also in automotive camera power applications. The device contains four step-down converter cores, which are bundled together as one single 4-phase buck converter. This document covers user software provided with the EVM and design documentation that includes schematics and parts list.

Table 2-1. LP875761Q1 Configurations

PART NUMBER	OUTPUT CONFIGURATION	NUMBER OF OUTPUTS	EVM NUMBER
LP875761-Q1	4-phase	1	LP875761Q1EVM

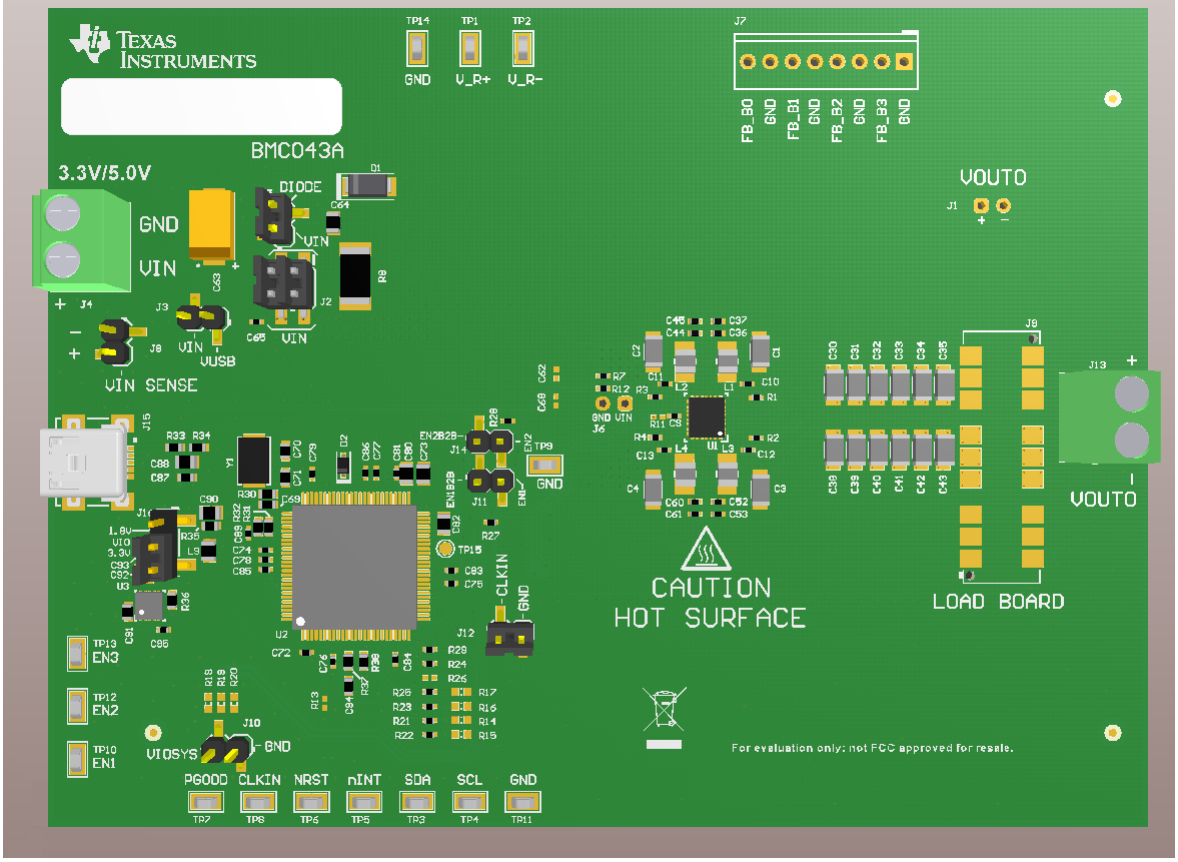


Figure 2-1. LP875761Q1EVM

3 Quick Setup Guide

Many of the components on the LP875761Q1EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

Upon opening the LP875761Q1EVM package, ensure that the following items are included:

- LP875761Q1EVM Evaluation Board
- USB Cable

If any of the items are missing, contact the closest Texas Instruments Product Information Center to inquire about a replacement.

3.1 Installing/Opening the Software

The EVM software is controlled through a graphical user interface (GUI). The software communicates with the EVM through an available USB port. The minimum hardware requirements for the EVM software are:

- IBM PC-compatible computer running a Microsoft Windows XP® or newer operating system
- Available USB port
- Mouse

Software installation

1. Open the LP8757_installer.exe.
2. Installer prompts to accept the license agreement (see Figure 3-1).
3. Installer prompts to choose which features of LP8757 Installer you want to install (see Figure 3-2).
4. Installer prompts to select Destination Folder (see Figure 3-3).
5. Press Install and the installation starts.
6. Installer prompts when installation is complete (see Figure 3-4).

Open the LP8757 GUI. Connect the EVM to the PC with the USB cable.

1. With the power supply disconnected from the unit under test (UUT), open LP8757.exe located in the directory selected during installation.
2. On the Evaluation SW window bottom right corner you should see text *Hardware connected*. Refer to Figure 3-5.

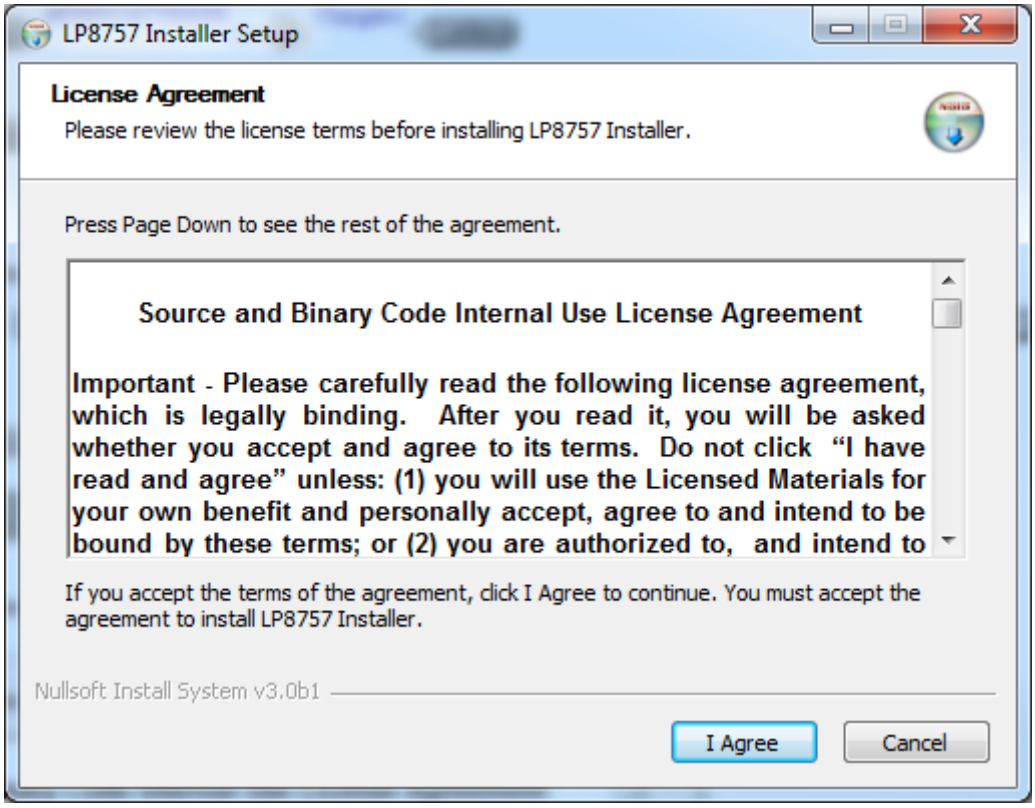


Figure 3-1. LP8757 Installer License Agreement

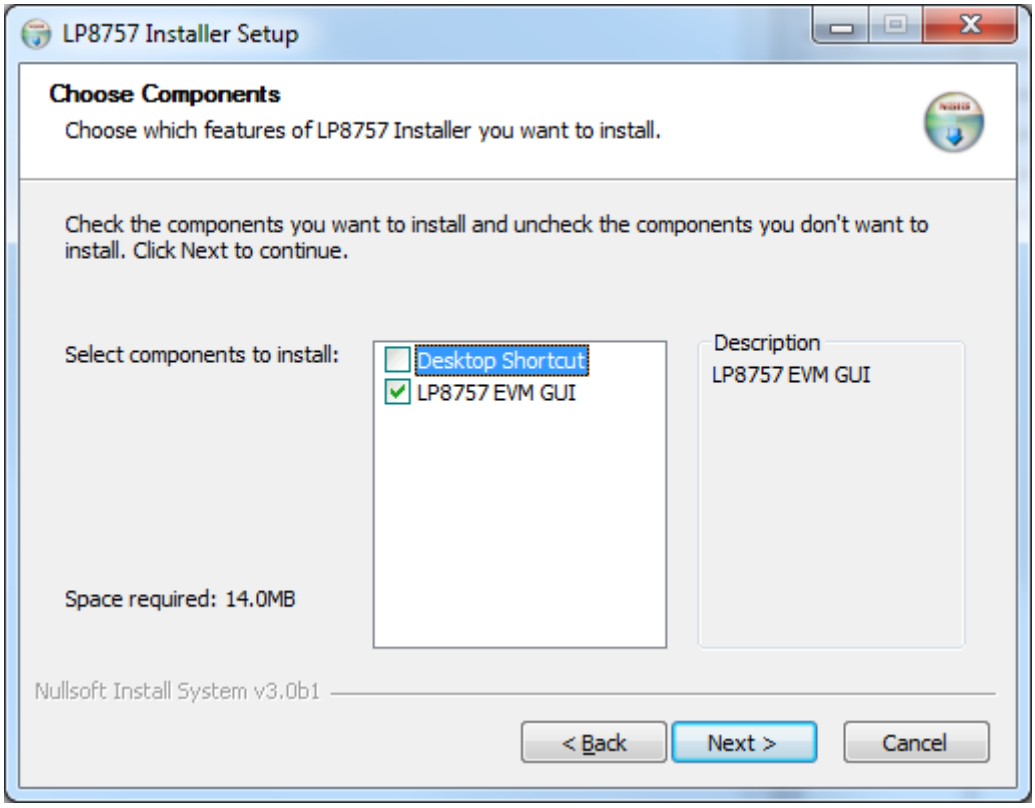


Figure 3-2. Features of LP8757 Installation

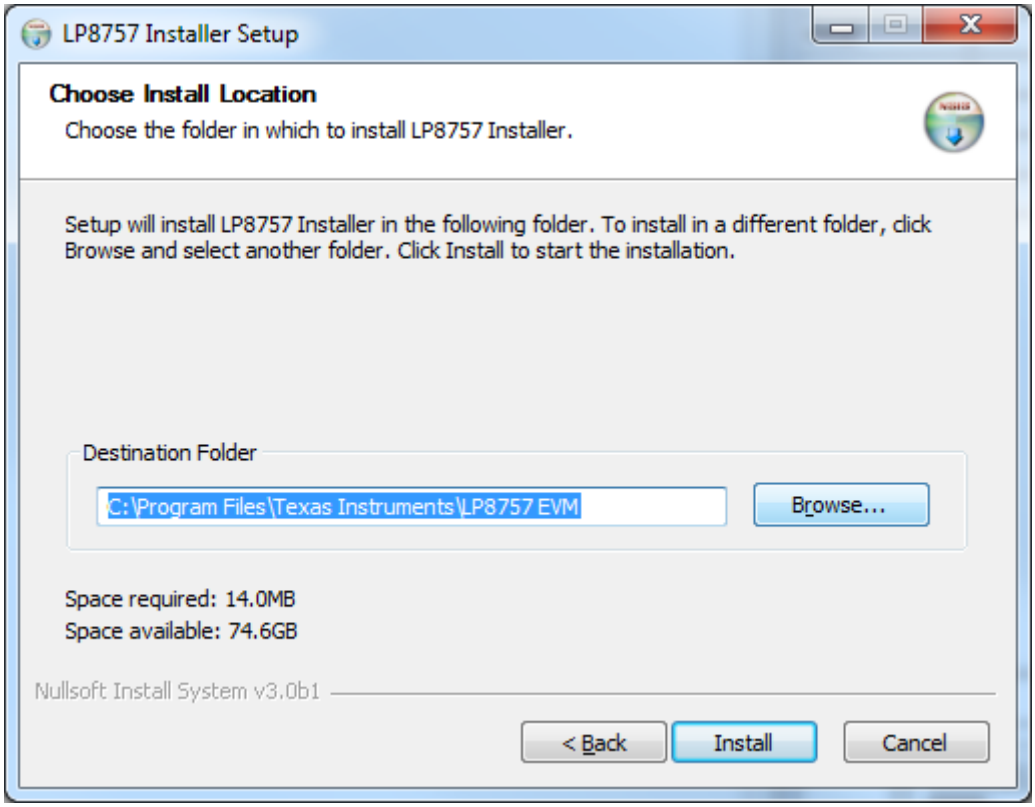


Figure 3-3. LP8757 Destination Folder

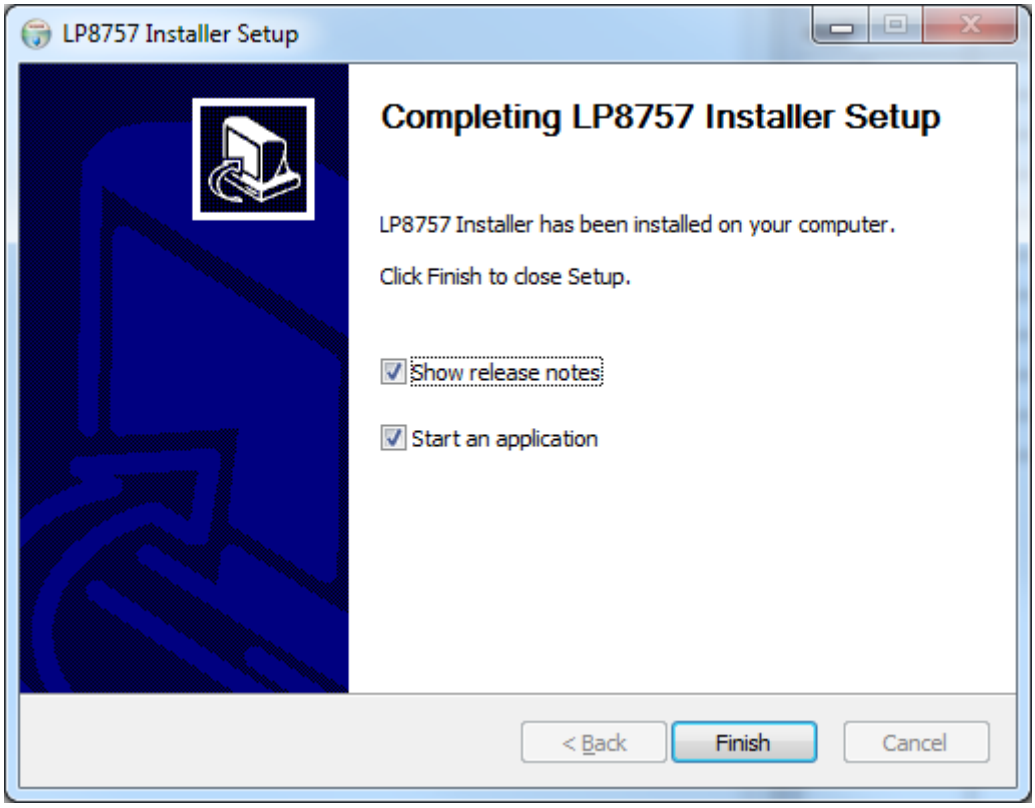


Figure 3-4. LP8757 Installation Complete

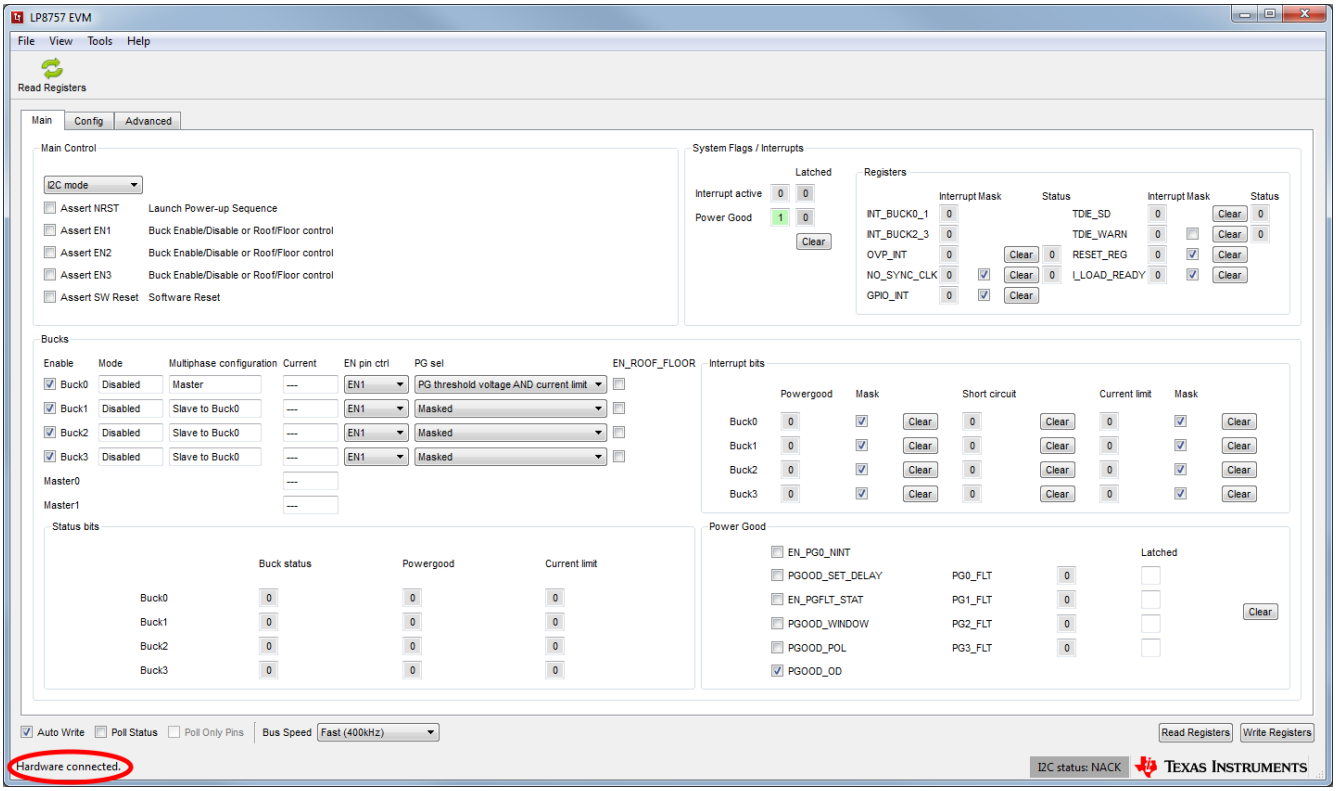


Figure 3-5. Evaluation Software Graphical User Interface (GUI) When Board Connected

3.2 Power Supply Setup

To power up the EVM, one power supply is needed. For full-load testing of the LP875761Q1EVM, a DC-power supply capable of at least 10 A and 5 V is required. 5 A is suggested as a practical minimum for partial load. The power supply is connected to the EVM using connector J4. The power supply and cabling must present low impedance to the UUT; the length of power supply cables must be minimized. Remote sense, using connector J8, can be used to compensate for voltage drop in the cabling.

With the power supply disconnected from the UUT, set the supply to 3.3 V or 5.0 V DC and the current limit to 5 A minimum. Set the power supply output OFF. Connect the power supply's positive terminal (+) to VIN and negative terminal (–) to GND on UUT (J4 power-in terminal block). Check that jumpers on the boards are set as shown in Figure 2-1 (factory default jumper configuration).

Set power supply output ON, and then continue with the following steps. Note that following steps are only an example. Register values, enable control, mode and multiphase status may differ depending on the LP875761Q1EVM configuration.

1. On Evaluation software GUI, click on Assert NRST (see Figure 3-6).
2. Click on either of the two Read Registers buttons. You should see ready message on green background next to the Read Registers button (see Figure 3-7).
3. Check that Buck0 is enabled, checkbox is ticked (see Figure 3-8).
4. Click on Assert EN1 (see Figure 3-9).
5. Click on either of the two Read Registers buttons.
6. In this example case the GUI indicates *Disabled* under *Mode* until EN1 is asserted. After EN1 is asserted *Mode* is changed to *Enabled*. In case BUCKx is enabled or disabled with bit instead of ENx pin, the *Mode* can be checked by reading registers. GUI indicates also *Master* under *Multiphase status* of Buck 0. Mode of other bucks are *Disabled* and Multiphase status is *Slave to Buck0*. The EVM is now ready for testing with default register settings loaded.

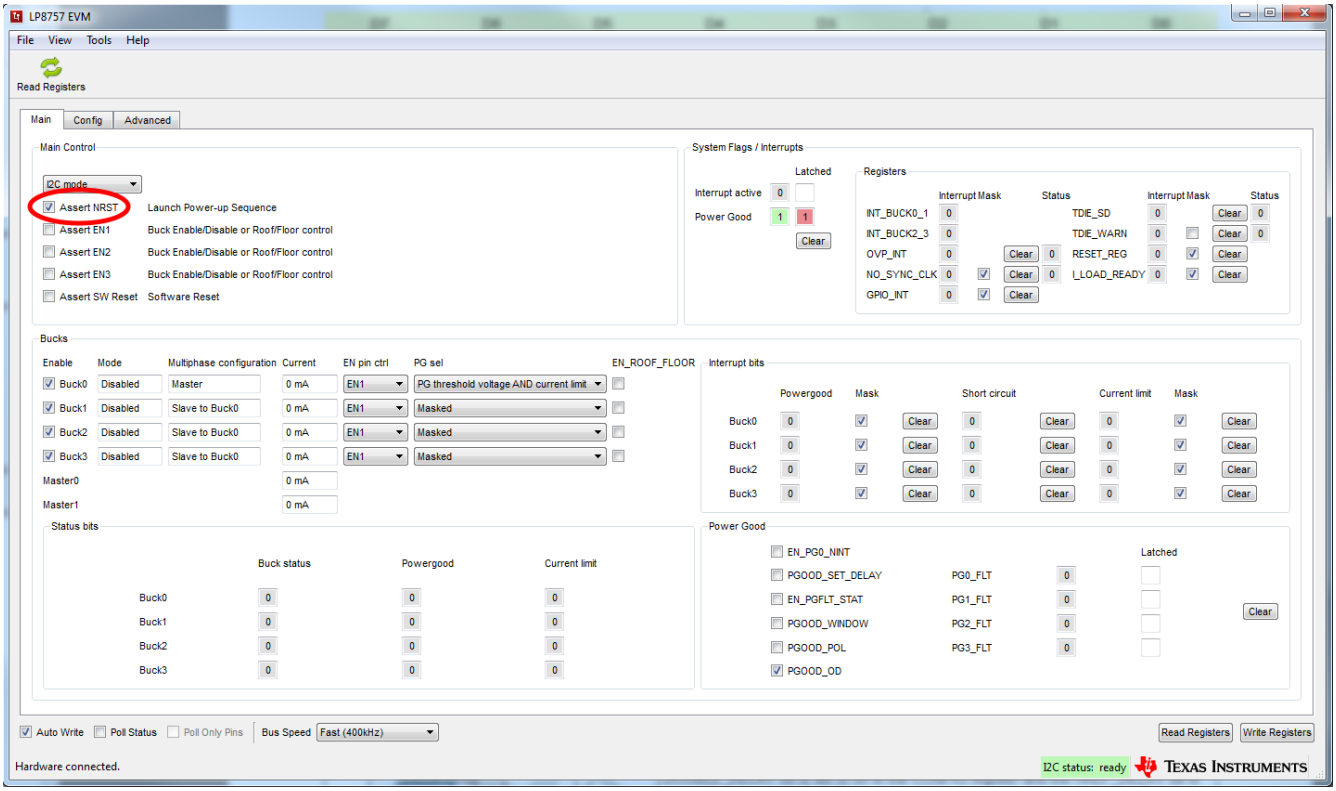


Figure 3-6. Assert nRST

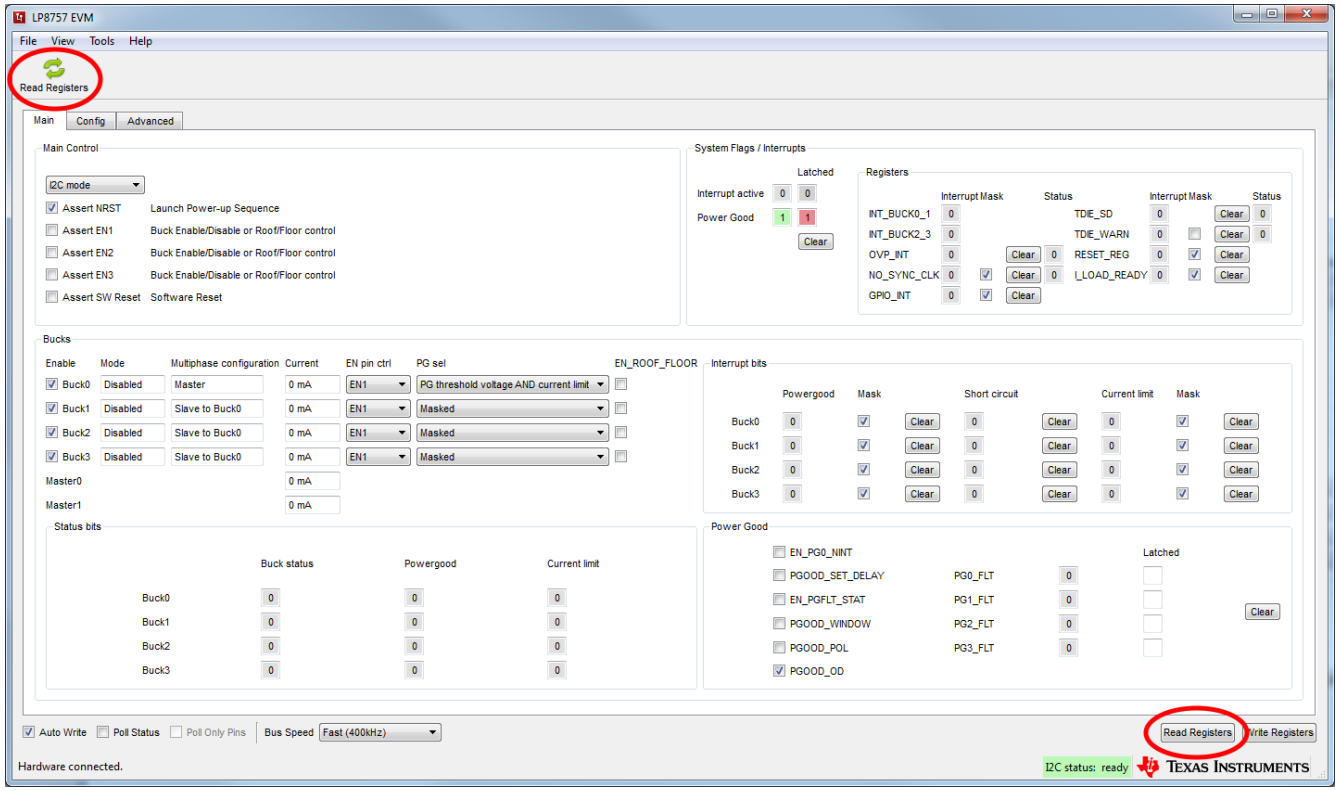


Figure 3-7. Read Registers Buttons

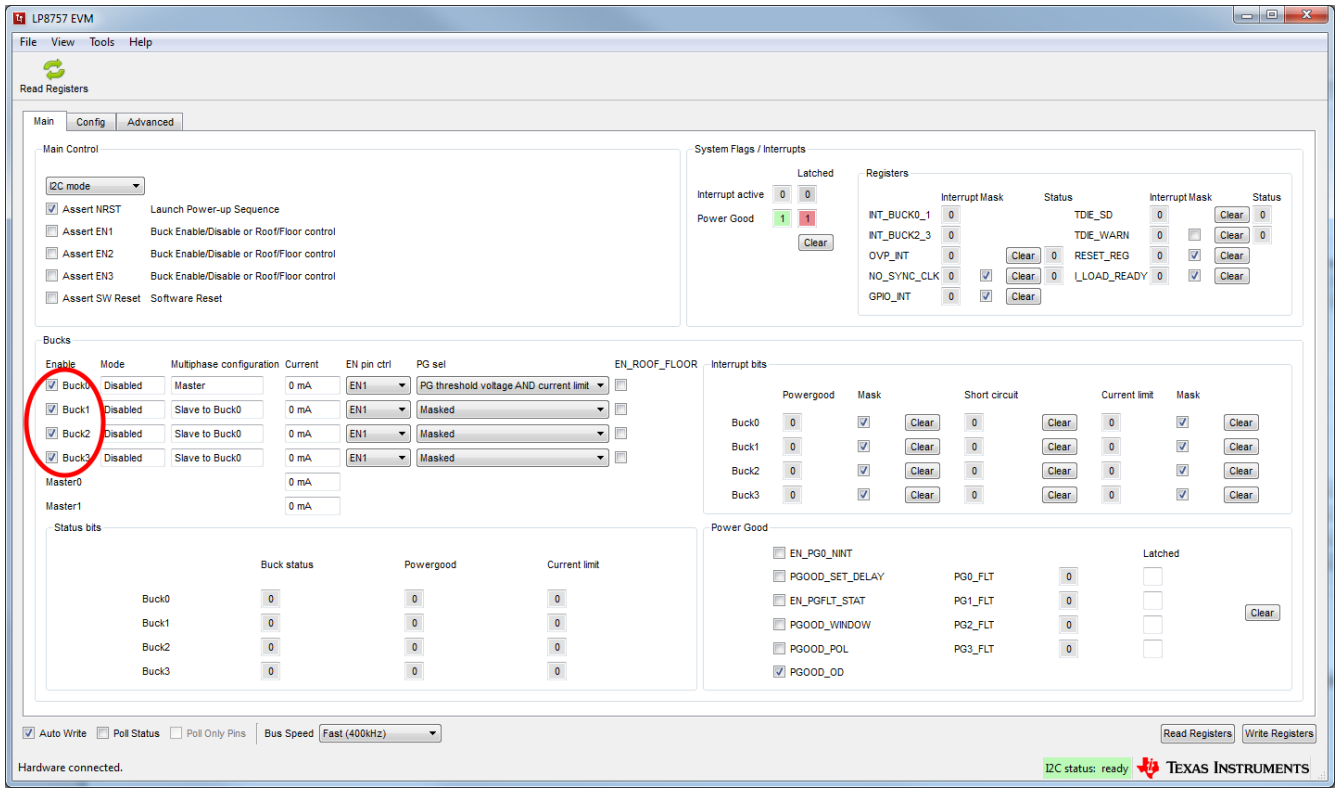


Figure 3-8. BUCK0 Enabled

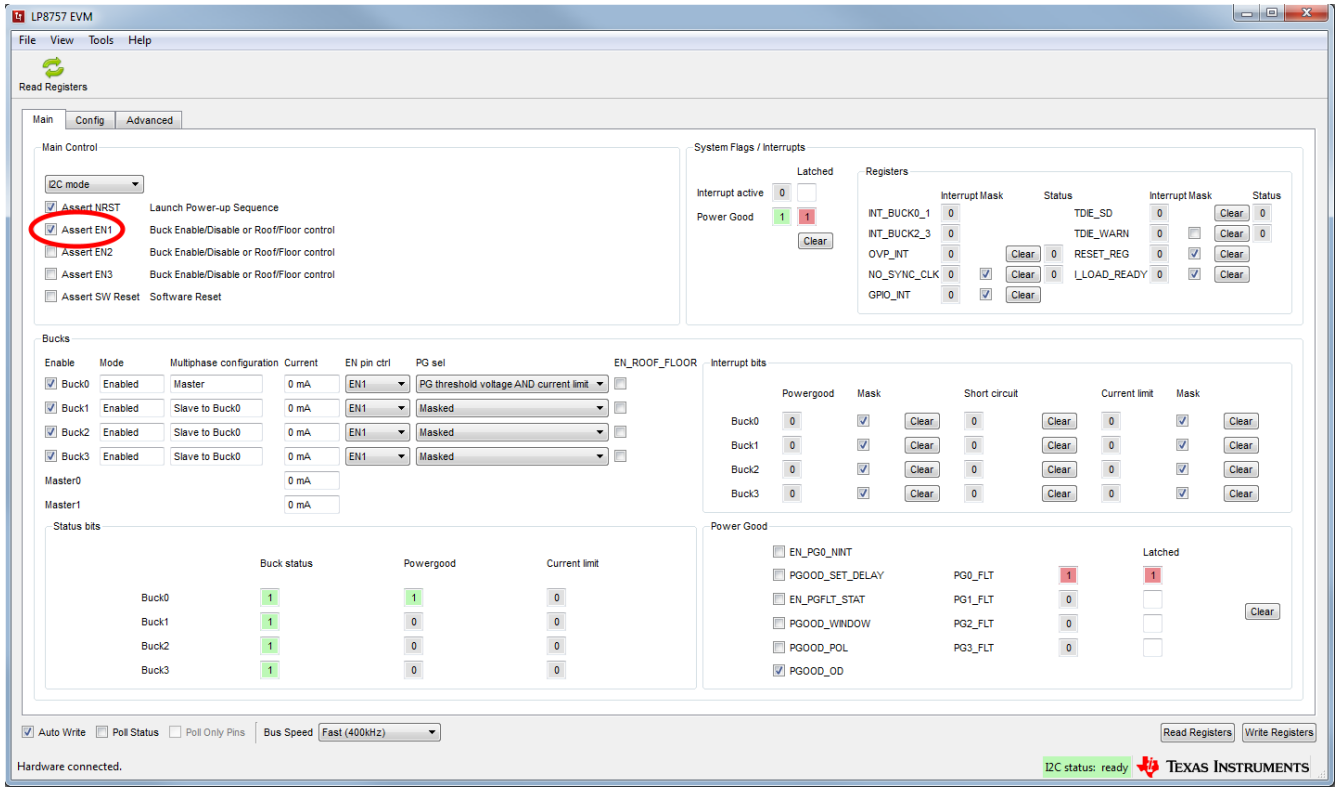


Figure 3-9. Assert EN1

3.3 Notes on Efficiency Measurement Procedure

Output Connections: An appropriate electronic load or high-power system source meter instrument, specified for operation down to 500 mV, is desirable for loading the UUT. The maximum load current is specified as 4 A per phase. Be sure to choose the correct wire size when attaching the electronic load. A wire resistance that is too high will cause a voltage drop in the power distribution path which becomes significant compared to the absolute value of the output voltage. Connect an electric load to J13. It is advised that, prior to connecting the load, it be set to sink 0 A to avoid power surges or possible shocks.

Voltage drop across the PCB traces will yield inaccurate efficiency measurements. For the most accurate voltage measurement at the EVM, use J6 (unpopulated through-hole) to measure the input voltage and J1 (unpopulated through-hole) to measure the output voltage.

To measure the current flowing to/from the UUT, use the current meter of the DC power supply/electric load as long as it is accurate. Some power source ammeters may show offset of several milliamps and thus will yield inaccurate efficiency measurements. In order to perform very accurate I_q measurements on the UUT, disconnect input protective Zener diode D1 by removing the shunt J5 from the board. When connected, this diode will cause some leakage, especially on high VIN voltages.

4 GUI Overview

The evaluation software has the following tabs: Main, Config, and Advanced. The three tabs together provide the user access to the whole register map of the LP875761-Q1. Additional register control can be obtained from Tools --> Direct Register Access.

4.1 Main Tab

The Main tab (see for example Figure 3-9) has the elemental controls for the EVM and provides a view to the chip status. Starting from top, the main controls are:

- I2C mode or 4 Enable mode. If this states I2C mode, device is controlled with I2C. When this states 4EN mode, bucks are controlled with ENx pins.
- Assert NRST: This checkbox will assert high level to LP875761-Q1 NRST pin. This pin enables the chip internal voltage reference and bias circuitry.
- Assert EN1: This checkbox will assert high level to LP875761-Q1 EN1 pin. Asserting EN1 may enable the buck regulator(s) or switch to different output voltage level, depending on the register settings.
- Assert EN2: This checkbox will assert high level to LP875761-Q1 EN2 pin. Asserting EN2 may enable the buck regulator(s) or switch to different output voltage level, depending on the register settings.
- Assert EN3: This checkbox will assert high level to LP875761-Q1 EN3 pin. Asserting EN3 may enable the buck regulator(s) or switch to different output voltage level, depending on the register settings.
- Assert EN4: In 4 Enable mode, this checkbox will assert high level to LP875761-Q1 SCL pin, (alternative function is EN4). Asserting EN4 may enable one or more of the buck regulators, depending on the register settings. This checkbox is visible only when device is configured to 4 Enable Signal Mode.
- Assert SW Reset: To perform a complete SW reset to the chip, assert this checkbox. See the LP875761-Q1 datasheet for explanation of LP875761-Q1 reset scenarios.

Note

The recommended start-up sequence for LP875761Q1 is to first assert NRST, then write all needed configuration bits by using the GUI, and then enable one or more of th buck regulators by ENx pin or EN_BUCKx bit.

The *Bucks* section provides status information and enable controls for all the 4 buck cores. On the left of the section are the check-boxes for the buck enable bits. The *Mode* field provides information on each of the buck core and can have any of the values given in Table 4-1:

Table 4-1. Mode Information

BUCK MODE	
Disabled	Buck state machine in 'disable'
Enabled	Buck state machine in 'enable'

The *Multiphase status* info field tells whether a buck core is configured as a master or a slave. The "Current" field gives the result of the buck converter load current measurement operation. Output currents of each buck core and total output current of one or more of the masters are shown on the fields.

The *System Flags / Interrupts* section as well as the *Interrupt bits* and the *Status bits* sections give data on system faults and warnings. If the interrupt is set for any reason the Interrupt active field shall show ‘1’ on red background. The flag causing the interrupt will also be set on the Main tab. Interrupts on LP875761-Q1 can only be cleared by writing '1’ to associated registers. Any individual flag can be cleared by clicking the *Clear* button next to each flag field. Some of the flags also have a mask bits. If *Mask* check-box of certain flag is checked, the interrupt is not generated. The *Status* bits will show the current status of the faults.

The *Power Good* section is for Power Good pin control and indication. It includes the latched values of buck Power Good Faults. These can be cleared with the Clear -button.

At the bottom of the GUI window is the *Auto Write* checkbox. If *Auto Write* is checked (default) any checking, un-checking or pulldown menu selections will immediately launch I^2C writes to the chip register(s). If not checked, the user can update the chip registers to correspond the configuration selected on the GUI by clicking *Write Registers*.

If *Poll Status* is selected the software sends a query to the LP875761-Q1 at a fixed interval in order to detect the status of the chip, including operation mode, multi-phase status, and output current. If also the *Poll Only Pins* is selected the software is monitoring only the state of Interrupt and Powergood pins. If *Poll Status* is not selected or if *Poll Only Pins* is selected, user can read the registers by applying *Read Registers*. *Bus Speed* pulldown menu selections are given in Table 4-2 below and is instantly applied for System I^2C.

Table 4-2. I^2C-Compatible Bus Support

BUS SPEED SELECTION	EXPLANATION
Fast (400 kHz)	Fast I^2C-compliant operation at 400 kHz
High-Speed (3.4 MHz)	HS I^2C-compliant data transfer with master codes.

4.2 Other Tabs and Menus

The *Tools* pulldown menu hosts another way of accessing the LP875761-Q1 registers (see Figure 4-1). The *Direct Register Access* tool can be used to read or write any register (see Figure 4-2). Selecting a register, the bits appear on the right side Field View (see Figure 4-3). When moving mouse over bits in Field View, bits are highlighted in the register view. Bits can be controlled either from register view or field view. Register settings can also be saved to a file or pre-made register file can be loaded in the Direct Register Access tool. Registers can be updated immediately or manually (see Figure 4-4).

When using direct register access, TI recommends un-checking the poll status check-box. This way the GUI will only do the reads and writes commanded from the direct access dialog.

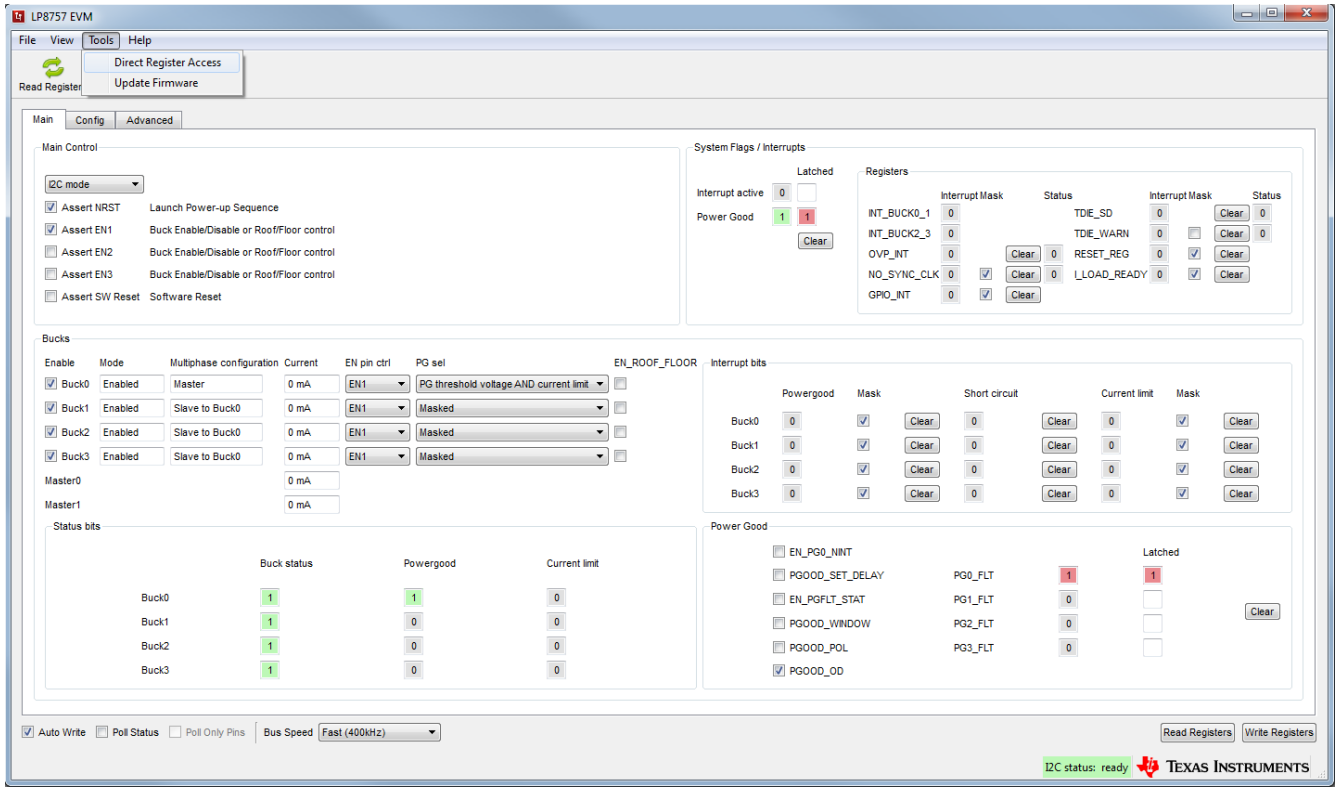
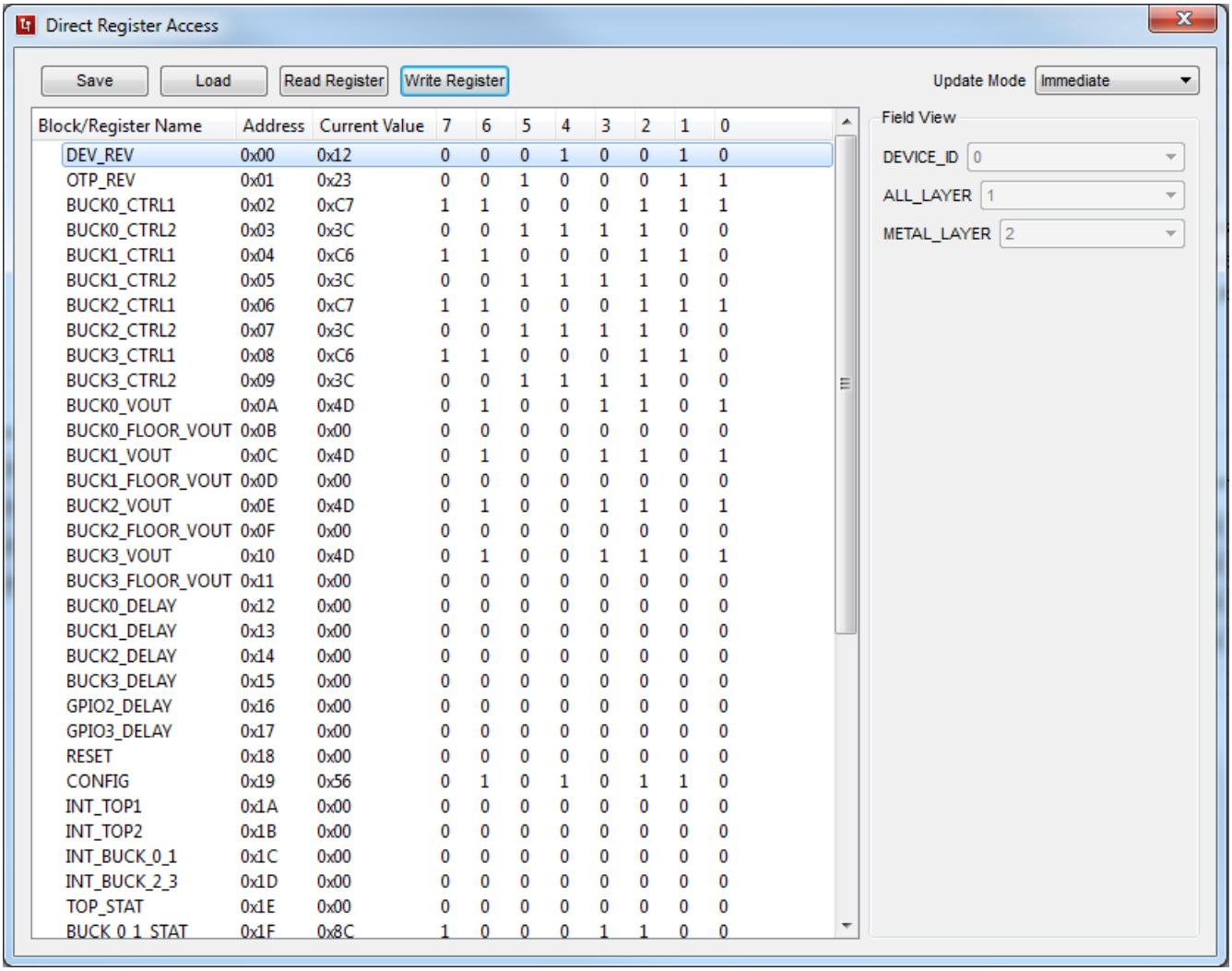


Figure 4-1. Accessing Direct Register Write



Block/Register Name	Address	Current Value	7	6	5	4	3	2	1	0
DEV_REV	0x00	0x12	0	0	0	1	0	0	1	0
OTP_REV	0x01	0x23	0	0	1	0	0	0	1	1
BUCK0_CTRL1	0x02	0xC7	1	1	0	0	0	1	1	1
BUCK0_CTRL2	0x03	0x3C	0	0	1	1	1	1	0	0
BUCK1_CTRL1	0x04	0xC6	1	1	0	0	0	1	1	0
BUCK1_CTRL2	0x05	0x3C	0	0	1	1	1	1	0	0
BUCK2_CTRL1	0x06	0xC7	1	1	0	0	0	1	1	1
BUCK2_CTRL2	0x07	0x3C	0	0	1	1	1	1	0	0
BUCK3_CTRL1	0x08	0xC6	1	1	0	0	0	1	1	0
BUCK3_CTRL2	0x09	0x3C	0	0	1	1	1	1	0	0
BUCK0_VOUT	0x0A	0x4D	0	1	0	0	1	1	0	1
BUCK0_FLOOR_VOUT	0x0B	0x00	0	0	0	0	0	0	0	0
BUCK1_VOUT	0x0C	0x4D	0	1	0	0	1	1	0	1
BUCK1_FLOOR_VOUT	0x0D	0x00	0	0	0	0	0	0	0	0
BUCK2_VOUT	0x0E	0x4D	0	1	0	0	1	1	0	1
BUCK2_FLOOR_VOUT	0x0F	0x00	0	0	0	0	0	0	0	0
BUCK3_VOUT	0x10	0x4D	0	1	0	0	1	1	0	1
BUCK3_FLOOR_VOUT	0x11	0x00	0	0	0	0	0	0	0	0
BUCK0_DELAY	0x12	0x00	0	0	0	0	0	0	0	0
BUCK1_DELAY	0x13	0x00	0	0	0	0	0	0	0	0
BUCK2_DELAY	0x14	0x00	0	0	0	0	0	0	0	0
BUCK3_DELAY	0x15	0x00	0	0	0	0	0	0	0	0
GPIO2_DELAY	0x16	0x00	0	0	0	0	0	0	0	0
GPIO3_DELAY	0x17	0x00	0	0	0	0	0	0	0	0
RESET	0x18	0x00	0	0	0	0	0	0	0	0
CONFIG	0x19	0x56	0	1	0	1	0	1	1	0
INT_TOP1	0x1A	0x00	0	0	0	0	0	0	0	0
INT_TOP2	0x1B	0x00	0	0	0	0	0	0	0	0
INT_BUCK_0_1	0x1C	0x00	0	0	0	0	0	0	0	0
INT_BUCK_2_3	0x1D	0x00	0	0	0	0	0	0	0	0
TOP_STAT	0x1E	0x00	0	0	0	0	0	0	0	0
BUCK_0_1_STAT	0x1F	0x8C	1	0	0	0	1	1	0	0

Figure 4-2. Direct Register Access View

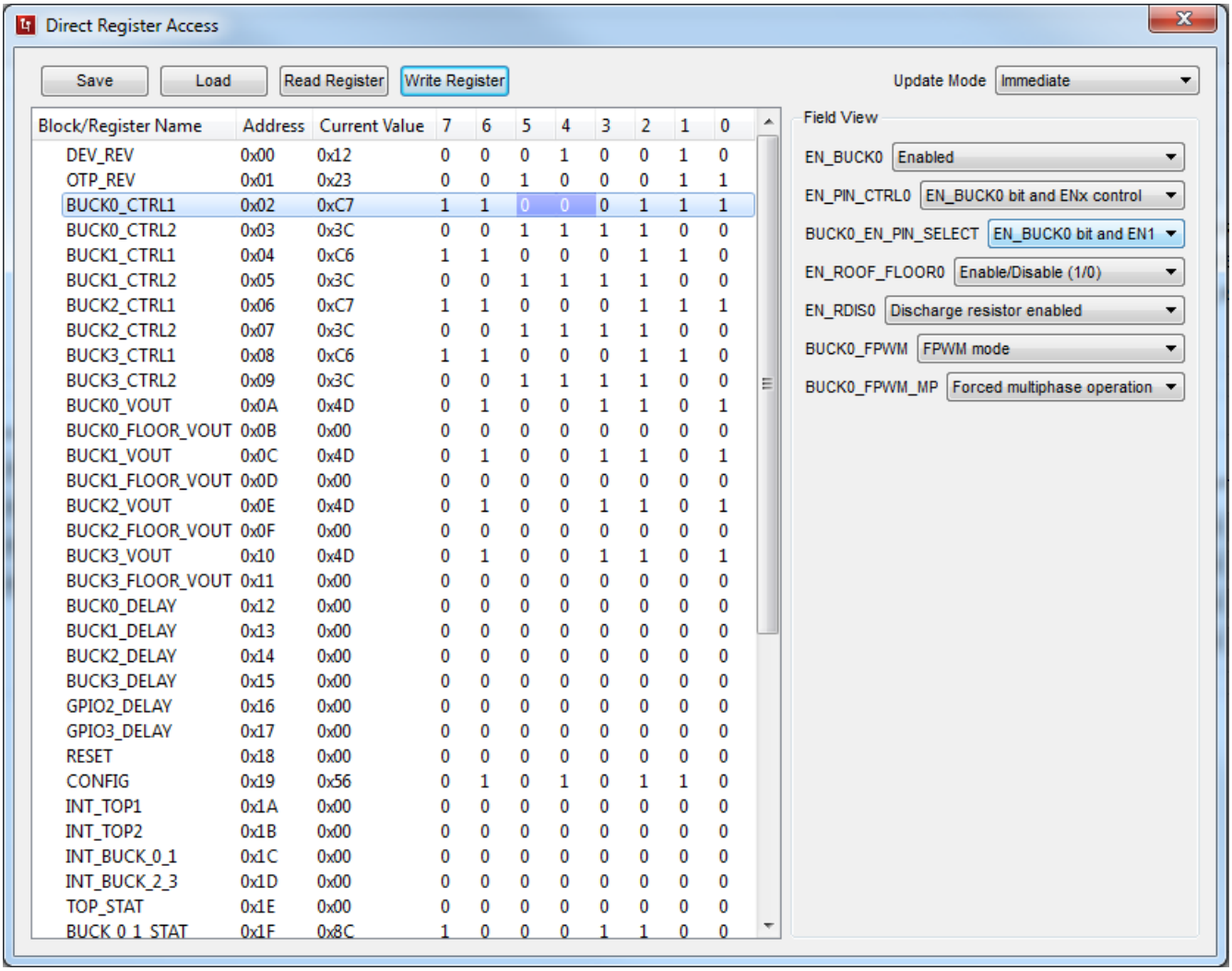


Figure 4-3. Selecting Register Values

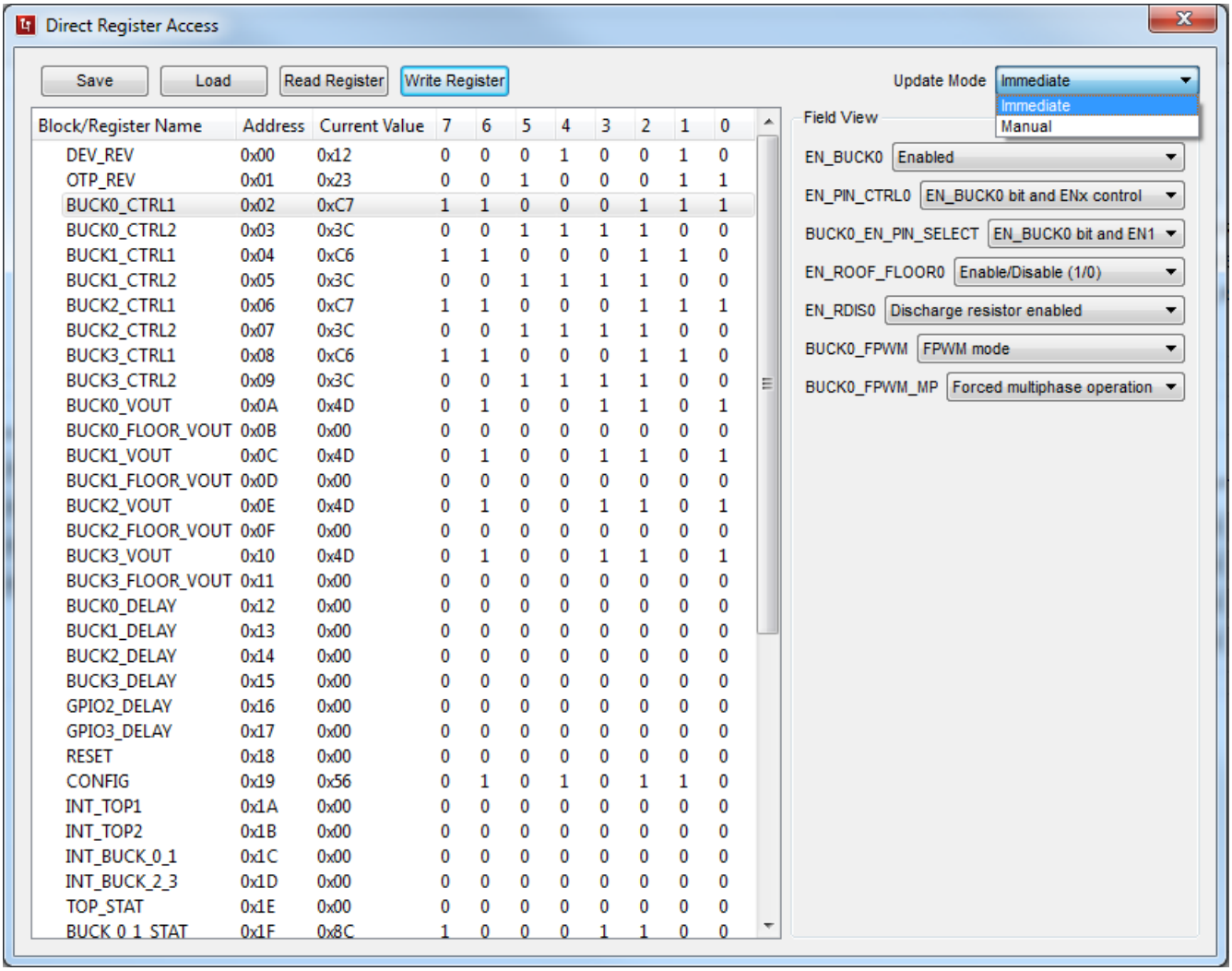


Figure 4-4. Register Update Mode

The *Configure* and *Advanced* tabs provide the user with pulldown menus and check-boxes for the part of the register space that is not covered by the Main tab, such as output voltage control. These controls are self-explanatory. Refer to the LP875761-Q1 data sheet for explanation of the functions. See following images for reference of the Config and Advanced tabs.

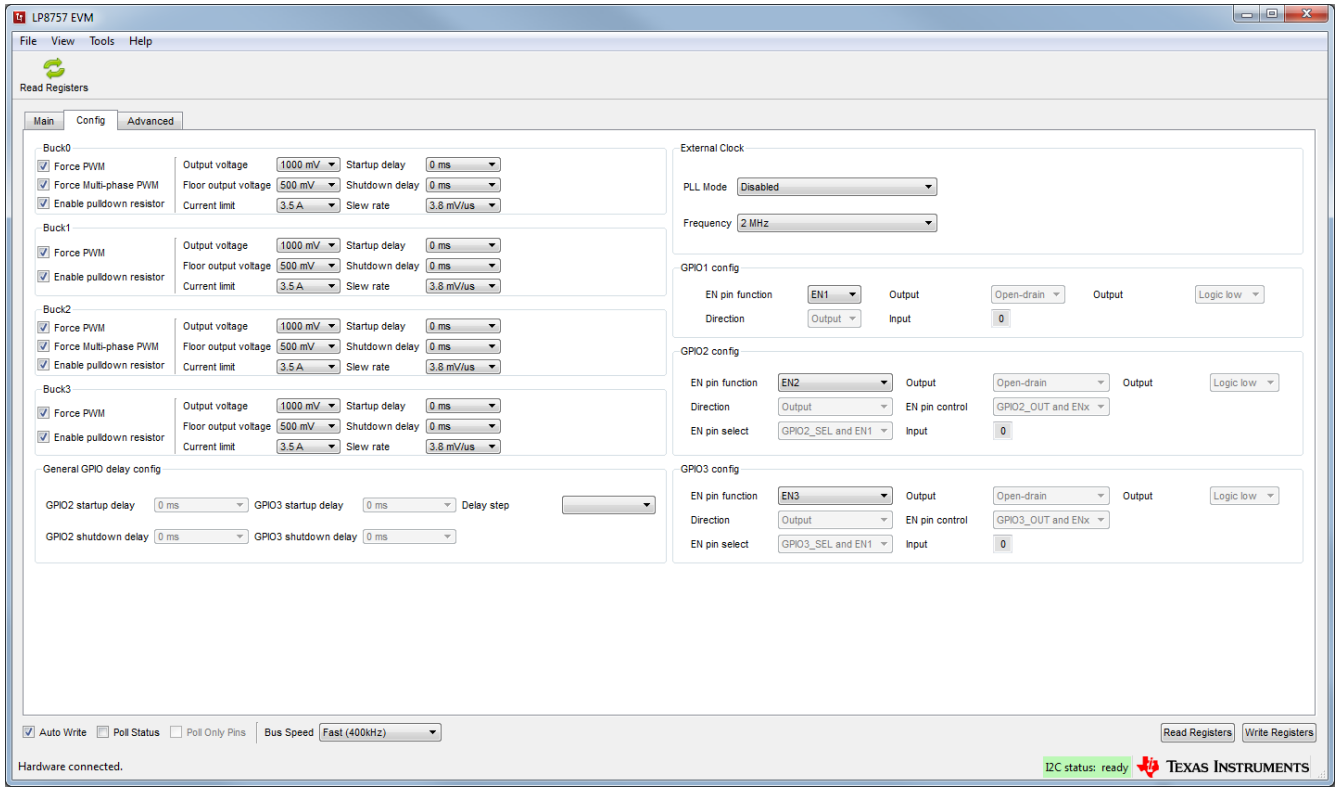


Figure 4-5. Config Tab of the LP8757 GUI

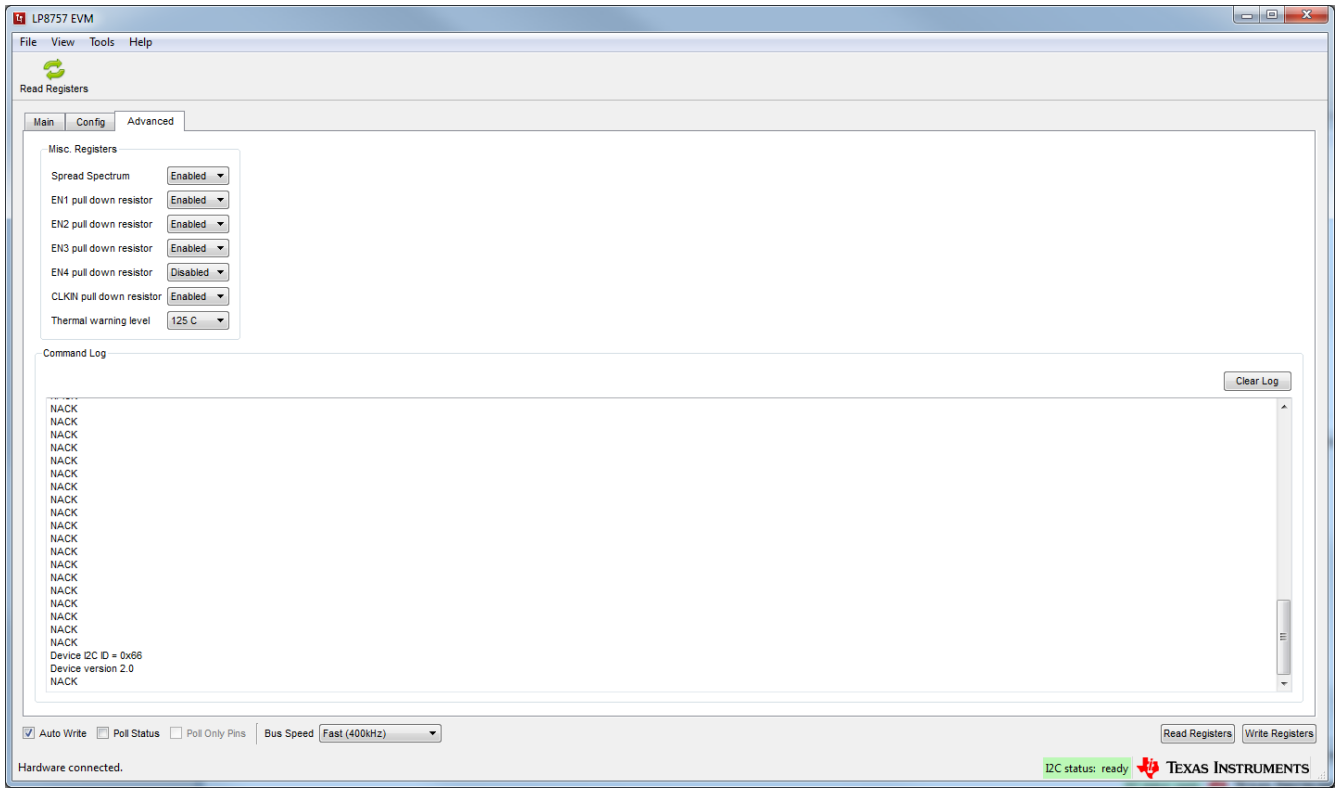


Figure 4-6. Advanced Tab of LP8757 GUI

4.3 Console

To show or hide the console, toggle the option in the View pulldown menu (see Figure 4-7). The console can be used to access the LP875761-Q1 registers. Registers can be read or written simply by referring to the logical registers by their name. See an example Figure 4-8. The console has a number of integrated macros that are listed in Table 4-3.

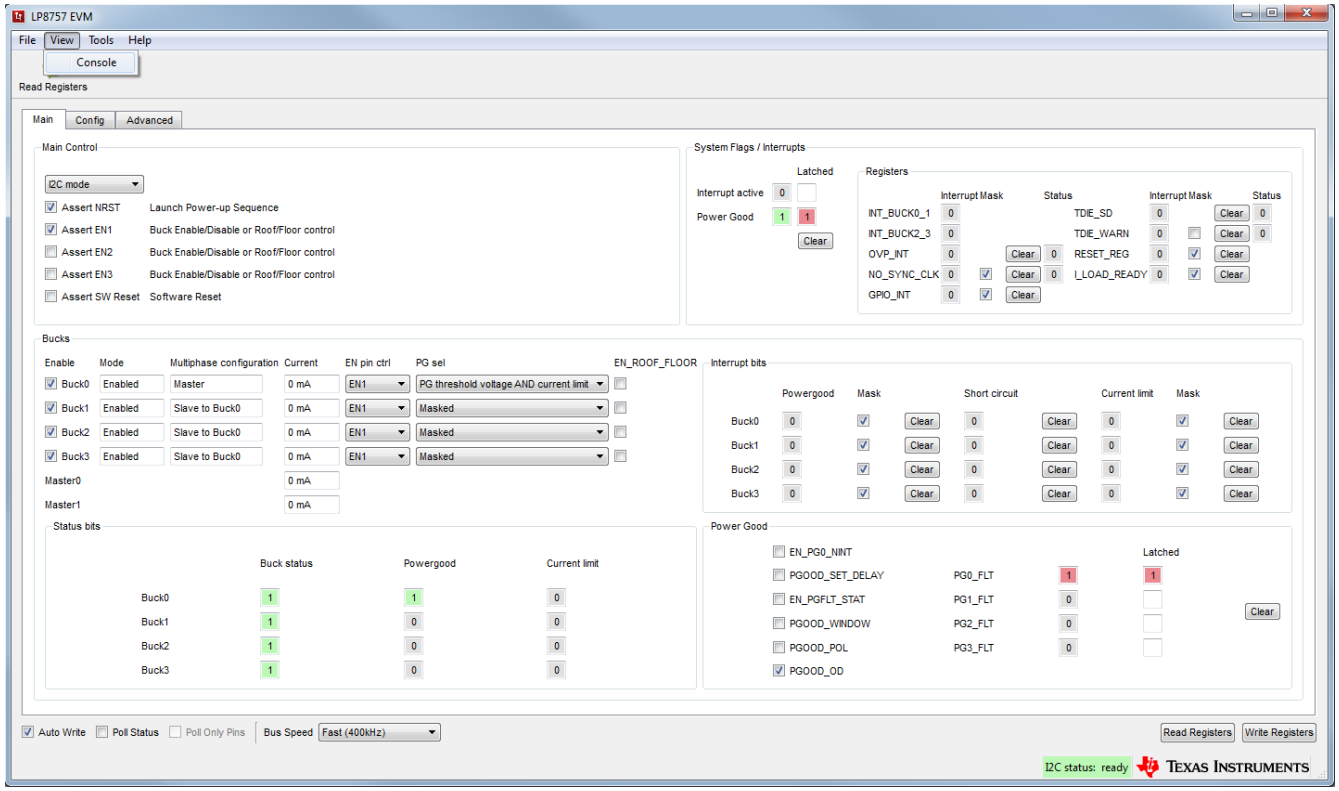


Figure 4-7. Opening Console

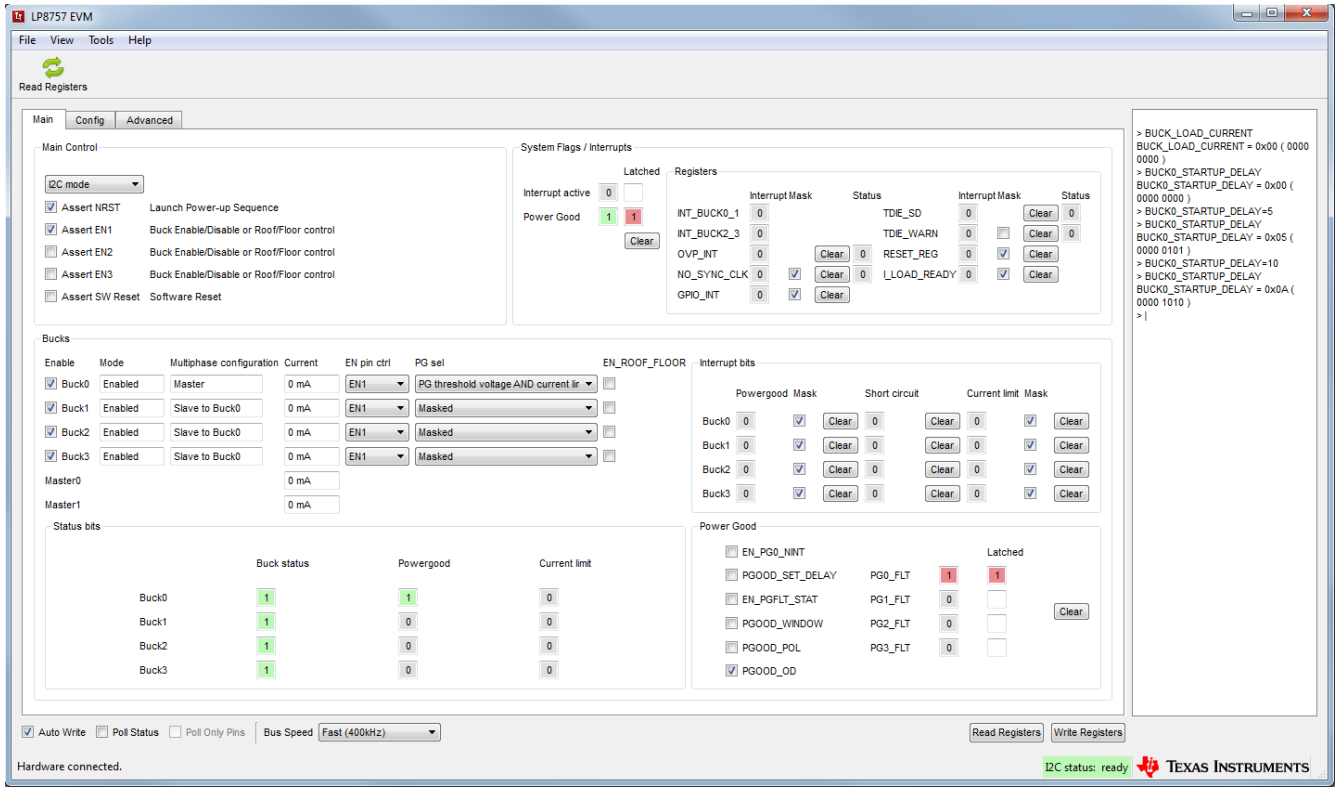


Figure 4-8. Example of Command Use in Console

Table 4-3. Console Macros

Command	Parameters	Explanation
register_name	= register value | -	Write a value to writable I^{2}C register or logical register. If no parameter given, will return the current register value. The logical register names are the same as given in the data sheet, and must be in uppercase. Example read: BUCK_LOAD_CURRENT; example write: BUCK0_STARTUP _DELAY = 10
wait	(time)	Wait for time given in ms. Useful in loops.
iout	(buck number)	Returns the measured load current of the chosen buck core.
0x	address = data or address[bits] = data	I^{2}C read or write command. addr = value examples: 0x12 = 0xaa 0x12[7] = 1 0x12[3:0] = 15

The console supports use of scripts. If a text file containing commands supported by the console is stored in the same folder with the evaluation software executable, then the script can be launched from the console by typing the text file name, like script.txt.

5 Bill of Materials

Table 5-1 lists EVM bill of materials. This is for output configurations listed in Table 2-1. See Section 7 for these configuration specific assembly details.

Note

The LP875761-Q1 I/O lines are connected to the microcontroller through 0-Ω resistors. These resistors are assembled to match the default I/O configuration of the LP875761-Q1. If LP875761-Q1 ENx/GPIOx or PGOOD pins are configured as push-pull outputs, corresponding 0-Ω resistors (R25, R27, R28, R29) must be removed to prevent possible damage to the microcontroller I/O pins. In open-drain configuration the microcontroller internal pullups are enabled by the GUI and pullup resistors R14 to R20 are not needed.

Table 5-1. Bill of Materials for LP875761Q1EVM

Designator	Description	Manufacturer	Part Number	Qty.
PCB	Printed Circuit Board	Any	BMC043	1
C1, C2, C3, C4, C30, C31, C32, C33, C34, C35, C38, C39, C40, C41, C42, C43, C46, C47, C48, C49, C50, C54, C55, C56, C57, C58, C66, C67	CAP, CERM, 22 µF, 10 V, ± 10%, X7R, AEC-Q200 Grade 1, 1206	MuRata	GCM31CR71A226KE02	28
C5, C6, C7, C8, C15, C16, C19, C20, C23, C24, C27, C28, C73, C80, C82, C88, C90	CAP, CERM, 10 µF, 10 V, ± 10%, X7R, AEC-Q200 Grade 1, 0805	MuRata	GCM21BR71A106KE22L	17
C9, C17, C21, C25, C29, C36, C44, C52, C60, C65, C72, C74, C75, C76, C77, C78, C79, C81, C83, C84, C85, C86, C89	CAP, CERM, 0.1 µF, 16 V,± 5%, X7R, AEC-Q200 Grade 1, 0402	MuRata	GCM155R71C104JA55D	23
C10, C11, C12, C13	CAP, CERM, 390 pF, 50 V,± 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	TDK	CGA2B2C0G1H391J050BA	4
C14, C18, C22, C26, C37, C45, C53, C61, C95	CAP, CERM, 0.01 µF, 50 V, ± 10%, C0G/NP0, AEC-Q200 Grade 1, 0402	MuRata	GCM155R71H103KA55D	9
C63	CAP, TA, 220 µF, 10 V, ± 10%, 0.15 Ω, SMD	AVX	TPSD227K010R0150	1
C64	CAP, CERM, 100 µF, 6.3 V, ± 20%, X5R, 0805	MuRata	GRM21BR60J107M	1
C69, C70, C71, C87	CAP, CERM, 15 pF, 100 V,± 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	MuRata	GCM1885C2A150JA16D	4
C91, C92, C93, C94	CAP, CERM, 1 µF, 25 V, ± 10%, X7R, AEC-Q200 Grade 1, 0603	MuRata	GCM188R71E105KA64D	4
D1	Diode, Zener, 5.6 V, 1 W, SMA	Diodes Inc.	SMAZ5V6-13-F	1
D2	Diode, Schottky, 30 V, 0.2 A, SOD-323	Diodes Inc.	BAT42WS-7-F	1
H1, H2, H3, H4	Bumpon, Hemisphere, 0.375 X 0.235, Black	3M	SJ61A2	4
H5	CABLE MINI USB 5PIN 1M 2.0 VERS	Assman WSW	AK672M/2-1-R	1
J2	Header, 100 mil, 2x2, Tin, SMT	Molex	15-91-2040	1
J3, J5, J8, J10, J11, J12, J14	Header, 2.54 mm, 2x1, Tin, SMT	Harwin	M20-8770246	7
J4, J13	Terminal Block, 2x1, 5 mm, Green, TH	Phoenix Contact	1935776	2
J15	Connector, Receptacle, Mini-USB Type B, R/A, Top Mount SMT	TE Connectivity	1734035-2	1
J16	Header, 100 mil, 3x1, Gold, SMT	Samtec	TSM-103-01-L-SV	1
L1, L2, L3, L4	Inductor, Shielded, 330 nH, 5.4 A, 0.017 Ω, AEC-Q200 Grade 1, SMD	MuRata Toko	DFE252012PD-R33M	4
L5, L6, L7, L8	Ferrite Bead, 30 Ω at 100 MHz, 4 A, 0805	MuRata	BLM21PG300SH1D	4

Table 5-1. Bill of Materials for LP875761Q1EVM (continued)

Designator	Description	Manufacturer	Part Number	Qty.
L9	Inductor, Wirewound, Ferrite, 10 µH, 0.12 A, 0.5 Ω, SMD	Taiyo Yuden	LB2012T100KR	1
LBL1	Thermal Transfer Printable Labels, 1.250" W x 0.250" H - 10,000 per roll	Brady	THT-13-457-10	1
R1, R2, R3, R4	RES, 3.9, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04023R90JNED	4
R5, R6, R7, R9, R10, R12, R21, R22, R23, R24, R25, R27, R28, R29	RES, 0, 5%, 0.063 W, 0402	Yageo America	RC0402JR-070RL	14
R8	RES, 0.01, 1%, 3 W, 2512	Bourns	CRA2512-FZ-R010ELF	1
R30	RES, 6.80 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-076K8L	1
R31, R32	RES, 39.0, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0739RL	2
R33	RES, 68.0 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0768KL	1
R34	RES, 33.0 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0733KL	1
R35	RES, 1.00, 1%, 0.1 W, 0603	Yageo America	RC0603FR-071RL	1
R36	RES, 470 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603470KJNEA	1
R37, R38	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06031K00FKEA	2
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5	Shunt, 100 mil, Gold plated, Black	TE Connectivity	881545-2	5
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14	Test Point, Miniature, SMT	Keystone	5015	14
U1	Four-Phase DC/DC Buck Converter, RNF0026C (VQFN-HR-26)	Texas Instruments	LP875761ARNFRQ1	1
U2	AT91SAM ARM-based Flash MCU, LQFP100	Atmel	ATSAM3U2CA-AU	1
U3	Dual Linear Regulator with 300 mA and 150 mA Outputs and Power-On-Reset, 10-pin LLP, Pb-Free	Texas Instruments	LP3996SD-1833/NOPB	1
Y1	Crystal, 12 MHz, 12pF, SMD	AVX	CX5032GB12000H0PESZZ	1
C51, C59	CAP, CERM, 22 µF, 10 V, ± 10%, X7R, AEC-Q200 Grade 1, 1206	MuRata	GCM31CR71A226KE02	0
C62, C68	CAP, CERM, 0.1 µF, 16 V,± 5%, X7R, AEC-Q200 Grade 1, 0402	MuRata	GCM155R71C104JA55D	0
J1, J6	Header, 100 mil, 2x1, Gold, TH	Samtec	TSW-102-07-G-S	0
J7	Terminal Block, 8x1, 2.54 mm, TH	Phoenix Contact	1725711	0
J9	Receptacle, 2.5 mm, 3x2, Gold, SMT	TE Connectivity	6651712-1	0
R11, R13, R26	RES, 0, 5%, 0.063 W, 0402	Yageo America	RC0402JR-070RL	0
R14, R15, R16, R17, R18, R19, R20	RES, 1.8 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06031K80JNEA	0

6 Board Layout

This section describes the board layout of the LP875761Q1EVM. See the LP875761-Q1 data sheet for specific PCB layout recommendations.

The board is constructed on a 4-layer PCB. using 55-µm copper on top and bottom layers to reduce resistance and improve heat transfer.

Board stack-up is shown in Figure 6-1. Figure 6-2 shows the top view of the entire board and Figure 6-3 through Figure 6-8 show the component placement, layout, and 3D view close to the LP875761-Q1 device.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.010mm	3.5	
3	Top Layer	Copper	0.055mm		
4	Dielectric1	FR-4	0.143mm	4.2	
5	MidLayer1	Copper	0.070mm		
6	Dielectric2	FR-4	0.960mm	4.2	
7	MidLayer2	Copper	0.070mm		
8	Dielectric3	FR-4	0.143mm	4.2	
9	Bottom Layer	Copper	0.055mm		
10	Bottom Solder	Solder Resist	0.010mm	3.5	
11	Bottom Overlay				

Figure 6-1. Board Stack-Up

The design utilizes dual side placement of the components. This allows placement of the inductors next to the LP875761-Q1 device for reducing SW node area for improved efficiency and reduced EMI. SW nets have also snubber components to reduce SW pin spiking and EMI. The input capacitors can be placed very close to the LP875761-Q1 device, to bottom side, to keep parasitic inductances low, and there is also space for input filters for further EMI reduction.

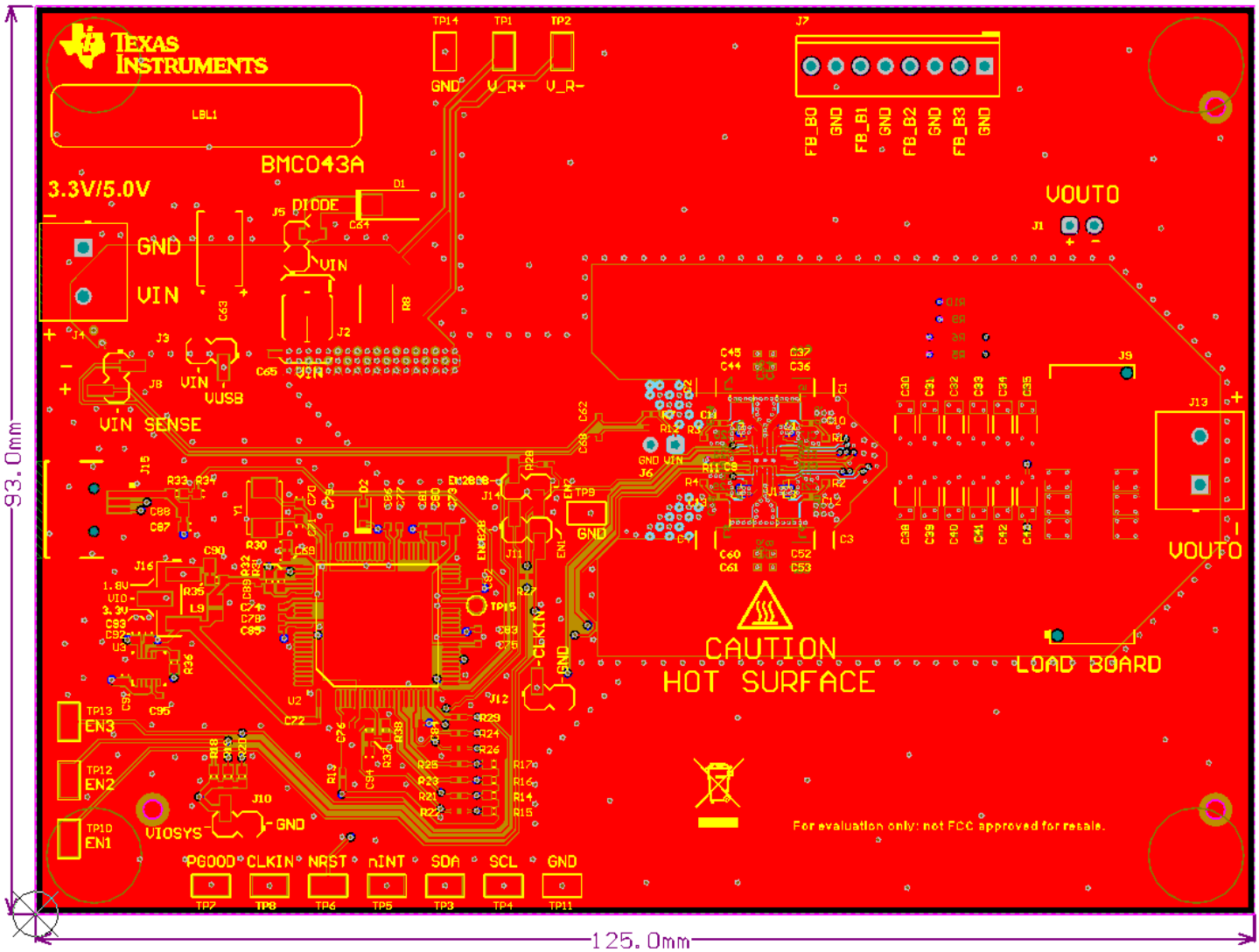


Figure 6-2. Top View of the LP875761-Q1EVM

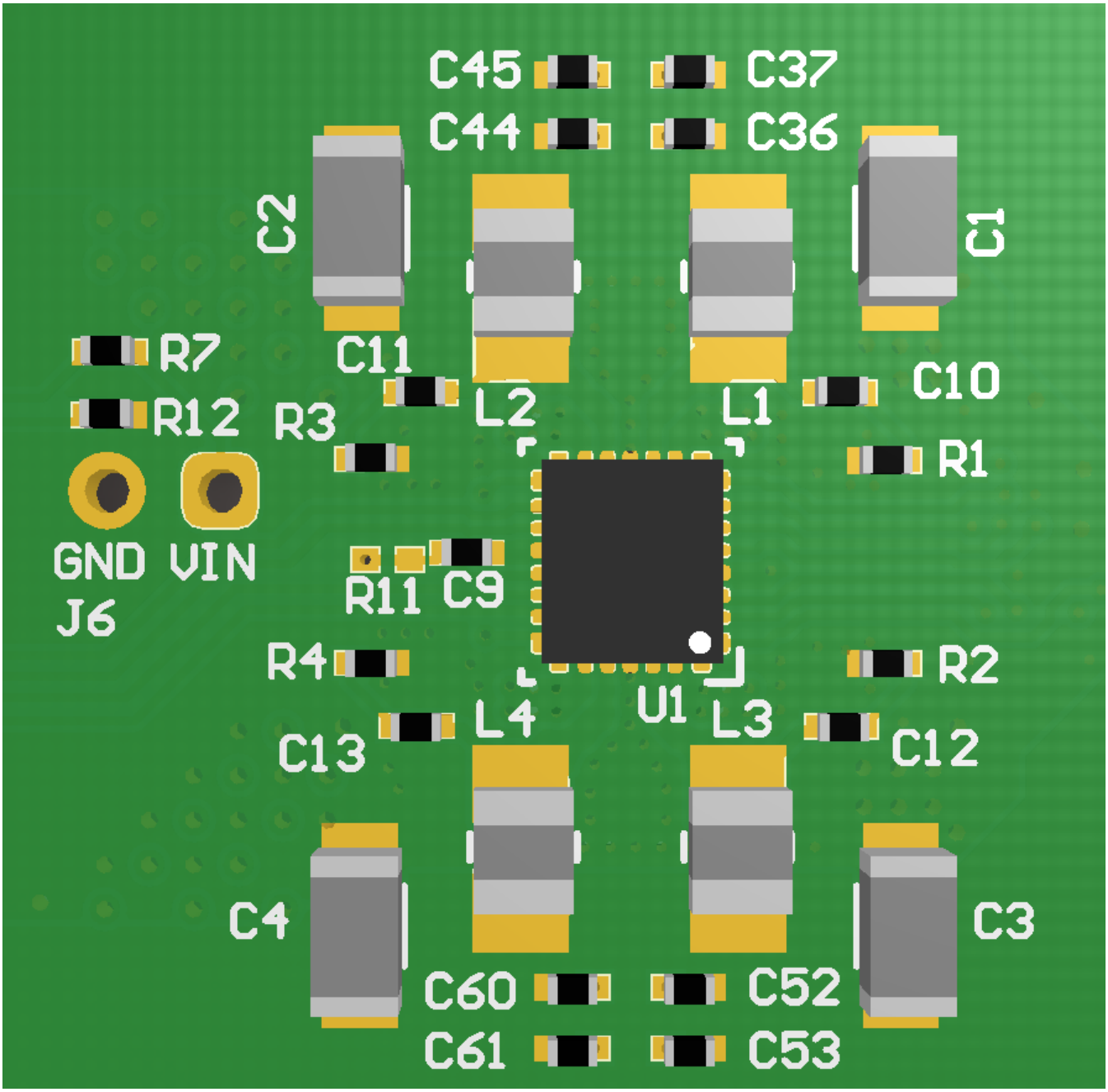


Figure 6-3. Component Placement Top Layer

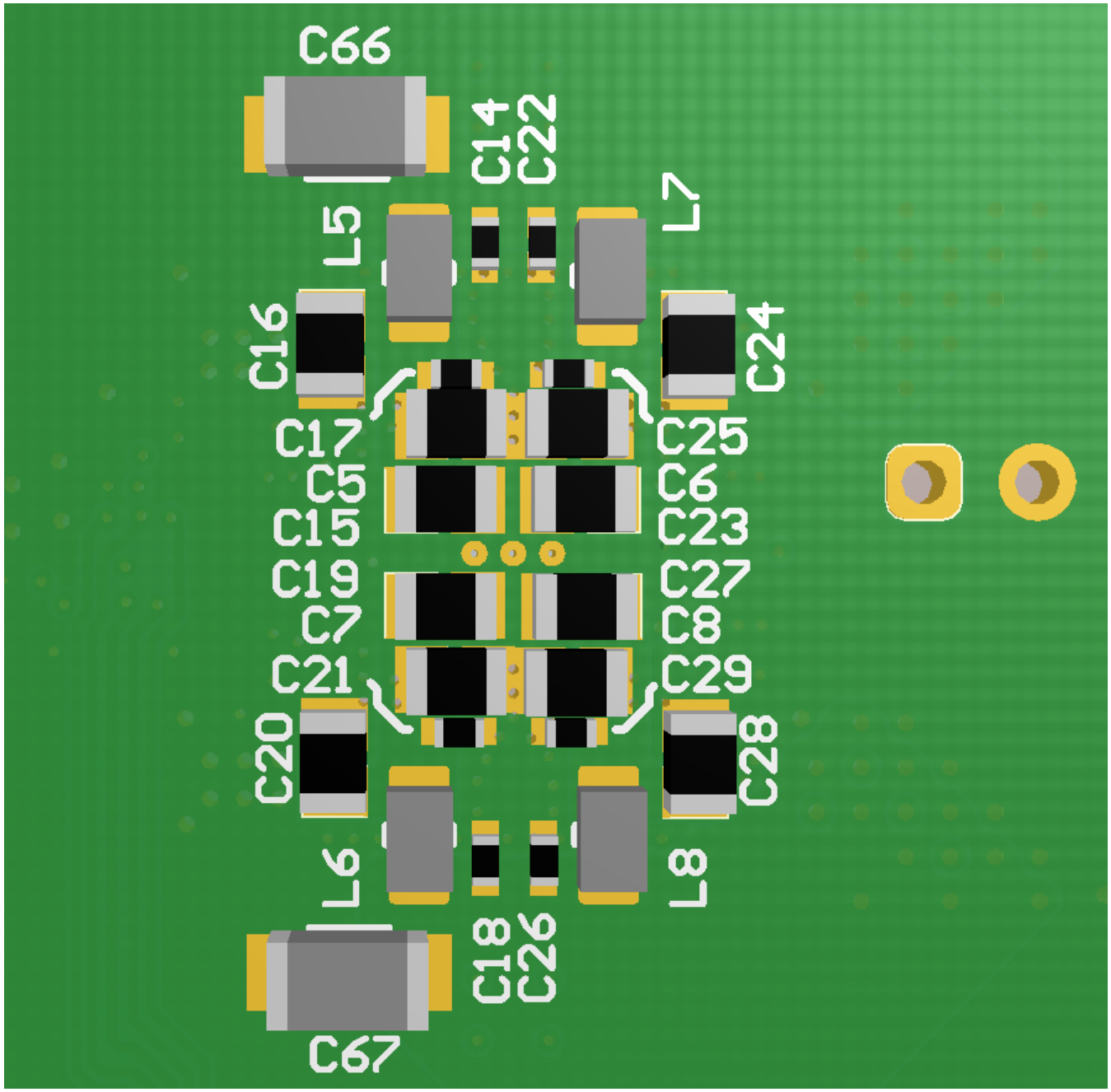
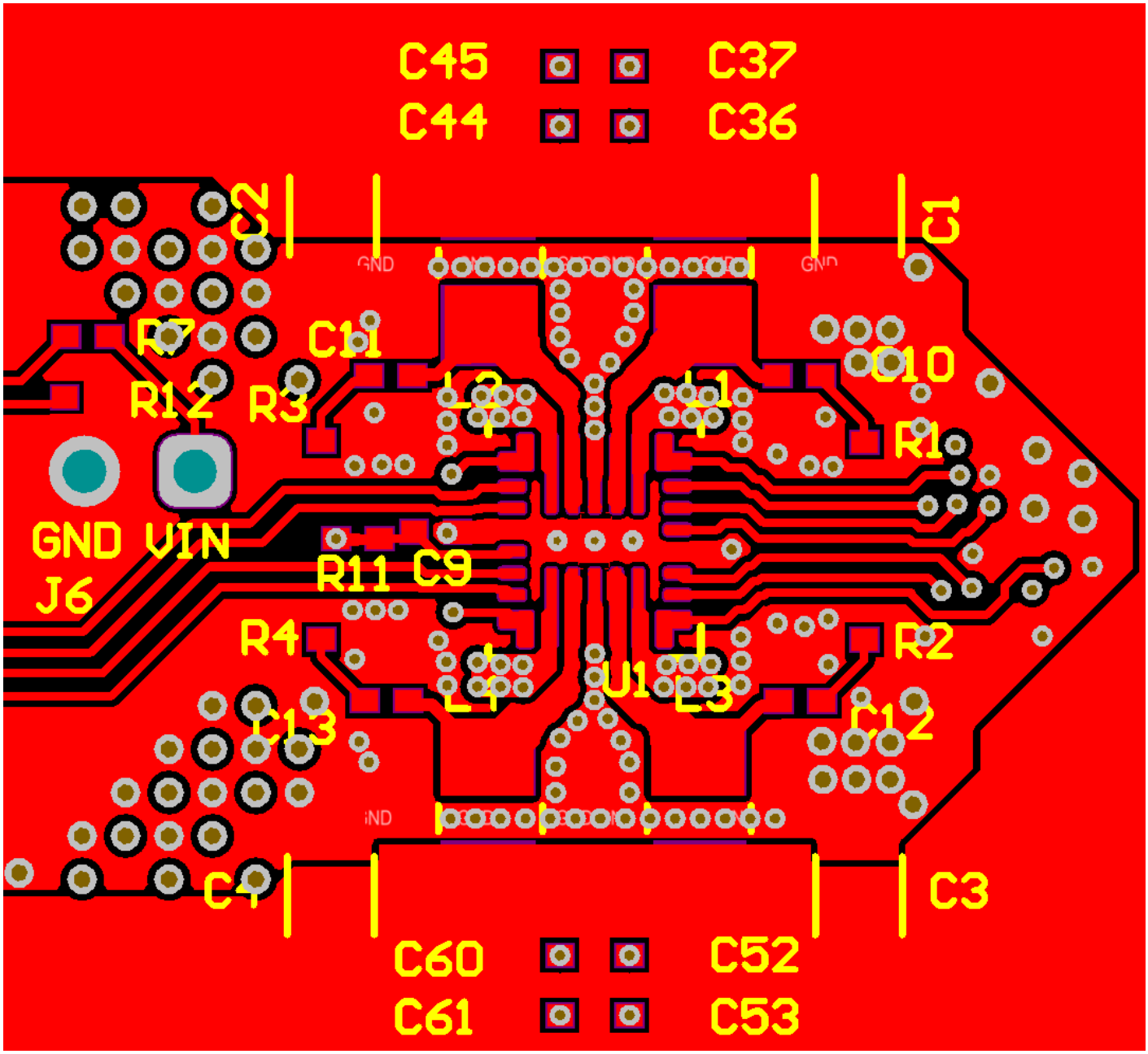
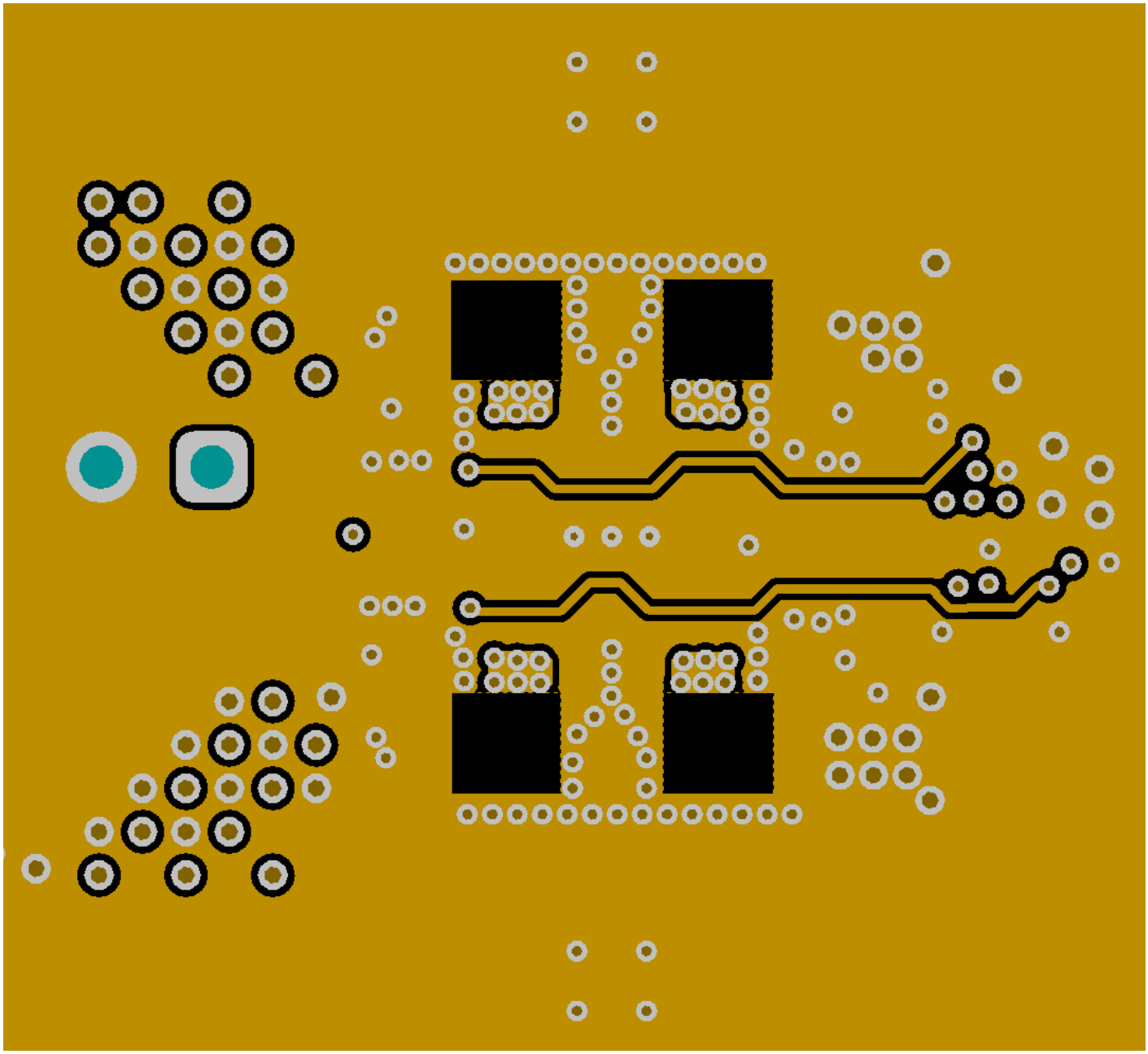


Figure 6-4. Component Placement Bottom Layer



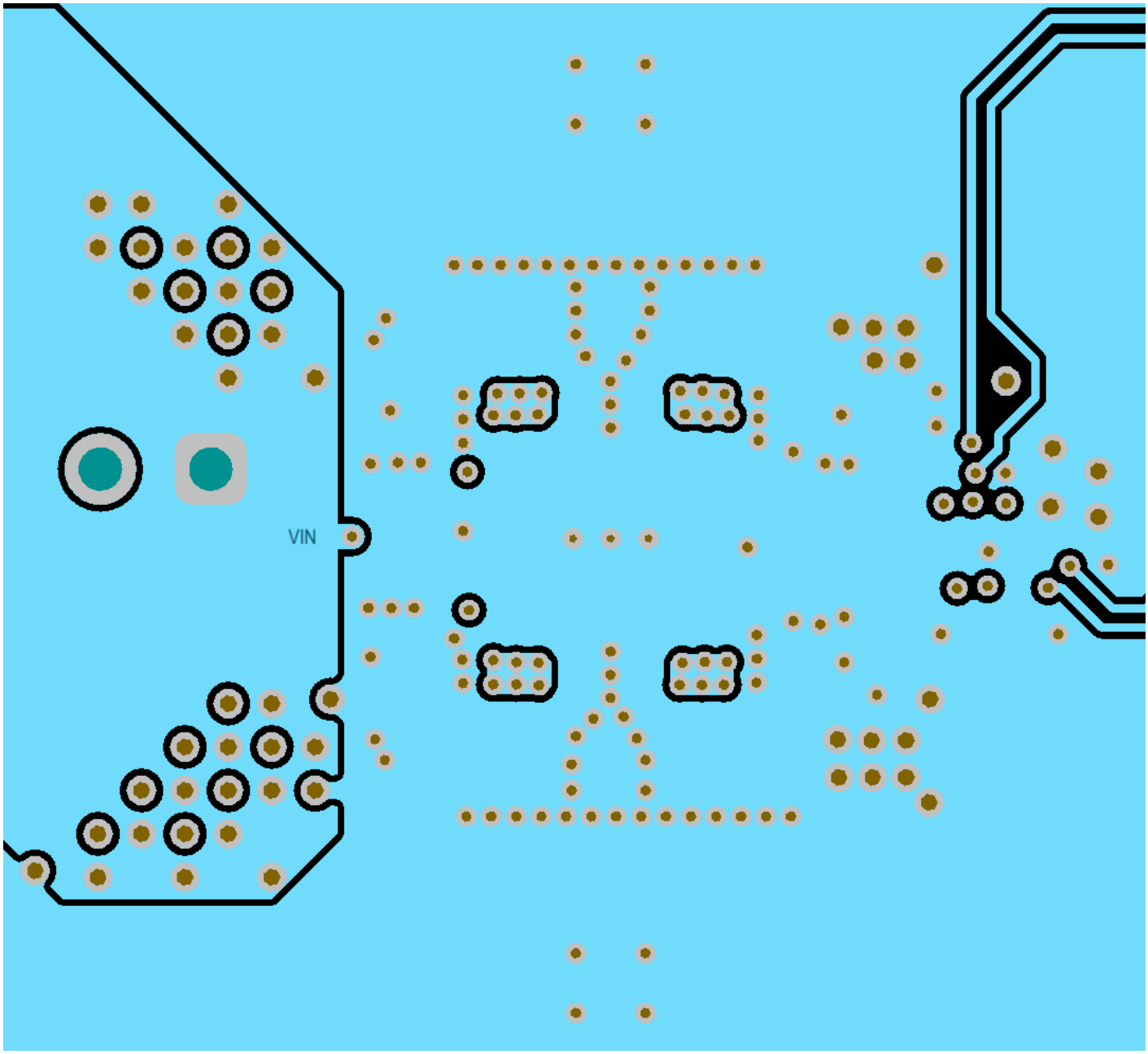
VIN nets are connected to bottom layer with multiple vias. This allows closer placement of the inductors, thus reducing SW node size and EMI. Also snubber circuits are placed next to SW nets for EMI reduction. Multiple GND vias are used to provide solid ground around the LP875761-Q1 device.

Figure 6-5. Top Layer



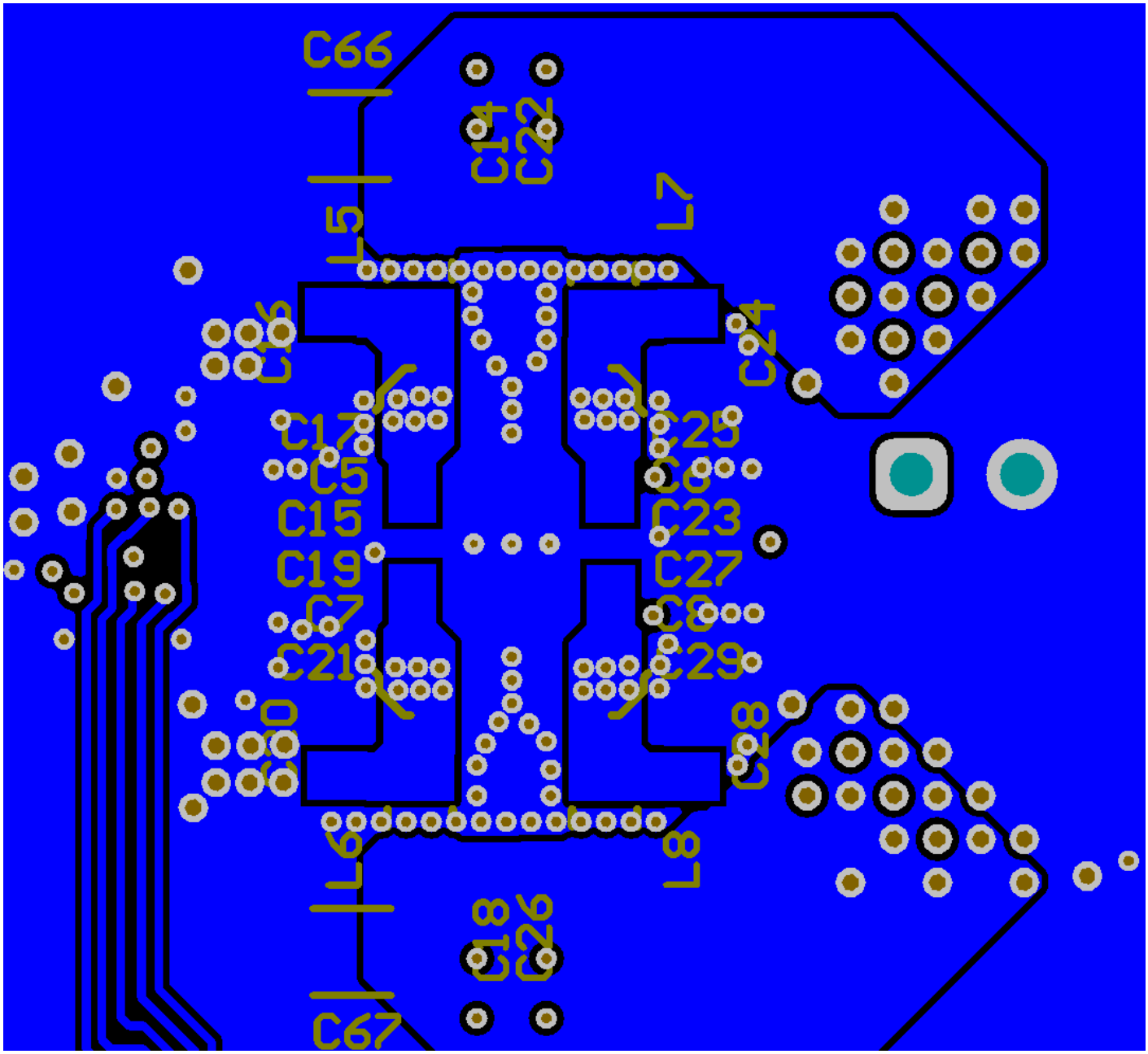
GND plane close to top layer (0.143 mm) helps to reduce parasitic inductance. Holes in the plane are under inductor footprint (SW node) to reduce parasitic capacitance of the SW node, thus reducing noise coupling and improving efficiency.

Figure 6-6. Mid-Layer1



VIN supply is routed in this layer between the ground planes to reduce radiated emissions. VIN and GND vias are placed in hatched pattern to avoid large gaps in these planes.

Figure 6-7. Mid-Layer2



Input capacitors and filters are placed under the LP875761-Q1 into bottom layer. This allows closer placement of the inductors and input components reducing SW and VIN net areas and improving EMI.

Figure 6-8. Bottom Layer (note mirror view)

7 LP875761Q1EVM Schematics

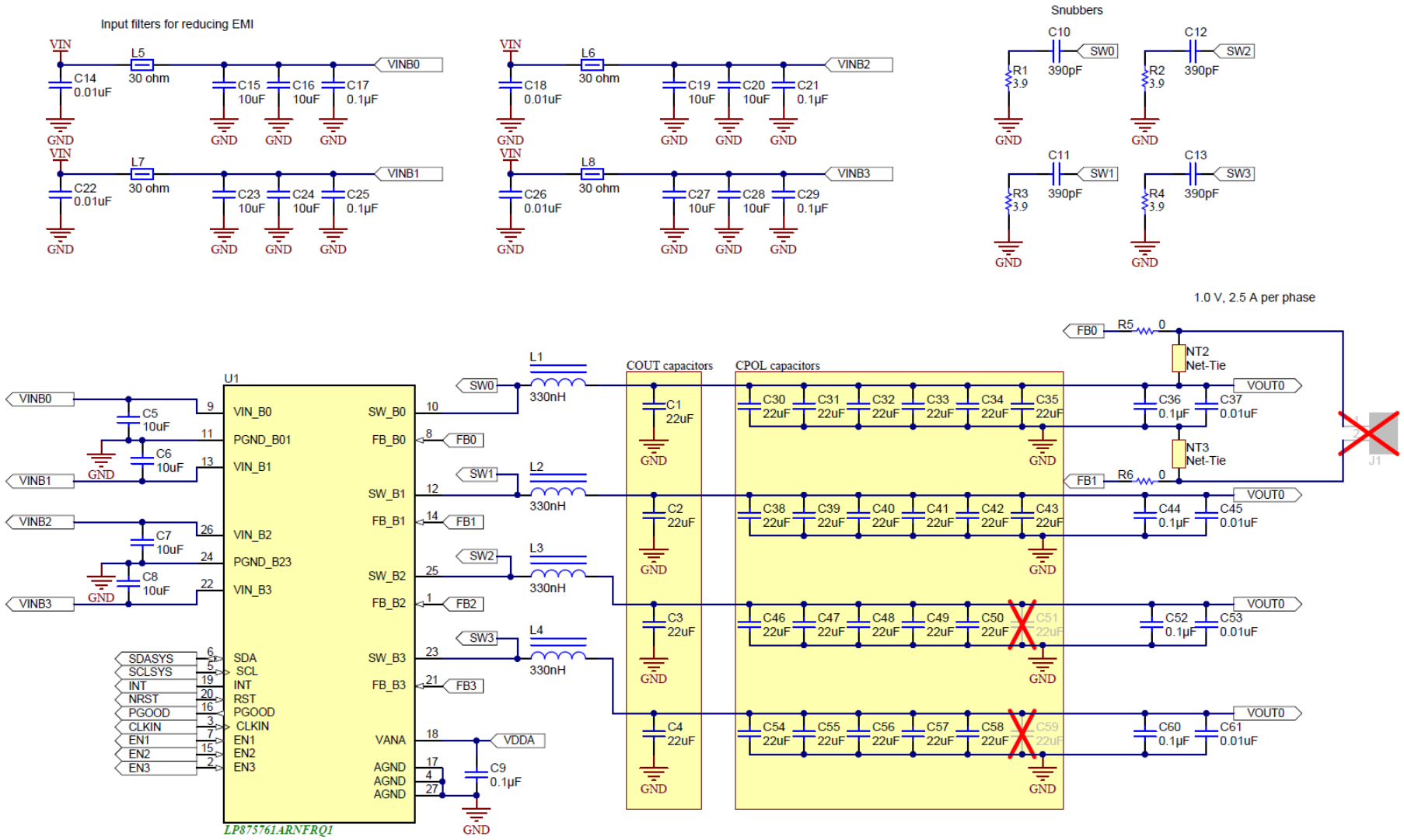


Figure 7-1. LP875761Q1EVM Schematic

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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