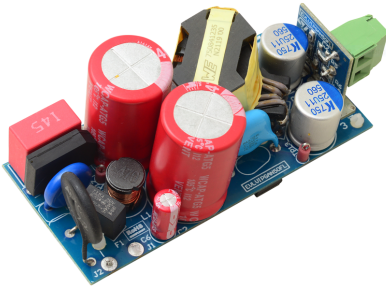


15 V / 50 W QR flyback converter based on VIPERGAN50



Features

- Universal input mains range: 90 – 265 V_{AC}
- Frequency: 50-60 Hz
- Output voltage: 15 V
- Output current: 3.35 A
- Stand-by mains consumption: < 85 mW at 230 V_{AC}
- Average efficiency: > 90%
- Tight line and load regulation over the entire input and output range
- Meets IEC55022 Class B conducted EMI even with reduced EMI filter, thanks to the frequency jittering feature
- RoHS compliant

Product status link

[EVLVIPGAN50FL](#)

Description

The [EVLVIPGAN50FL](#) evaluation board implements a 15 V-50 W SSR isolated flyback converter developed for general purpose application, operating from 90 to 265 V_{AC}.

The reference design is built around the VIPERGAN50, a new advanced offline high-voltage converter by STMicroelectronics, having the following features:

- 650 V PowerGaN with embedded senseFET (Si) and HV startup;
- QR operation with dynamic blanking time and adjustable valley synchronization delay functions, to maximize efficiency at any input line and load condition;
- Valley-lock to ensure constant valley skipping;
- Input voltage feedforward compensation for mains-independent OPP intervention;
- Adaptive burst mode for advanced power management in light load conditions;
- Frequency jittering for EMI suppression.

Enhanced system reliability is ensured by the built-in soft-start function and by the following set of protections:

- Input OVP (settable);
- Brown-in and brown-out (settable);
- Output OVP (settable);
- Output overload;
- OCP LEB;
- Embedded thermal shutdown.

The EVLVIPGAN50FL is composed of a main board and a daughterboard, whose schematics are shown in [Figure 1](#) and [Figure 2](#) respectively.

The main board contains, on the primary side, a diode bridge for double wave rectification, an input pi filter for EMI, a flyback transformer, the VIPERGAN50 and all the related components needed for polarization and features setting; on the secondary side, the output capacitors and the output rectifier, realized by a Power MOSFET driven by a synchronous rectifier for efficiency optimization.

1 Schematic diagram

Figure 1. EVLVIPGAN50FL schematic (mainboard)

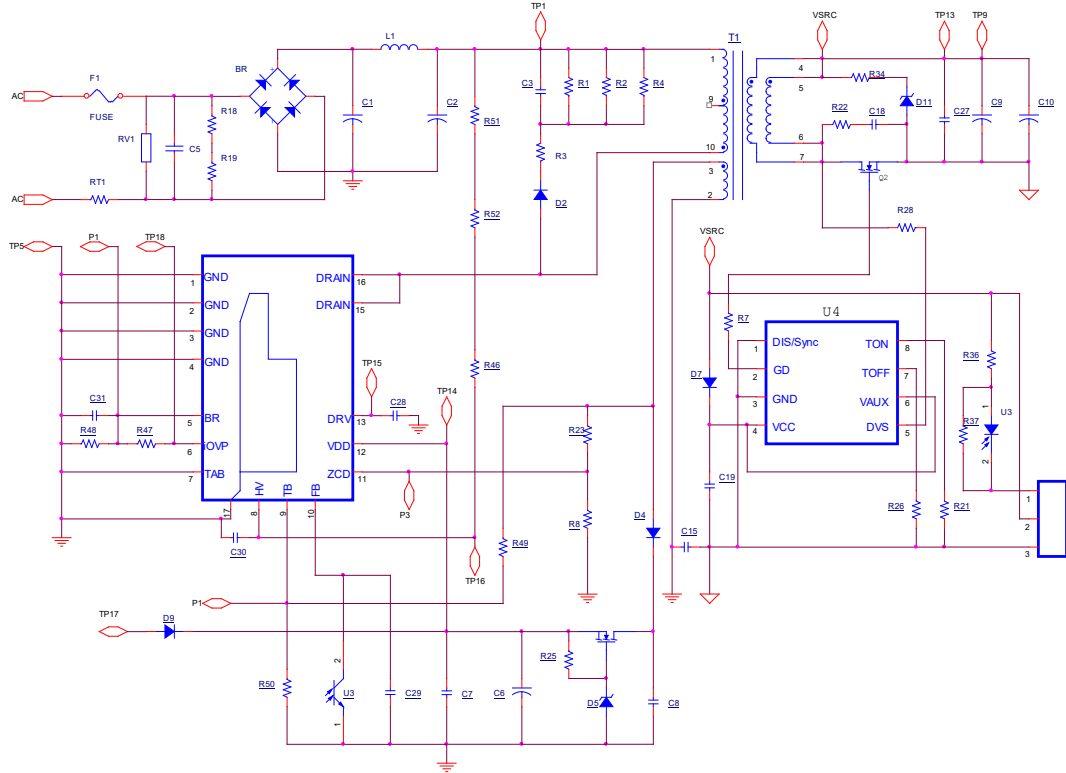
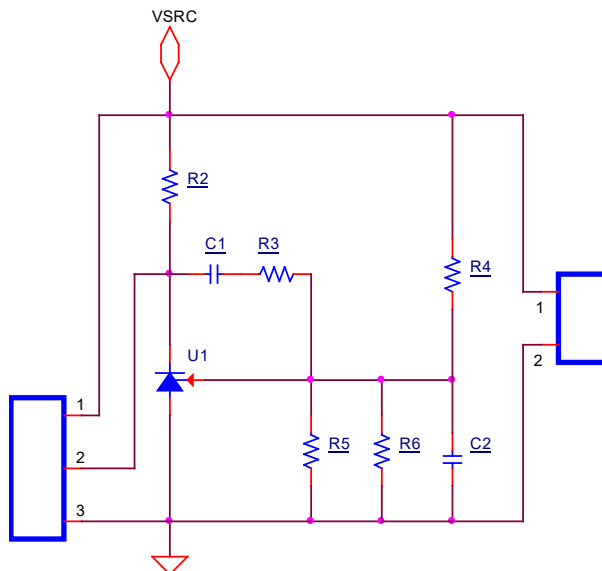


Figure 2. EVLVIPGAN50FL schematic (daughterboard)



Revision history

Table 1. Document revision history

Date	Version	Changes
05-Sep-2022	1	Initial release.

Contents

1 Schematic diagram	2
Revision history	3

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