BLC9H10XS-606A

Power LDMOS transistor

Rev. 1 — 24 March 2020

AMPLEON

Product data sheet

1. Product profile

1.1 General description

600 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 616 MHz to 960 MHz.

Table 1. Typical performance 634.5/737 MHz

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 50 V; I_{Dq} = 400 mA (main); $V_{GS(amp)peak}$ = 0.7 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	617 to 652	50	49.2	19.1	52.3	–33.5 [1][2]
	728 to 746	50	49.2	19.5	50.2	–35 [1][2]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

[2] Test data is based on wideband demo measurement (f = 617 MHz to 746 MHz).

Table 2. Typical performance 789.5 MHz

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 48 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.05 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	758 to 821	48	50.5	18.8	55.5	–29.3 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

Table 3. Typical performance 881.5 MHz

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 48 V; I_{Dq} = 400 mA (main); $V_{GS(amp)peak}$ = 0.05 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	869 to 894	48	50.5	17.9	53.2	–30.2 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

Table 4. Typical performance 942 MHz

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 48 V; I_{Dq} = 350 mA (main); $V_{GS(amp)peak}$ = 0.05 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	925 to 960	48	50.5	17.2	54.7	–29.2 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

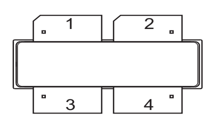
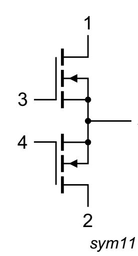
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 616 MHz to 960 MHz frequency range

2. Pinning information

Table 5. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 6. Ordering information

Type number	Package		
	Name	Description	Version
BLC9H10XS-606A	-	plastic earless flanged cavity package; 4 leads	SOT1250-4

4. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–6	+11	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–6	+11	V

Table 7. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	[1]	–40	+150	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 50 V; I_{Dq} = 600 mA (main); $V_{GS(amp)peak}$ = 0.5 V; T_{case} = 80 °C		
		P_L = 112 W	0.236	K/W
		P_L = 141 W	0.198	K/W

6. Characteristics

Table 9. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.5 mA	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 150 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 47 V; I_D = 600 mA	-	2	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	24.5	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 7.5 A	-	9.8	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 5.25 A	-	160	203	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3 mA	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 300 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 47 V; I_D = 1200 mA	-	2	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	49.0	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 15.0 A	-	18.7	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 10.5 A	-	82	107	mΩ

Table 10. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 760.5 MHz; f_2 = 800.5 MHz; RF performance at V_{DS} = 48 V; I_{Dq} = 550 mA (main); $V_{GS(amp)peak}$ = 0.5 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 758 MHz to 803 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 107 W	16.8	18	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 107 W	-	–13	–8	dB
η_D	drain efficiency	$P_{L(AV)}$ = 107 W	48	53.8	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 107 W	-	–31	–26	dBc

Table 11. RF characteristics

Test signal: pulsed CW, t_p = 100 μs; δ = 10 %; f = 803 MHz; RF performance at V_{DS} = 48 V; I_{Dq} = 550 mA; $V_{GS(amp)peak}$ = 0.5 V; T_{case} = 25 °C; unless otherwise specified; in a Doherty production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression	-	485	630	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC9H10XS-606A is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 48 V; I_{Dq} = 550 mA; $V_{GS(amp)peak}$ = 0.5 V; f = 758 MHz; P_L = 200 W (5 dB OBO); 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH.

7.2 Impedance information

Table 12. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 900 mA (main); V_{DS} = 48 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
780	4.3 – j4.5	1.6 + j0.2	304	66.0	19.1
800	4.4 – j4.9	1.6 + j0.2	303	64.7	19.1
820	4.6 – j5.3	1.6 + j0.2	303	65.0	19.2
840	4.7 – j5.6	1.6 + j0.2	308	65.6	19.1
Maximum drain efficiency load					
780	4.3 – j4.5	2.0 + j1.0	244	70.7	20.8
800	4.4 – j4.9	1.4 + j1.0	233	70.1	20.7
820	4.6 – j5.3	1.4 + j1.2	209	72.2	21.2
840	4.7 – j5.6	1.4 + j1.2	206	72.5	21.2

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 13. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 1800 mA (peak); V_{DS} = 48 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
780	2.5 – j2.8	1.0 – j0.1	620	65.7	17.8
800	2.5 – j3.0	1.0 – j0.1	633	65.9	17.8
820	2.7 – j3.2	1.0 – j0.1	631	64.8	17.6
840	2.7 – j3.3	1.0 – j0.1	639	64.8	17.7
Maximum drain efficiency load					
780	2.5 – j2.8	0.6 + j0.6	371	75.6	20.5
800	2.5 – j3.0	0.6 + j0.6	375	78.8	20.8
820	2.7 – j3.2	0.6 + j0.4	447	77.9	19.5
840	2.7 – j3.3	0.6 + j0.4	447	77.2	19.8

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

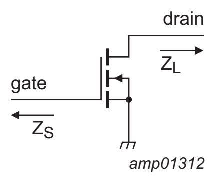
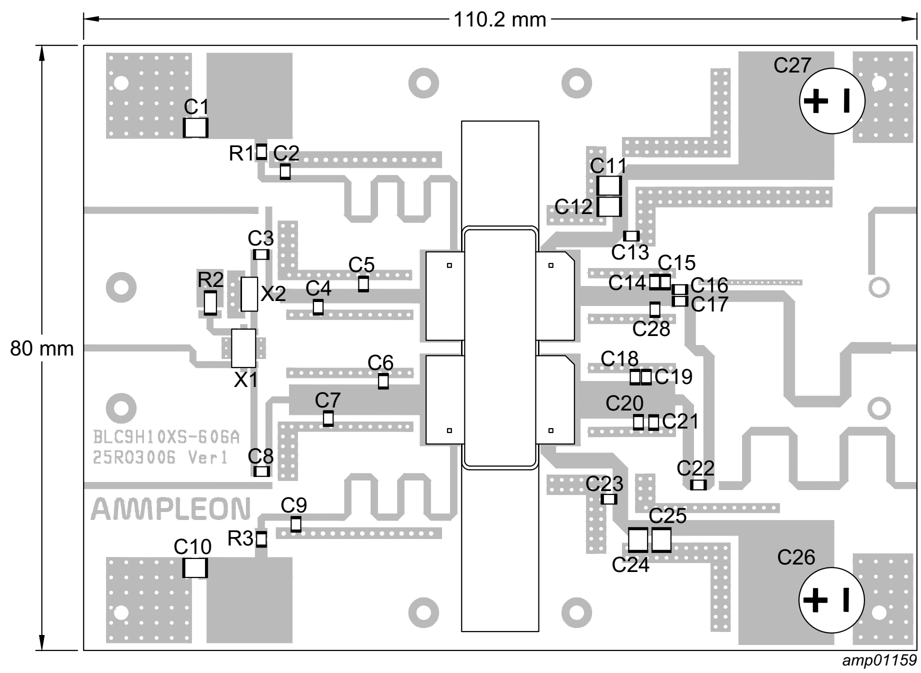


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): RO3006: ε_r = 6.15; thickness = 0.635 mm; thickness copper plating = 35 μm. See Table 14 for a list of components.

Fig 2. Component layout

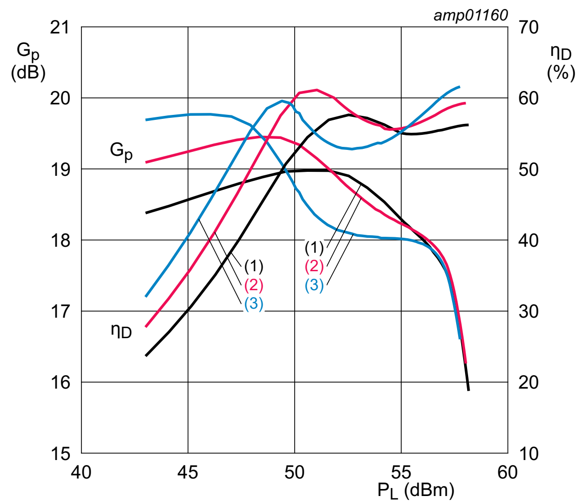
Table 14. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C10	multilayer ceramic chip capacitor	10 μF, 50 V	Murata: Hi-Q SMD 1210
C2, C3, C8, C9, C13, C22, C23	multilayer ceramic chip capacitor	68 pF	Murata: Hi-Q SMD 0805
C4	multilayer ceramic chip capacitor	3.9 pF	Murata: Hi-Q SMD 0805
C5, C15	multilayer ceramic chip capacitor	4.7 pF	Murata: Hi-Q SMD 0805
C6, C7	multilayer ceramic chip capacitor	5.6 pF	Murata: Hi-Q SMD 0805
C11, C12, C24, C25	multilayer ceramic chip capacitor	10 μF, 100 V	Murata: Hi-Q SMD 1210
C14	multilayer ceramic chip capacitor	4.3 pF	Murata: Hi-Q SMD 0805
C16, C17, C18	multilayer ceramic chip capacitor	5.1 pF	Murata: Hi-Q SMD 0805
C19, C28	multilayer ceramic chip capacitor	6.2 pF	Murata: Hi-Q SMD 0805
C20	multilayer ceramic chip capacitor	1 pF	Murata: Hi-Q SMD 0805
C21	multilayer ceramic chip capacitor	10 pF	Murata: Hi-Q SMD 0805
C26, C27	electrolytic capacitor	1000 μF, 100 V	
R1, R3	resistor	5.1 Ω	SMD 0805
R2	resistor	50 Ω	SMD 2512
X1	hybrid coupler	2 dB, 90°	X3C7F1-02S
X2	attenuator	1 dB; 10 W	D10AA1Z4

7.4 Graphical data

7.4.1 Pulsed CW



V_{DS} = 48 V; I_{Dq} = 550 mA; $V_{GS(amp)peak}$ = 0.5 V; t_p = 100 μs; δ = 10 %.

(1) f = 758 MHz

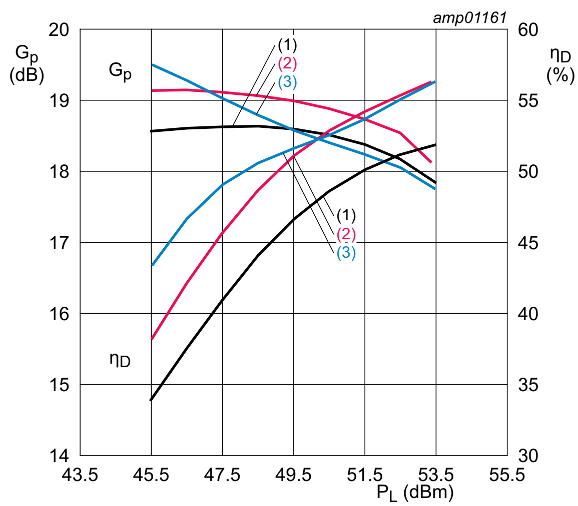
(2) f = 780 MHz

(3) f = 803 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values

7.4.2 1-Carrier W-CDMA

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB per carrier at 0.01 % probability on CCDF; 3GPP test model 1; 1 to 64 DPCH.



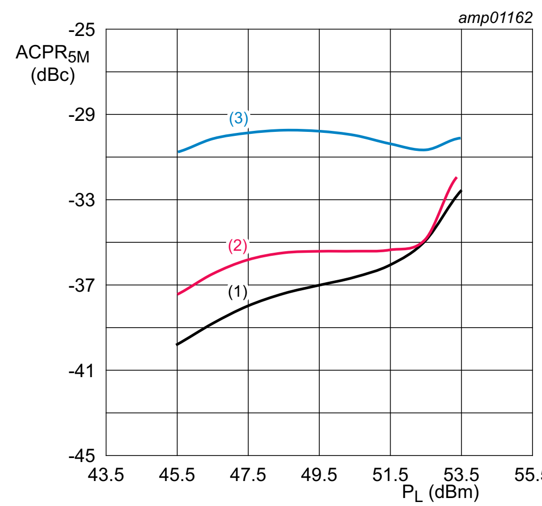
V_{DS} = 48 V; I_{Dq} = 550 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 760.5 MHz

(2) f = 780 MHz

(3) f = 800.5 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



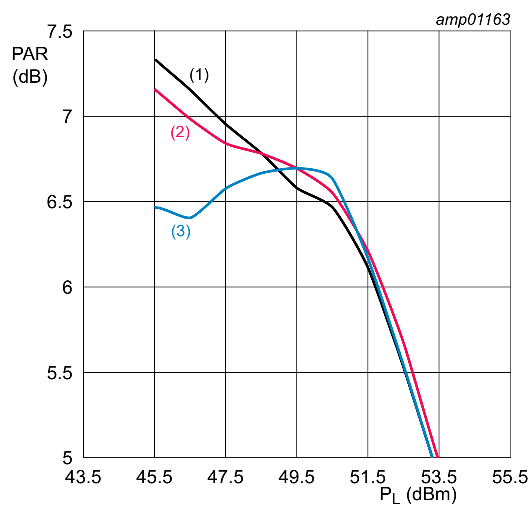
V_{DS} = 48 V; I_{Dq} = 550 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 760.5 MHz

(2) f = 780 MHz

(3) f = 800.5 MHz

Fig 5. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 48 V; I_{Dq} = 550 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 760.5 MHz

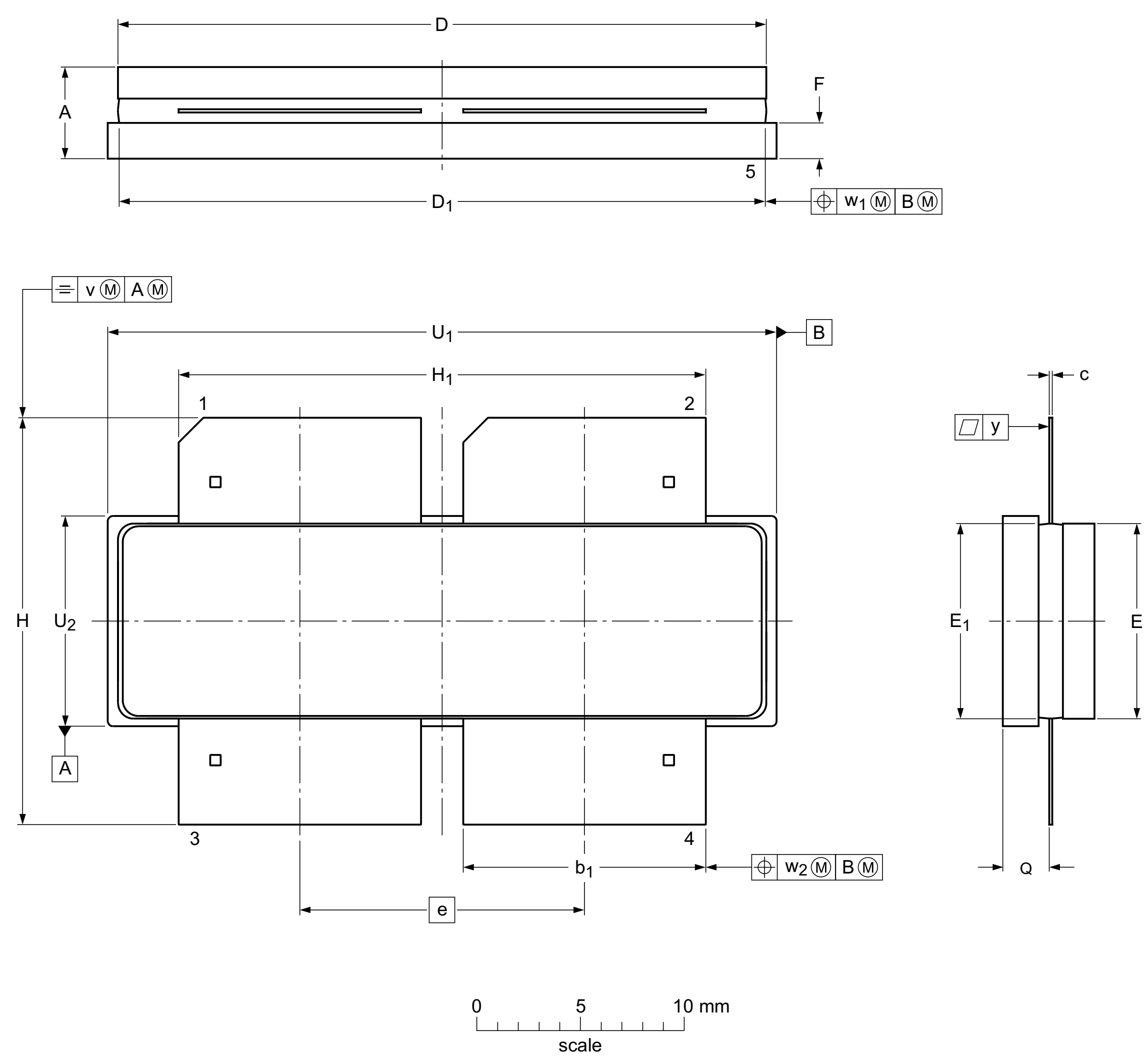
(2) f = 780 MHz

(3) f = 800.5 MHz

Fig 6. Peak-to-average power ratio as a function of output power; typical values

8. Package outline

Plastic earless flanged cavity package; 4 leads **SOT1250-4**



Dimensions

Unit		A	b_1	c	D	D_1	E	E_1	e	F	H	H_1	Q[(1)]	U_1	U_2	v	w_1	w_2	y
mm	max	4.52	11.79	0.18	31.44	31.34	9.60	9.50		1.73	19.71	25.50	2.25	32.33	10.23	0.50	0.50	0.50	0.10
	nom								13.72										
	min	4.12	11.58	0.13	31.04	31.14	9.20	9.30		1.53	19.51	25.30	2.03	32.13	10.03				

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1250-4_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1250-4						19-01-17

Fig 7. Package outline SOT1250-4

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 15. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of ≥ 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 16. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9H10XS-606A v.1	20200324	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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For sales office addresses, please visit: **http://www.ampleon.com/sales**

14. Contents

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Date of release: 24 March 2020

Document identifier: BLC9H10XS-606A