

SN74HC595B 8-Bit Shift Registers With 3-State Output Registers

1 Features

- 8-Bit Serial-In, Parallel-Out Shift Registers
- Available in Ultra Small Logic QFN package(0.5 mm max height)
- Over-Voltage Tolerant on Inputs Independent of V_{CC}
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads
- Low Power Consumption: 80- μ A (Maximum) I_{CC}
- $t_{pd} = 13$ ns (Typical)
- ± 6 -mA Output Drive at 5 V
- Low Input Current: 1 μ A (Maximum)
- Shift Register Has Direct Clear
- -55°C to 125°C Operating Temperature

2 Applications

- Network Switches
- Factory Automation
- Mobile Wearables
- Industrial Building Automation
- Power Infrastructure
- LED Displays
- Servers

3 Description

The SN74HC595B devices contain an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift register and storage register. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and serial outputs for cascading. When the output-enable (\overline{OE}) input is high, the all outputs are in the high-impedance state except Q_H .

Table 1. Device Information

PART NUMBER	PACKAGE (PINS)	BODY SIZE (NOM)
SN74HC595BRWN	X1QFN (16)	2.50 mm x 2.50 mm

(1) For available package, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

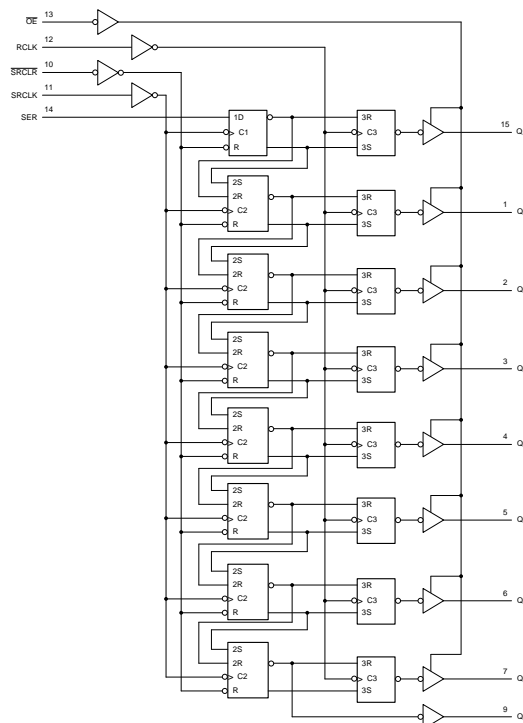


Table of Contents

1 Features	1	7.2 Functional Block Diagram	12
2 Applications	1	7.3 Feature Description	13
3 Description	1	7.4 Device Functional Modes	13
4 Pin Configuration and Functions	3	8 Application and Implementation	14
5 Specifications	4	8.1 Application Information	14
5.1 Absolute Maximum Ratings	4	8.2 Typical Application	14
5.2 ESD Ratings	4	9 Power Supply Recommendations	16
5.3 Recommended Operating Conditions	4	10 Layout	16
5.4 Thermal Information	5	10.1 Layout Guidelines	16
5.5 Electrical Characteristics	5	10.2 Layout Example	16
5.6 Timing Requirements	6	11 Device and Documentation Support	17
5.7 Switching Characteristics	7	11.1 Documentation Support	17
5.8 Operating Characteristics	8	11.2 Community Resources	17
5.9 Typical Characteristics	9	11.3 Trademarks	17
6 Parameter Measurement Information	10	11.4 Electrostatic Discharge Caution	17
7 Detailed Description	11	11.5 Glossary	17
7.1 Overview	11	12 Mechanical, Packaging, and Orderable Information	17

4 Pin Configuration and Functions

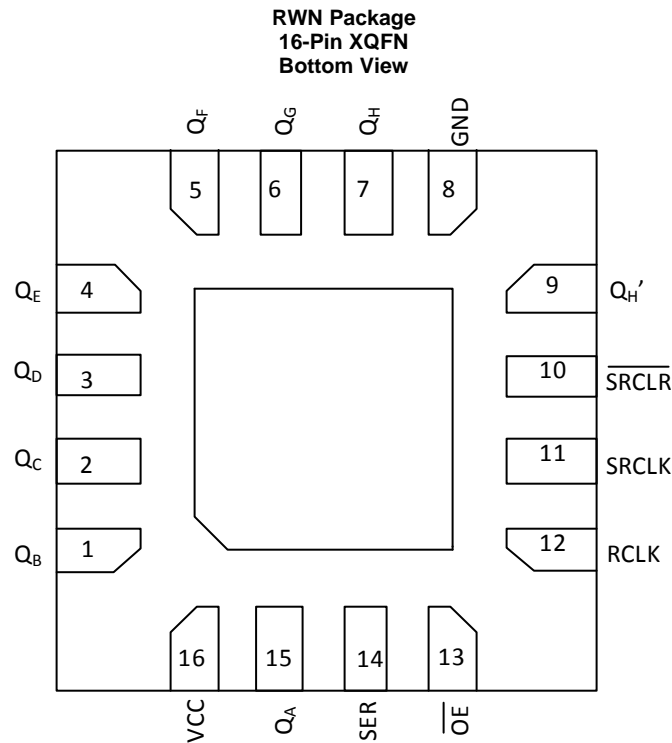


Table 2. Pin Functions

PIN		I/O	DESCRIPTION
NAME	RWN		
GND	8	—	Ground Pin
\overline{OE}	13	I	Output Enable; does not control Q_H'
Q_A	15	O	Q_A Output
Q_B	1	O	Q_B Output
Q_C	2	O	Q_C Output
Q_D	3	O	Q_D Output
Q_E	4	O	Q_E Output
Q_F	5	O	Q_F Output
Q_G	6	O	Q_G Output
Q_H	7	O	Q_H Output
Q_H'	9	O	Q_H' Output
RCLK	12	I	RCLK Input
SER	14	I	SER Input
SRCLK	11	I	SRCLK Input
\overline{SRCLR}	10	I	\overline{SRCLR} Input
V_{CC}	16	—	Power Pin

5 Specifications

5.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	-0.5	7	V	
V _I	Input voltage	-0.5	7	V	
I _{IK}	Input clamp current ⁽¹⁾	V _I < 0	-20	mA	
I _{OK}	Output clamp current ⁽²⁾	V _O < 0 or V _O > V _{CC}	±20	mA	
I _O	Continuous output current	V _O = 0 to V _{CC}	±35	mA	
Continuous current through V _{CC} or GND			±70	mA	
T _J	Junction temperature		150	°C	
T _{stg}	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN74HC595B			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 4.5 V	3.15		
		V _{CC} = 6 V	4.2		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	V
		V _{CC} = 4.5 V		1.35	
		V _{CC} = 6 V		1.8	
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
Δt/Δv	Input transition rise or fall time ⁽²⁾	V _{CC} = 2 V		1000	ns
		V _{CC} = 4.5 V		500	
		V _{CC} = 6 V		400	
T _A	Operating free-air temperature		-55	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).
- (2) If this device is used in the threshold region (from V_{IL} max = 0.5 V to V_{IH} min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_i = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74HC595B	UNIT
		RWN (X1QFN)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112	°C/W
$R_{\theta JCTop}$	Junction-to-case (top) thermal resistance	47.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	72.4	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	72.4	
$R_{\theta JCbott}$	Junction-to-case (bottom) thermal resistance	32.2	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -55^\circ\text{C to } 125^\circ\text{C}$		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	2 V	$I_{OH} = -20 \mu\text{A}$			1.9	1.998	1.9	1.9	V
			4.5 V			4.4	4.499	4.4	4.4	
			6 V			5.9	5.999	5.9	5.9	
		4.5 V	$Q_H, I_{OH} = -4 \text{ mA}$			3.98	4.3	3.7	3.84	
			$Q_A - Q_H, I_{OH} = -6 \text{ mA}$			3.98	4.3	3.7	3.84	
			$Q_H, I_{OH} = -5.2 \text{ mA}$			5.48	5.8	5.2	5.34	
6 V	$Q_A - Q_H, I_{OH} = -7.8 \text{ mA}$			5.48	5.8	5.2	5.34			
	V_{OL}	2 V	$I_{OL} = 20 \mu\text{A}$			0.002	0.1	0.1	0.1	V
			4.5 V			0.001	0.1	0.1	0.1	
6 V			0.001	0.1	0.1	0.1				
4.5 V		$Q_H, I_{OL} = 4 \text{ mA}$			0.17	0.26	0.4	0.33		
		$Q_A - Q_H, I_{OL} = 6 \text{ mA}$			0.17	0.26	0.4	0.33		
		$Q_H, I_{OL} = 5.2 \text{ mA}$			0.15	0.26	0.4	0.33		
6 V	$Q_A - Q_H, I_{OL} = 7.8 \text{ mA}$			0.15	0.26	0.4	0.33			
	I_I	$V_I = V_{CC}$ or 0	6 V	± 0.1	± 100	± 1000	± 1000	nA		
I_{OZ}	$V_O = V_{CC}$ or 0, $Q_A - Q_H$	6 V	± 0.01	± 0.5	± 10	± 5	μA			
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V		8	160	80	μA			
C_i		2 V to 6 V		3	10	10	10	pF		

5.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

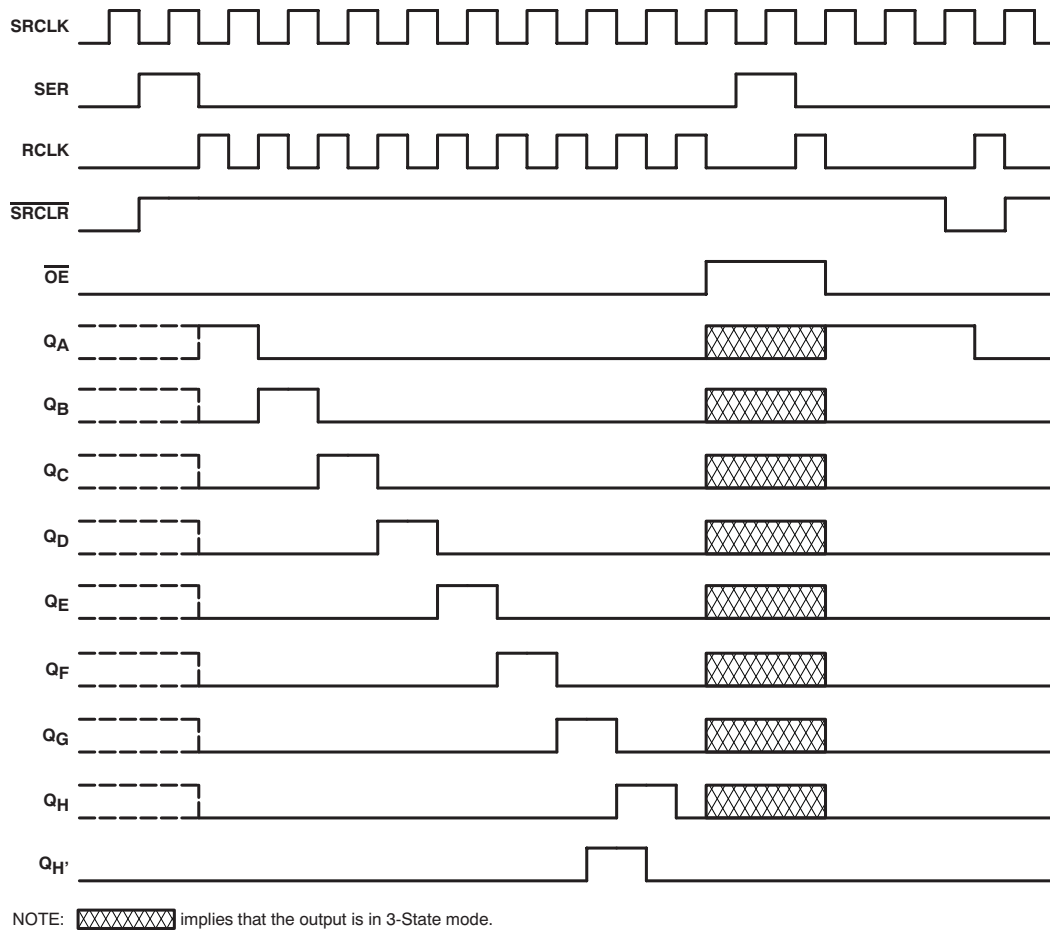
		V _{CC}	T _A = 25°C		T _A = -55°C to 125°C		T _A = -40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	2 V	6		4.2		5		MHz
		4.5 V	31		21		25		
		6 V	36		25		29		
t _w	SRCLK or RCLK high or low	2 V	80	120		100		ns	
		4.5 V	16	24		20			
		6 V	14	20		17			
	$\overline{\text{SRCLR}}$ low	2 V	80	120		100			
		4.5 V	16	24		20			
		6 V	14	20		17			
t _{su}	SER before SRCLK↑	2 V	100	150		125		ns	
		4.5 V	20	30		25			
		6 V	17	25		21			
	SRCLK↑ before RCLK↑ ⁽¹⁾	2 V	75	113		94			
		4.5 V	15	23		19			
		6 V	13	19		16			
	$\overline{\text{SRCLR}}$ low before RCLK↑	2 V	50	75		65			
		4.5 V	10	15		13			
		6 V	9	13		11			
	$\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑	2 V	50	75		60			
		4.5 V	10	15		12			
		6 V	9	13		11			
t _h	Hold time, SER after SRCLK↑	2 V	0	0		0		ns	
		4.5 V	0	0		0			
		6 V	0	0		0			

(1) This set-up time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

5.7 Switching Characteristics

Over recommended operating free-air temperature range.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			T _A = -55°C to 125°C		T _A = -40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			50 pF	2 V	6	26		4.2		5	MHz	
				4.5 V	31	38		21		25		
				6 V	36	42		25		29		
t _{pd}	SRCLK	Q _{H'}	50 pF	2 V		50	160		240		200	ns
				4.5 V		17	32		48		40	
				6 V		14	27		41		34	
	RCLK	Q _A – Q _H	50 pF	2 V		50	150		225		187	
				4.5 V		17	30		45		37	
				6 V		14	26		38		32	
t _{PHL}	$\overline{\text{SRCLR}}$	Q _{H'}	50 pF	2 V		51	175		261		219	ns
				4.5 V		18	35		52		44	
				6 V		15	30		44		37	
t _{en}	$\overline{\text{OE}}$	Q _A – Q _H	50 pF	2 V		40	150		255		187	ns
				4.5 V		15	30		45		37	
				6 V		13	26		38		32	
t _{dis}	$\overline{\text{OE}}$	Q _A – Q _H	50 pF	2 V		42	200		300		250	ns
				4.5 V		23	40		60		50	
				6 V		20	34		51		43	
t _t		Q _A – Q _H	50 pF	2 V		28	60		90		75	ns
				4.5 V		8	12		18		15	
				6 V		6	10		15		13	
		Q _{H'}	50 pF	2 V		28	75		110		95	
				4.5 V		8	15		22		19	
				6 V		6	13		19		16	
t _{pd}	RCLK	Q _A – Q _H	150 pf	2 V		60	200		300		250	ns
				4.5 V		22	40		60		50	
				6 V		19	34		51		43	
t _{en}	$\overline{\text{OE}}$	Q _A – Q _H	150 pf	2 V		70	200		298		250	ns
				4.5 V		23	40		60		50	
				6 V		19	34		51		43	
t _t		Q _A – Q _H	150 pf	2 V		45	210		315		265	ns
				4.5 V		17	42		63		53	
				6 V		13	36		53		45	

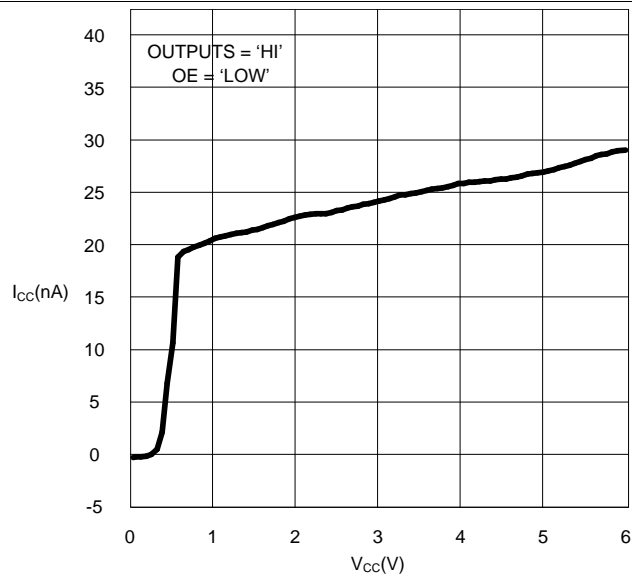

Figure 1. Timing Diagram

5.8 Operating Characteristics

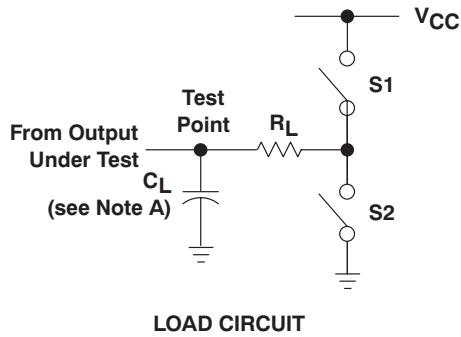
 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	400	pF

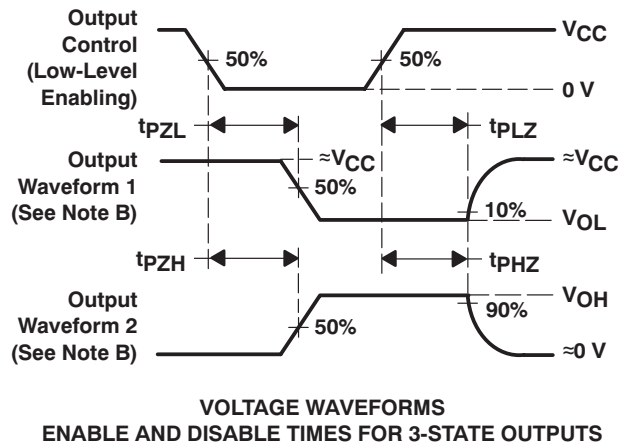
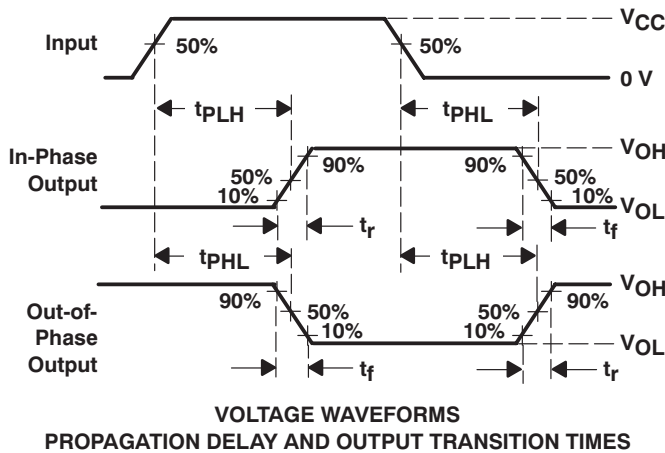
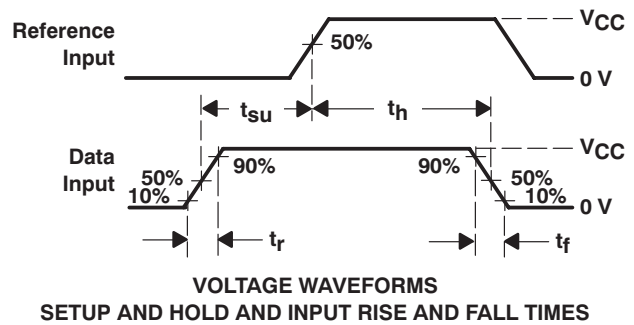
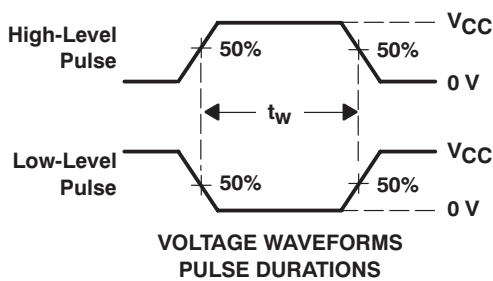
5.9 Typical Characteristics



6 Parameter Measurement Information



PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t		50 pF or 150 pF	Open	Open



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - E. The outputs are measured one at a time, with one input transition per measurement.
 - F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74HC595B is part of the HC family of logic devices intended for CMOS applications. The SN74HC595B device is an 8-bit shift register that feeds an 8-bit D-type storage register.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register. The Q_H may be used for daisy chaining the device and will not go into high impedance when \overline{OE} is asserted.

7.2 Functional Block Diagram

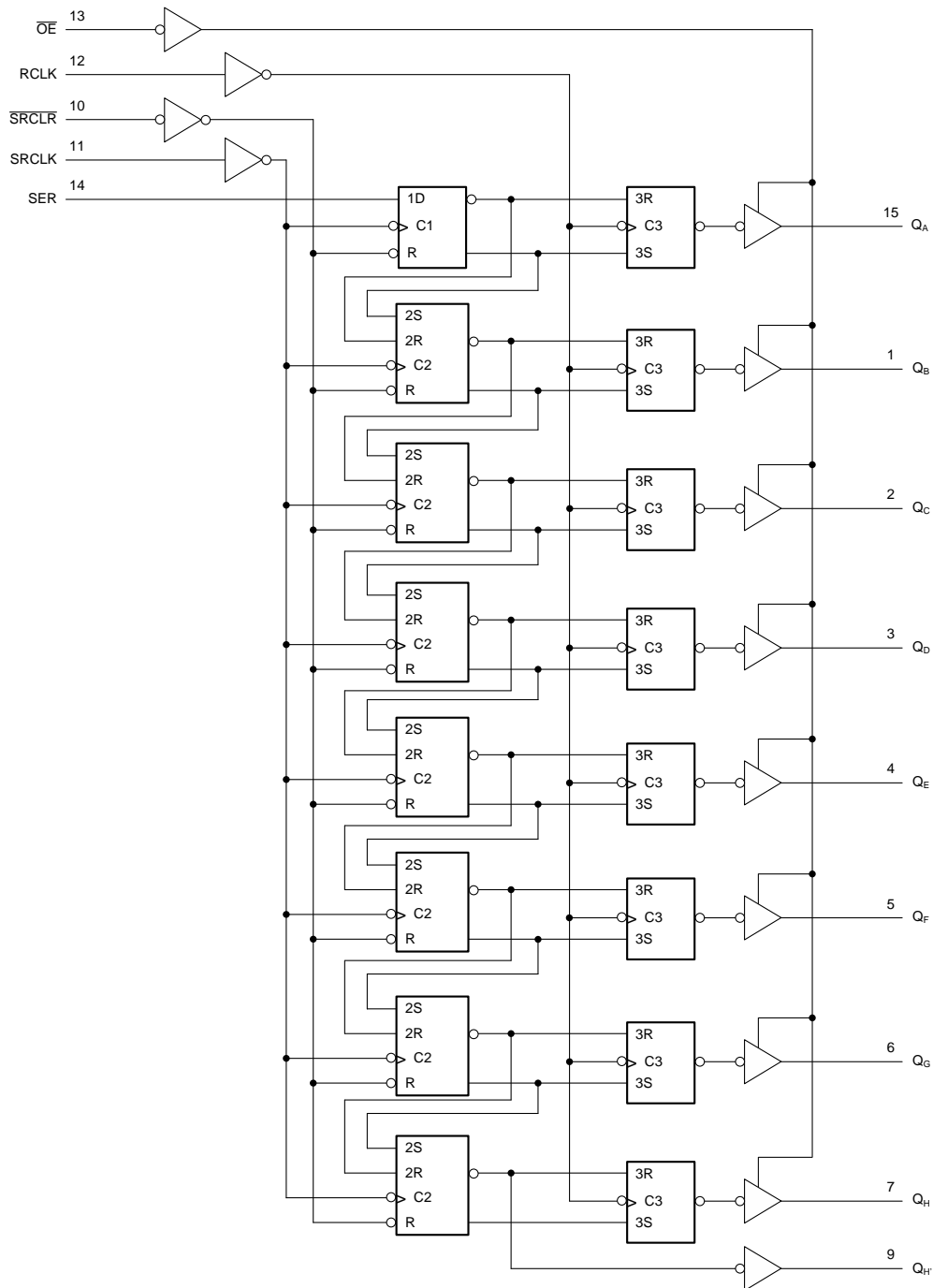


Figure 4. Logic Diagram (Positive Logic)

7.3 Feature Description

The SN74HC595B device is an 8-bit Serial-In, Parallel-Out shift register. It has a wide operating voltage of 2 V to 6 V, and the high-current 3-state outputs can drive up to 15 LSTTL Loads. The device has a low power consumption of 80- μ A (Maximum) I_{CC} . Additionally, this device has a low input current of 1 μ A (Maximum) and a ± 6 -mA output drive at 5 V. The device is available currently in the smallest logic QFN package at 0.5 mm max height with 0.4 mm pitch. The inputs are over voltage tolerant independent of V_{CC} .

7.4 Device Functional Modes

Table 3 lists the functional modes of the SN74HC595B devices.

Table 3. Function Table

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	\overline{OE}	
–	–	–	–	H	Outputs $Q_A - Q_H$ are disabled. Q_H is active .
–	–	–	–	L	Outputs $Q_A - Q_H$ are enabled.
–	–	L	–	–	Shift register is cleared.
L	↑	H	–	–	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	–	–	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
–	–	–	↑	–	Shift-register data is stored in the storage register.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN74HC595B is a low-drive CMOS device that is used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. Q_H pin of the first register should be connected to the serial (SER) pin of the second register for daisy chaining.

8.2 Typical Application

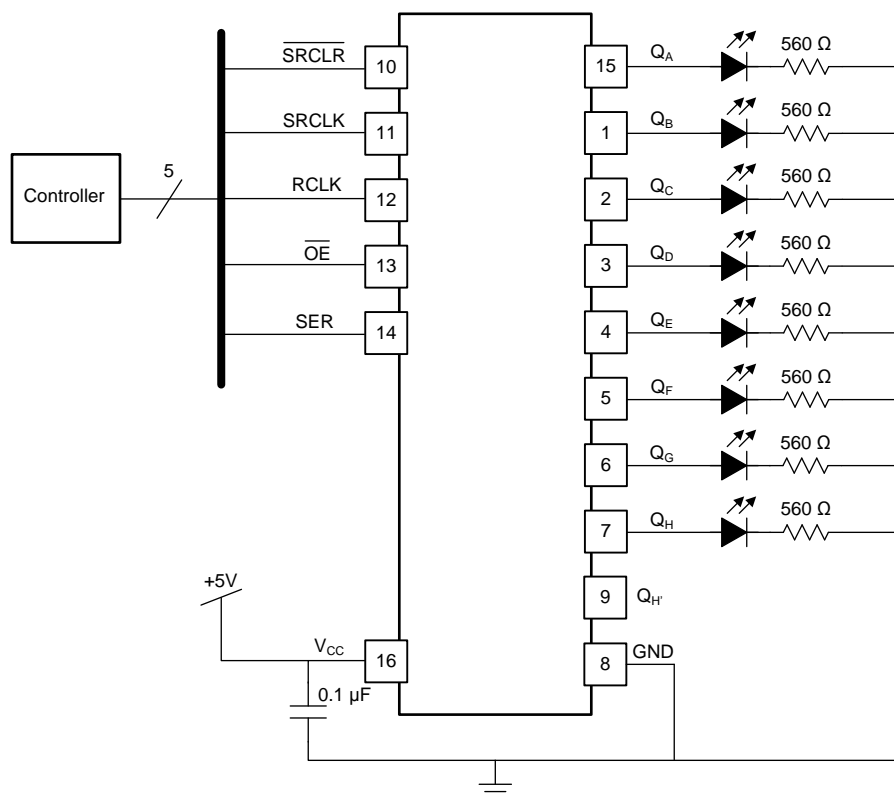


Figure 5. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has a balanced output drive. Take care to avoid bus contention because it can drive currents in excess of the maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended input conditions
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Inputs are over-voltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}

Typical Application (continued)

- Recommended output conditions
 - Load currents should not exceed 35 mA per output as per the [Absolute Maximum Ratings](#) table.
 - Outputs should not be pulled below Ground or above V_{CC}

8.2.3 Application Curves

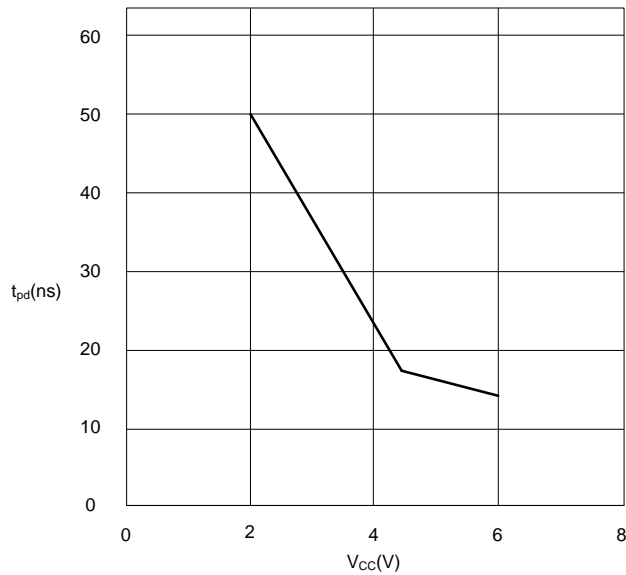


Figure 6. SN75HC595B t_{pd} vs. V_{CC}

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table. The total current through Ground or V_{CC} should not exceed 70 mA as per [Absolute Maximum Ratings](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µf is recommended; if there are multiple V_{CC} pins, then 0.01 µf or 0.022 µf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µf and a 1 µf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

10 Layout

10.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input and the gate are used, or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 7](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

10.2 Layout Example

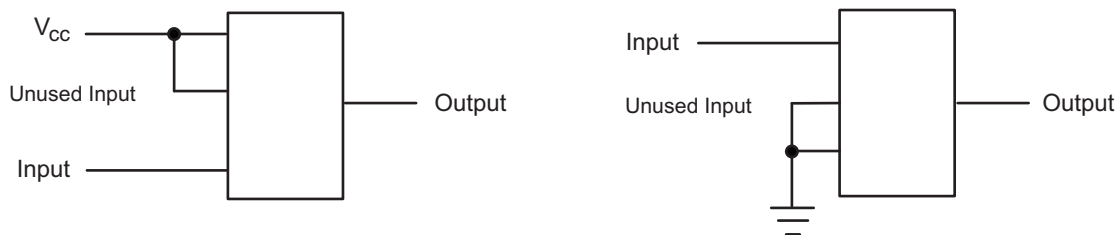


Figure 7. Layout Diagram

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, [SCBA004](#)

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC595BRWNR	ACTIVE	X1QFN	RWN	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	13YI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

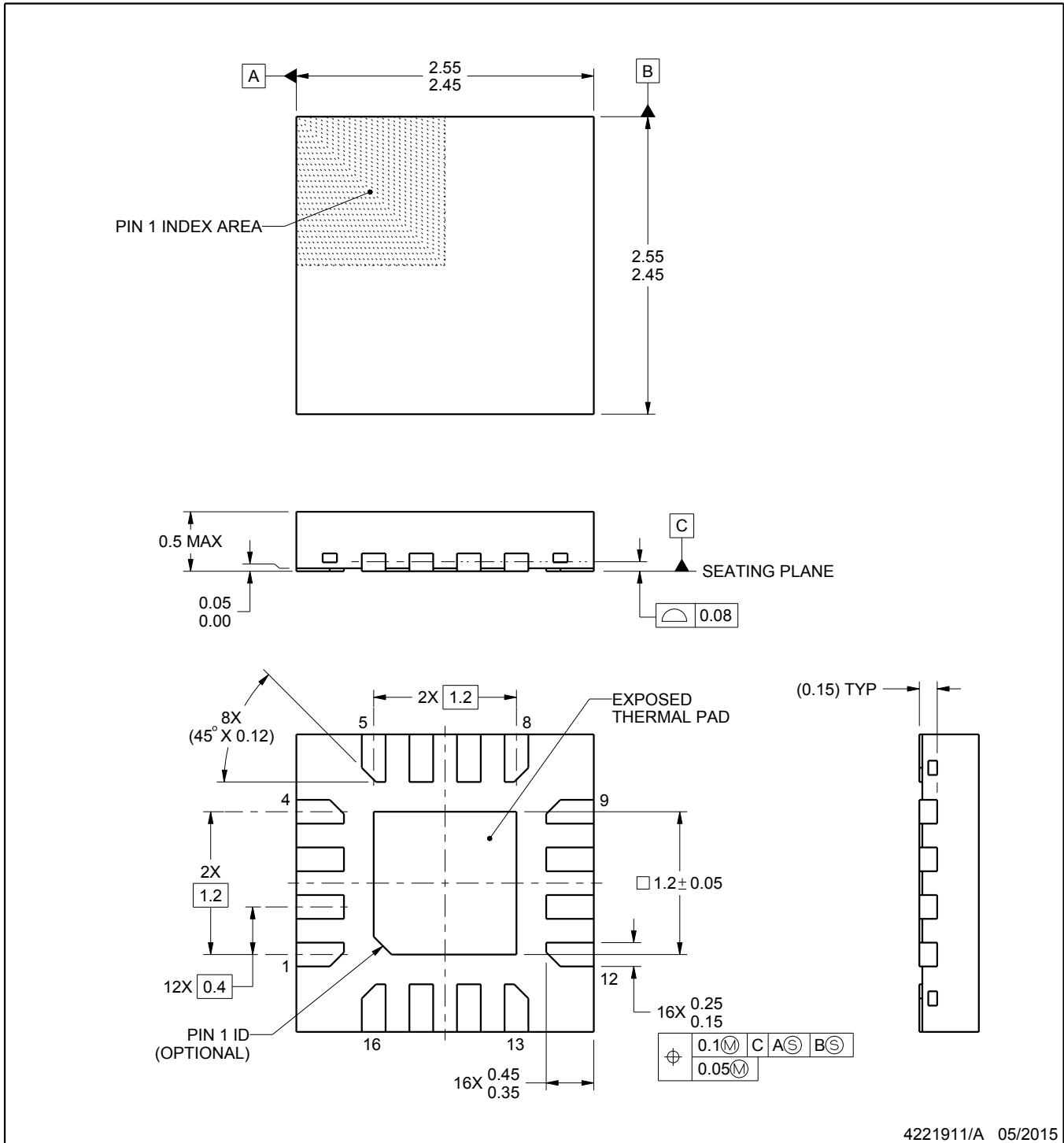
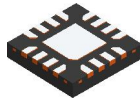
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC595BRWNR	X1QFN	RWN	16	2000	178.0	13.5	2.8	2.8	0.75	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC595BRWNR	X1QFN	RWN	16	2000	189.0	185.0	36.0



4221911/A 05/2015

NOTES:

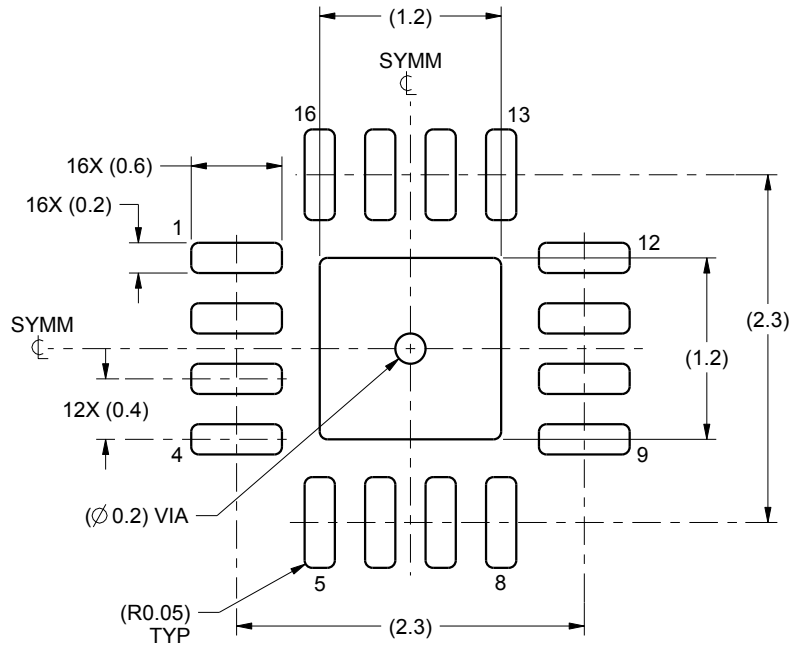
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

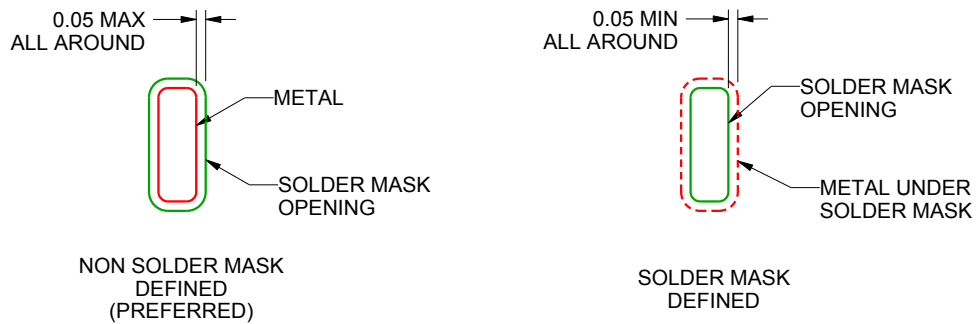
RWN0016A

X1QFN - 0.5 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4221911/A 05/2015

NOTES: (continued)

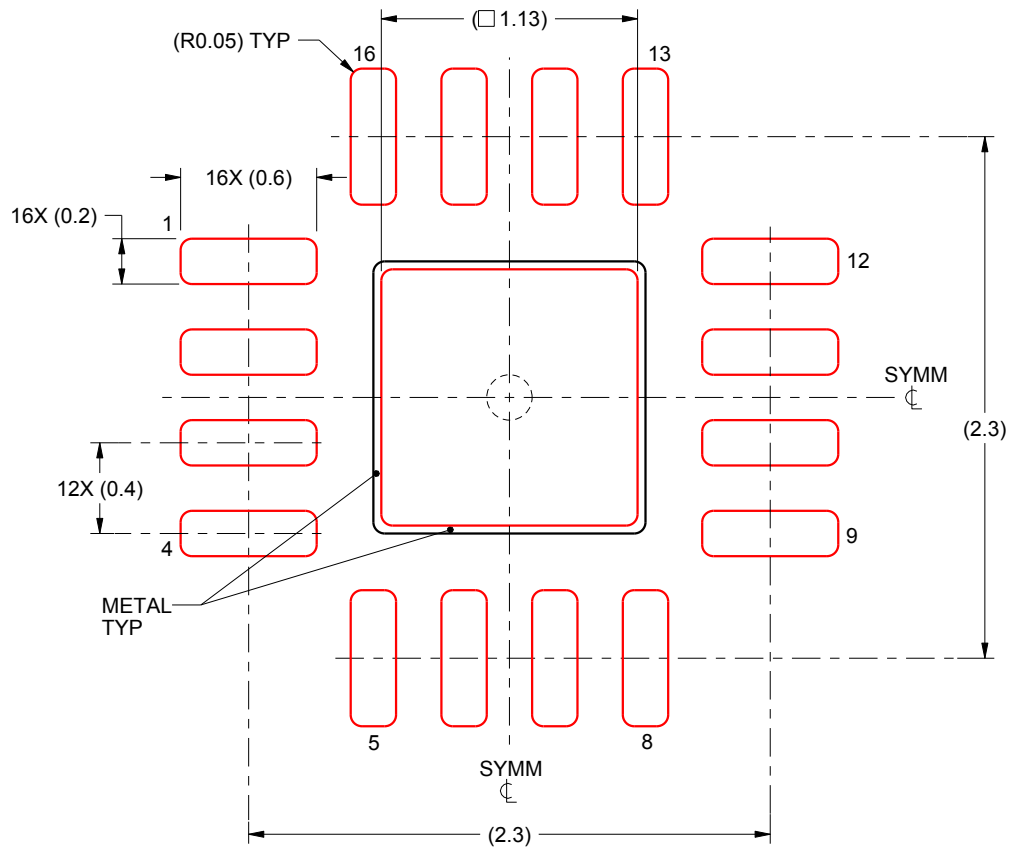
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

RWN0016A

X1QFN - 0.5 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

4221911/A 05/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated