Introduction

Teseo-LIV3 is a family of tiny GNSS modules sized 9.7 mm × 10.1 mm × 2.5 mm featuring STMicroelectronics® positioning receiver Teseo III. It is a standalone positioning receiver which embeds the new ST GNSS positioning engine capable of receiving signals from multiple satellite navigation systems.

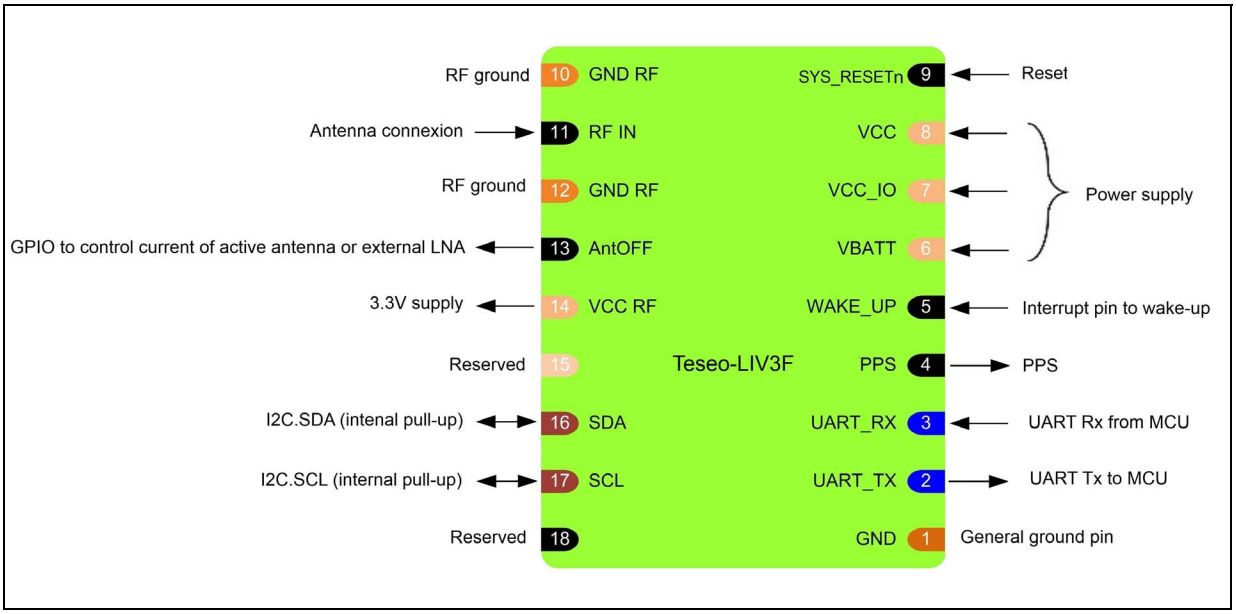
This document is relevant for the following Teseo-LIV3 modules.

Table 1. Teseo-LIV3 supported devices

Device type	Description
Teseo-LIV3F	Tiny GNSS module flash based
Teseo-LIV3R	Tiny GNSS module ROM based

In *Figure 1* pinout of the module is represented as follows:

Figure 1. Teseo-LIV3 pinout



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1 Power

Teseo-LIV3 is supplied by 3 power pins: VCC (pin8), VCC_IO (pin7) and VBAT (pin6).

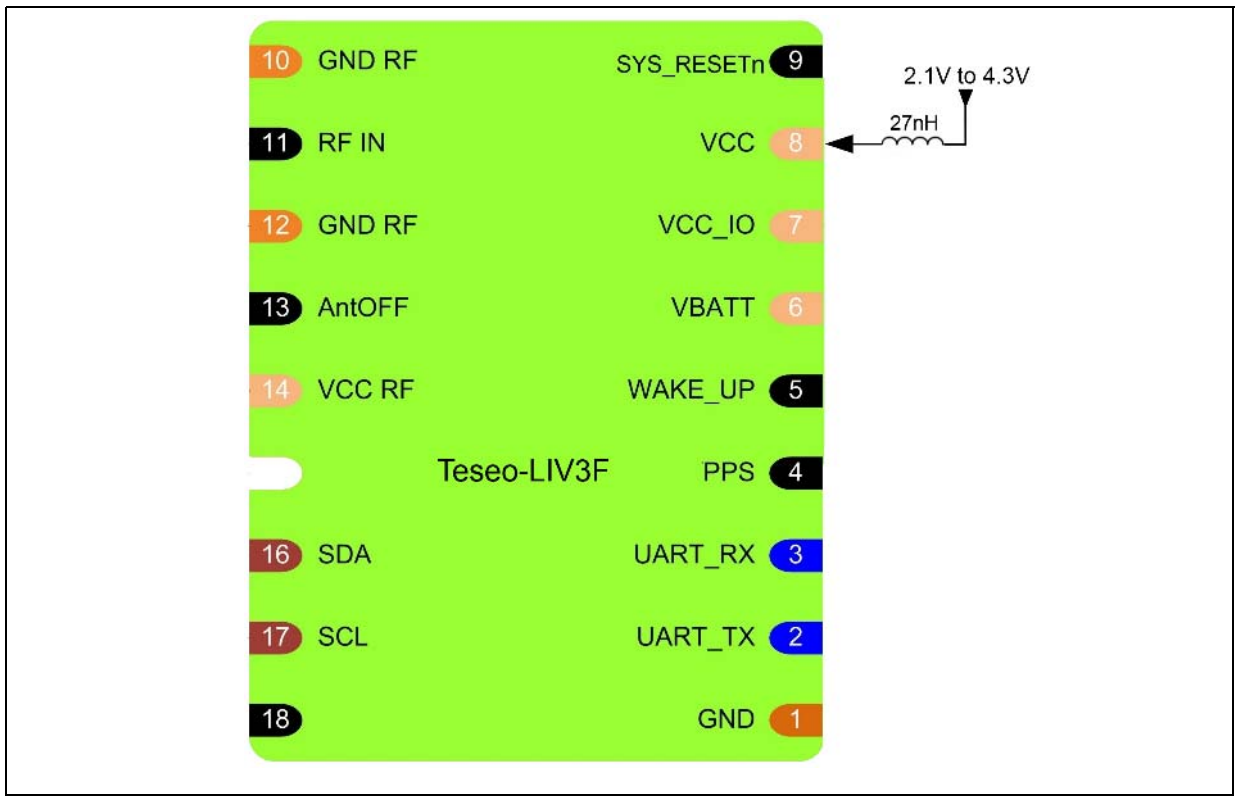
1.1 VCC (pin8)

VCC is the main supply. V_{CC} limiting values are: 2.1 V - 4.3 V.

At startup or during low power application current can change suddenly. It is important that supply IC is able to provide this current variation.

Take care that interference on VCC power line could degrade Teseo-LIV3 sensitivity performance, to avoid that it's recommended a 27 nH inductor (Murata LQG15HS27NJ02) as shown in *Figure 2: Inductor on VCC power line*.

Figure 2. Inductor on VCC power line



The suggested inductor on the VCC power line is able to recover interference coming from VCC power line.

1.2 VBAT (pin6)

VBAT is the supply for the low power domain backup: backup RAM and RTC.

VBAT can be either connected to VCC or it can be supplied by a dedicated supply always ON. When VBAT supply is kept ON during low power mode to allow fast recovery of GNSS

fix VBAT prevents current flow as soon as VBAT is lower than VCC. It is important when VBAT is supplied with small battery and especially if battery is not rechargeable.

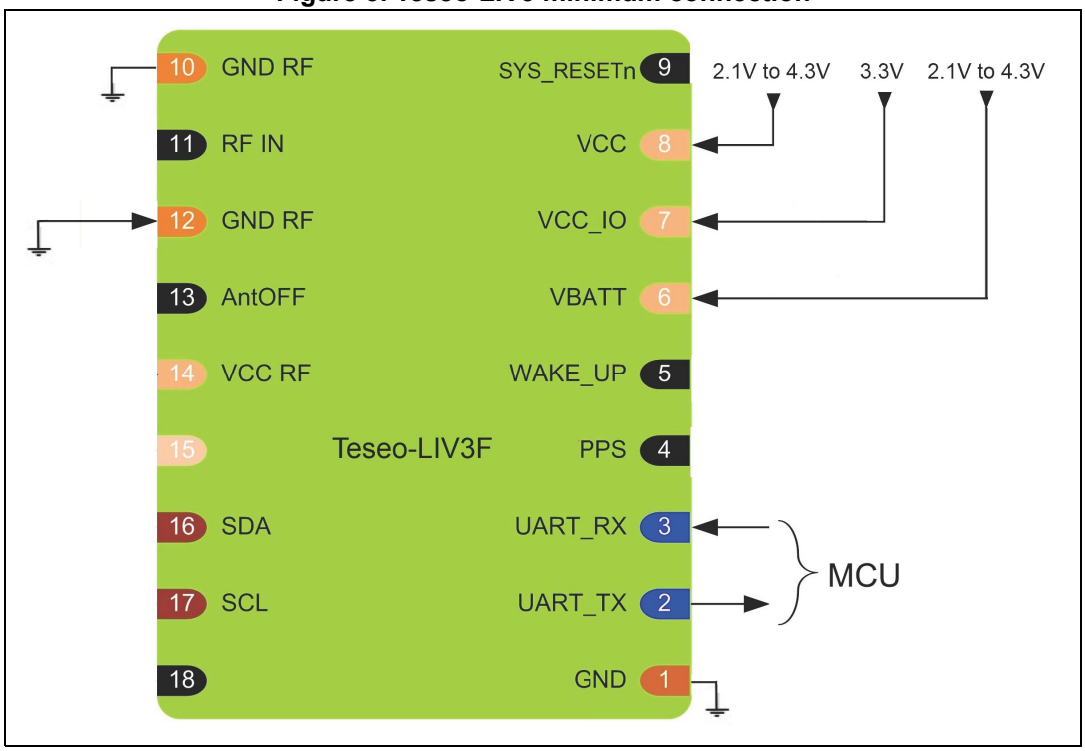
VBAT range can be from 2.1 V to 4.3 V.

1.3 VCC_IO (pin7)

VCC_IO is 3.3 V.

Figure 3 shows the minimum connection to make Teseo-LIV3 GNSS working.

Figure 3. Teseo-LIV3 minimum connection

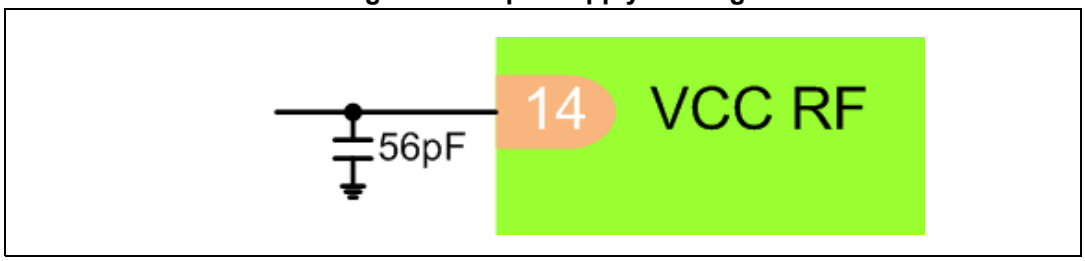


1.4 VCC_RF (pin14)

VCC_RF is an output image of VCC with a filtering for LNA or active antenna supply.

It can be filtered to remove high frequency noise as shown in *Figure 4*.

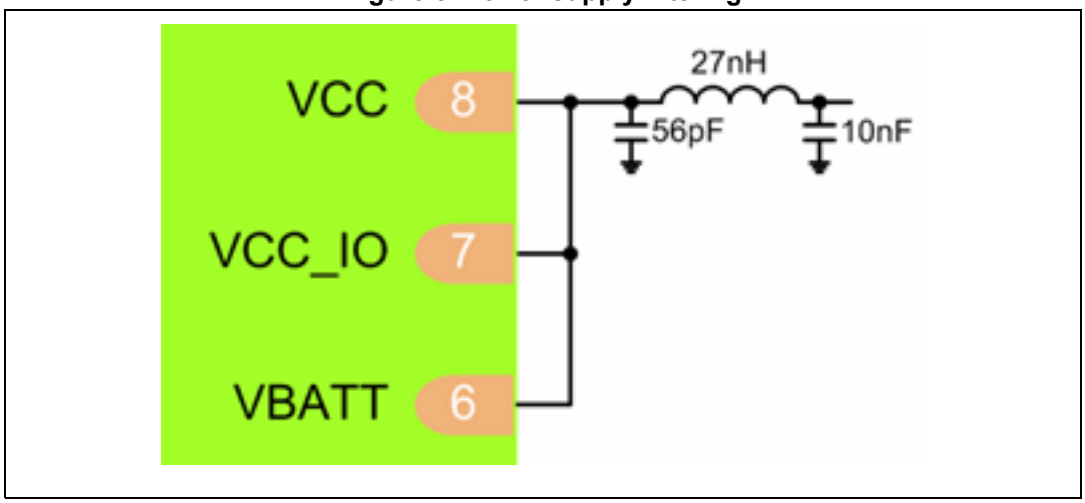
Figure 4. Output supply filtering



1.5 Power supply design reference

During prototyping stage, for the first PCBs, it is recommended to plan to have some filtering components on Teseo-LIV3 power supplies as shown In *Figure 5*.

Figure 5. Power supply filtering



Inductor size is 0401 (1.0×0.5mm) and capacitors are 0201 (0.6×0.3mm).

In case VCC_IO is separate from VCC, a serial 27nH inductor could also be planned for first PCBs.

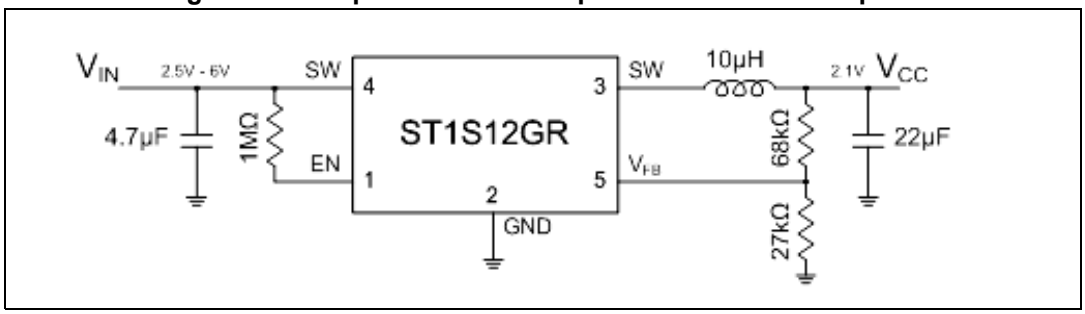
If all 3 pins have common supply, one single capacitor and one single inductor can be used. If not it is recommended to duplicate the filtering.

1.6 Current consumption optimization

Use of an SMPS at 2.1 V to supply VCC is recommended to optimize current consumption.

Here is an application example with ST1S12GR with an efficiency around 85%.

Figure 6. Example of SMPS to improve current consumption



If VCC_IO is also supplied by an SMPS, this will reach the lowest current consumption.

2 Reserved (pin15, 18)

In Teseo-LIV3 pin15 and 18 are reserved.

3 Interfaces

3.1 I2C (pin16, 17)

Teseo-LIV3 supports I2C slave mode only.

Internal 10 KΩ pull-up resistor on VCC_IO is present. It is important to avoid having other pull-up for current leakage in low power mode.

3.2 UART (pin2, 3)

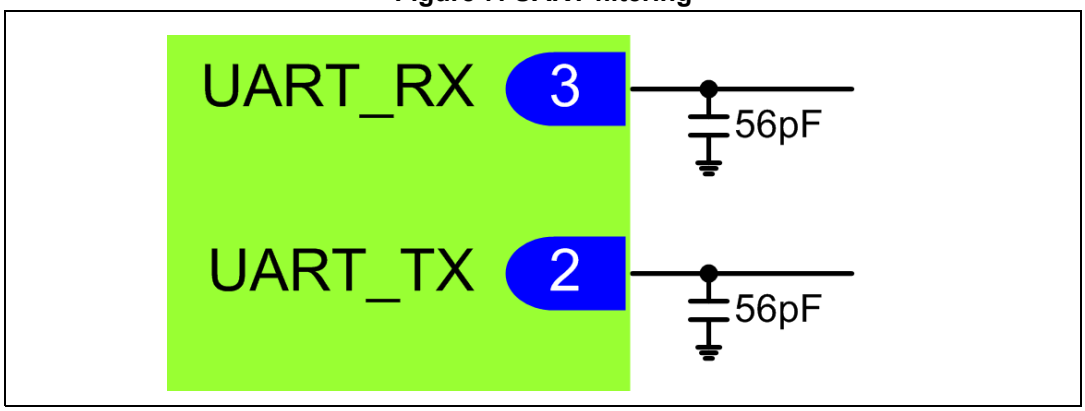
UART is a Universal Asynchronous Receiver/Transmitter that supports much of the functionality of the industry-standard 16C650 UART.

These UARTs vary from industry-standard 16C650 on some minor points which are:

- Receive FIFO trigger levels
- The deltas of the modem status signals are not available
- 1.5 stop bit is not supported
- Independent receive clock feature is not supported

During prototyping stage, for the first PCBs, it is recommended to plan to have some filtering components on Teseo-LIV3 UART lines as shown in *Figure 7*.

Figure 7. UART filtering



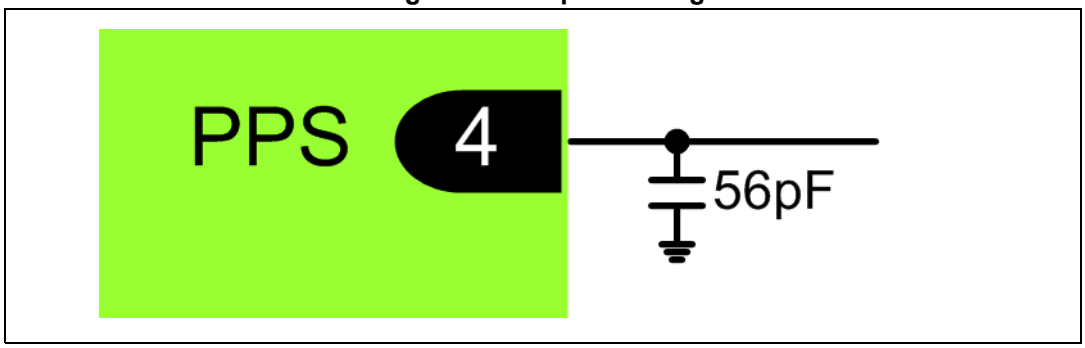
4 I/O pins

4.1 PPS (pin4)

PPS is the time pulse every one second. It can be configured with different condition of pulses.

During prototyping stage, for the first PCBs, it is recommended to plan to have some filtering components on Teseo-LIV3 PPS pin as shown in *Figure 8*.

Figure 8. PPS pin filtering



4.2 Wake_Up (pin5)

It is an external interrupt that is used to wake-up Teseo-LIV3 for asynchronous wake-up during standby software for instance.

It can be activated by a GPIO from host for instance. Wake_Up signal is active high.

4.3 SYS_RESETn (pin9)

It can force a Teseo-LIV3 under reset.

Reset signal is active low.

Host processor must have full control of this pin to guarantee the Teseo-LIV3F's firmware upgrade support. It is mandatory only on Teseo-LIV3F.

4.4 RF_IN (pin10)

It is the RF input.

4.5 AntOFF (pin13)

AntOFF is a GPIO used to switch OFF external LNA or switch OFF current for the active antenna.

A 10 kΩ pull down is necessary to ensure a low level during standby period.

5 Standby modes

Standby mode is the mode where only low power backup domain is running. It means VBAT must always be maintained. It allows to have very low current consumption and fast GNSS re-acquisition at the end of the standby time due to RTC.

Teseo-LIV3 offers 2 different ways of standby:

- Hardware standby
- Software standby

As IO buffers are not supplied during standby mode, it is important to keep all IO without external voltage to avoid any current leakage. UART_RX is an exception it can be left high.

5.1 Software standby

Software standby is activated by the binary for periodic standby. More details of how to set it are in the Software Manual. As HW standby, all supplies are kept ON.

Periodic fixes are from 5 s up to 24 hours between 2 fixes.

It ensures a current below 20 µA on Teseo-LIV3. Be careful that VCC_RF is ON during this standby, then in case of active antenna or external LNA, it is important to switch them OFF.

5.2 Hardware standby

This standby is ensured by switching OFF VCC (pin 8) and VCC_IO (pin 7) supplies and setting SYS_RESETn (pin 9) to 0 V. It can be activated asynchronously from GNSS binary with one GPIO switching OFF the supplies from a host.

During this standby only VBAT (pin 6) is kept ON.

It ensures a current below 15 µA. During this standby mode VCC_RF (pin 14) is OFF.

6 Front ends management

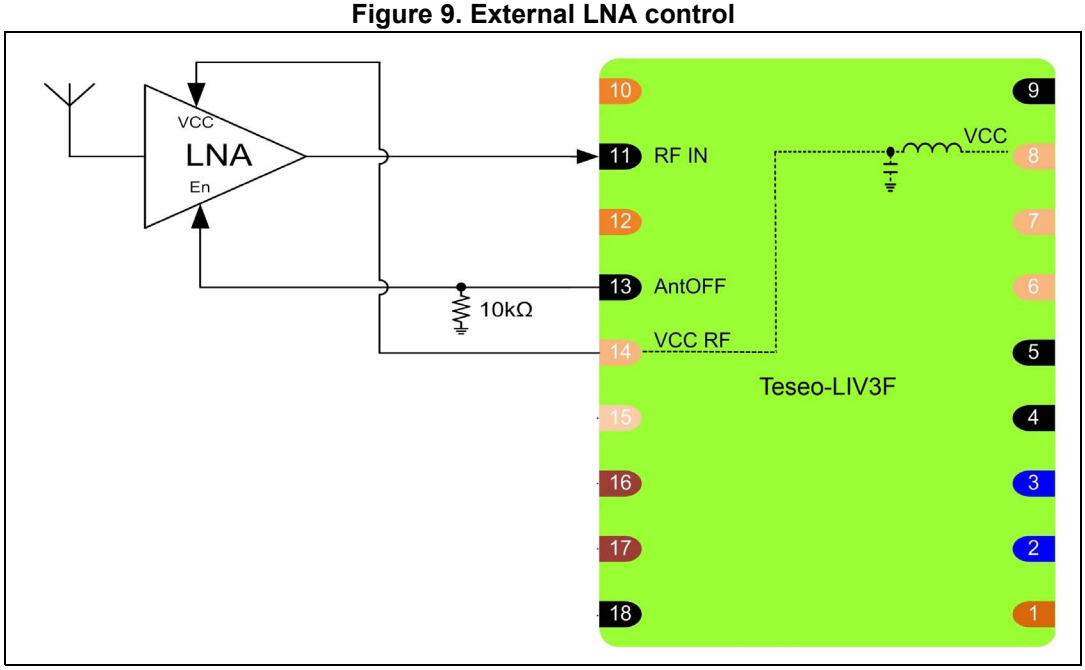
RF input impedance is 50 Ω.

6.1 External LNA

External LNA means a passive antenna used with an LNA on the same PCB as Teseo-LIV3 module. To optimize power consumption during low power mode if needed, the LNA should have an enable pin compatible with VCC_IO to be switched OFF/ON.

Here is a block diagram describing the connection.

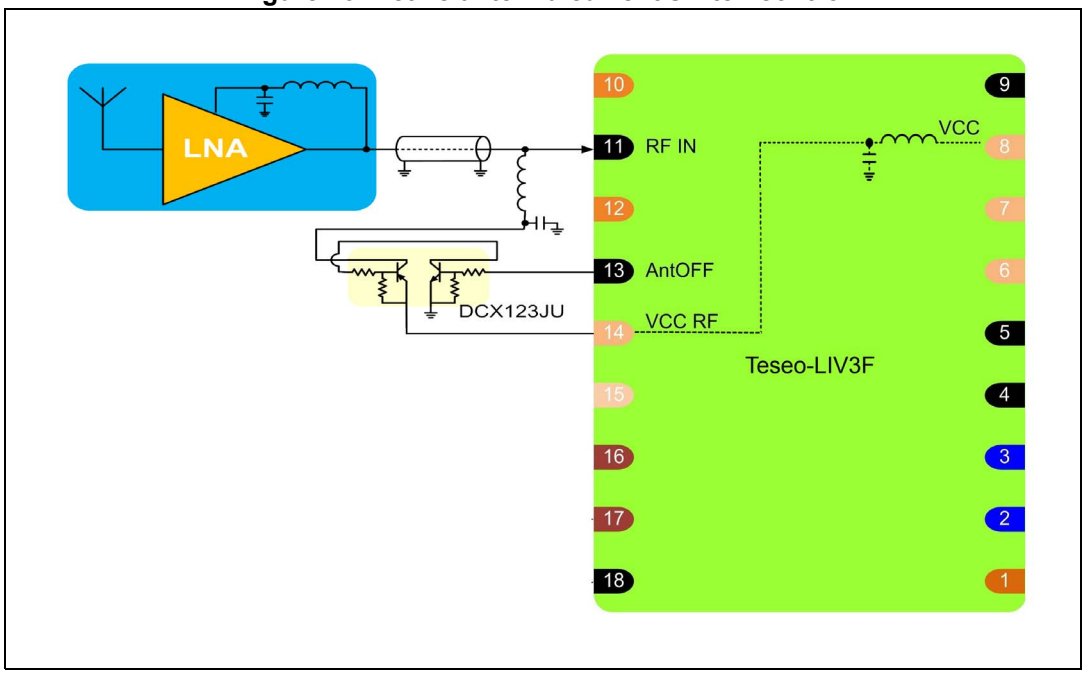
Figure 9. External LNA control



6.2 Active antenna

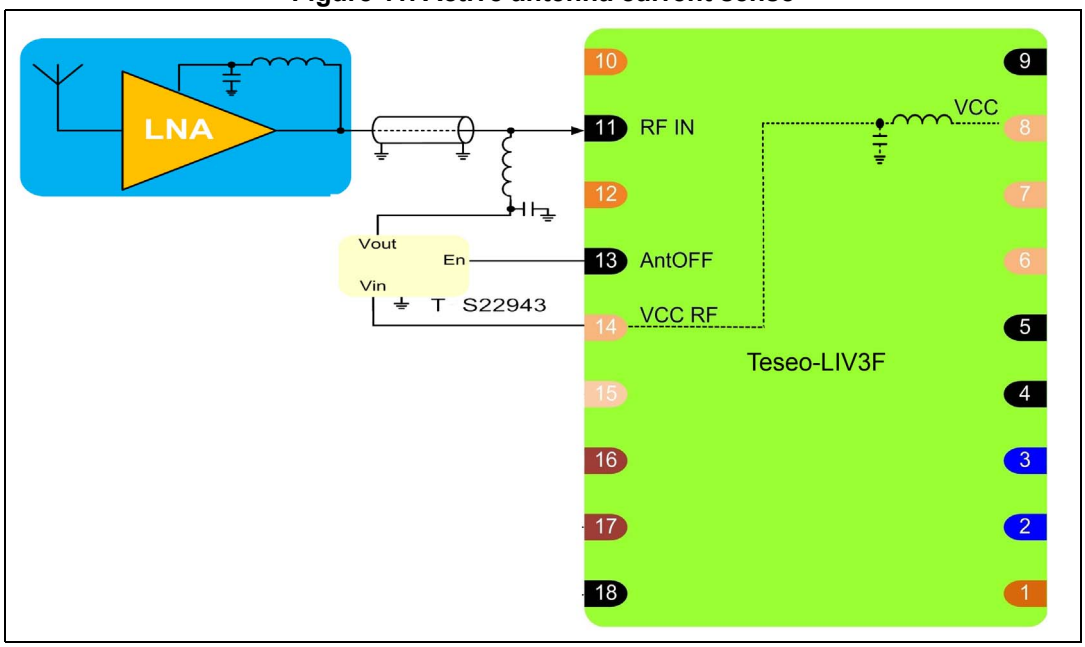
To optimize the current during low power operating mode, the active antenna can be used with a switch to cut the current flow.

Figure 10. Active antenna current switch control



To improve the functionality, a current limiter could be used in order to prevent any short circuit on the antenna see *Figure 11*.

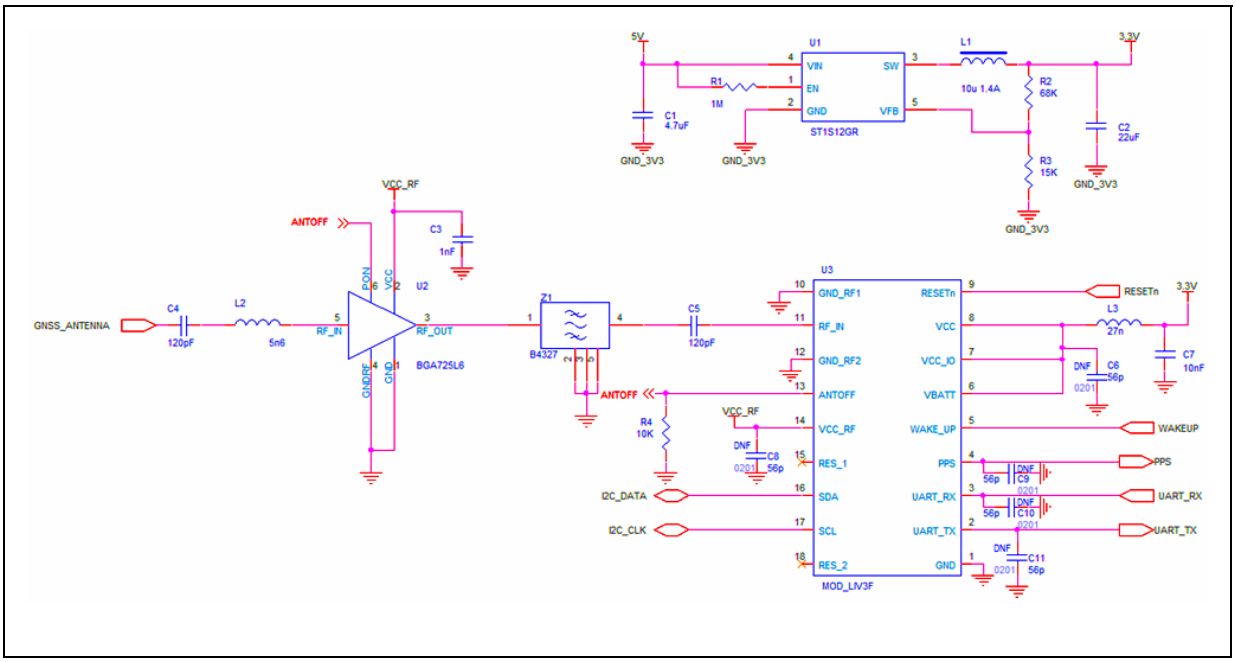
Figure 11. Active antenna current sense



7 Reference schematic and BOM

7.1 Schematic

Figure 12. General schematic



7.1.1 Bill of material

Table 2. Bill of material

Refs	Value	Description	Manufacturing 1		Manufacturing 2	
			Name	Part number	Name	Part number
C1	4 µ7	Surface mount 0603 capacitor ceramic 4.7 µF, 10% 10 V X7S 4 µ7; 10; X7S	Murata	GRM188C71A475KE11		
C2	22 µF	Capacitor, Ceramic, SMD, MLCC, Temperature Stable, Class II, 22 uF, +/-20%, 6.3 V, X5R, 0805	KEMET	C0805C226M9PACTU		
C3	1 nF	Automotive Grade Surface mount 0402 capacitor ceramic 1 nF, 10% 50 V X7R 1 nF; 50; X7R	Murata	GCM155R71H102KA37	TDK	CGA2B2X7R1H102K050BA
C7	10 nF	Multilayer Ceramic Capacitors MLCC - SMD/SMT SOFT 0402 50V 0.01uF X7R 10% T: 0.5 mm	TDK	CGA2B3X7R1H103K050BE	Murata	GCM155R71H103JA55D
C4,C5	120 pF	Automotive Grade Surface mount 0402 capacitor ceramic 120 pF, 5% 50 V C0G 120 pF; C0G	Murata	GCM1555C1H121JA16	TDK	CGA2B2C0G1H121J050BA
L1	10 µH	Surface mount magnetically shielded, wire wound inductor for power line applications. 10 µ; 1.4 A	TDK	LTF5022T-100M1R4-LC		
L2	5n6H	Surface mount wire wound inductor. 5n6H; 3%; 0.76 A	Coilcraft	0402CS-5N6XJLU	Murata	LQW15AN5N6G80D+00-21
L3	27 nH	Unshielded Multilayer Inductor, 27 nH, 350 mA, 460 mOhm Max, 0402 (1005 Metric)	Murata	LQG15HS27NJ02	TDK	MLG1005S27NJT000
C6,C8, C9,C10,C11	NM	56pF surface mount, general purpose multilayer ceramic chip capacitor, COG, 0201, 50V, +/-2%	Murata	GRM0335C1H560GA01	TDK	CGA1A2C0G1H560J030BA
R1	1 M	Surface mount chip resistor 1 M; 5%; 1/16 W	Yageo	RC0402JR-071ML		
R2	68 K	Surface mount chip resistor 68K; 1%; 1/16 W	Yageo	AC0402FR-0768KL		
R3	15 K	Surface mount chip resistor 15 K; 1%; 1/16 W	Yageo	RC0402FR-1315KL		
R4	10 k	Surface mount chip resistor 10 K; 5%; 1/16 W	Yageo	RC0402JR-0710KP		
U1	ST1S12GR	Synchronous rectification adjustable step-down switching regulator ST1S12GR; 0.7; 1.7	ST	ST1S12GR TSOT23-5L		

Table 2. Bill of material (continued)

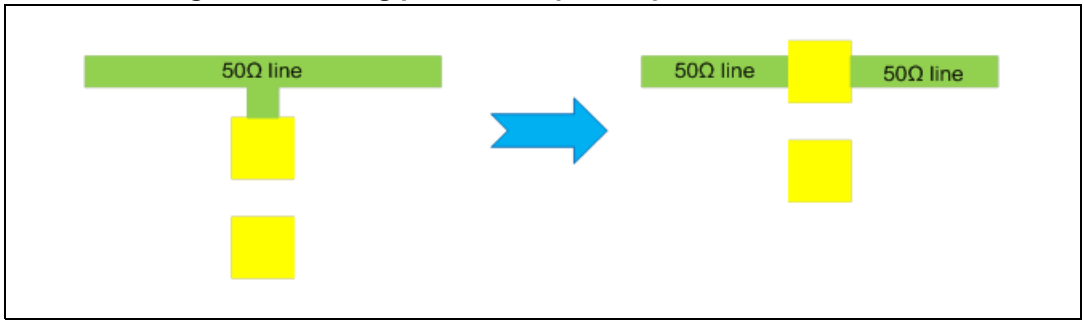
Refs	Value	Description	Manufacturing 1		Manufacturing 2	
			Name	Part number	Name	Part number
U2	BGA725L6	Low Noise Amplifier for GPS, GLONASS, Galileo and Compass BGA725L6	Infineon	BGA725L6		
Z1	B4327	Automotive SAW RF filter for GPS+COMPASS+GLONASS	Epcos	B39162B4327P810		
U3	LIV3	TESEOIII module SMPS version	ST	LIV3		

8 Layout recommendation

To guarantee good RF performance, 0402 components are preferable because they avoid having too big component pads compared with RF 50 ohms line.

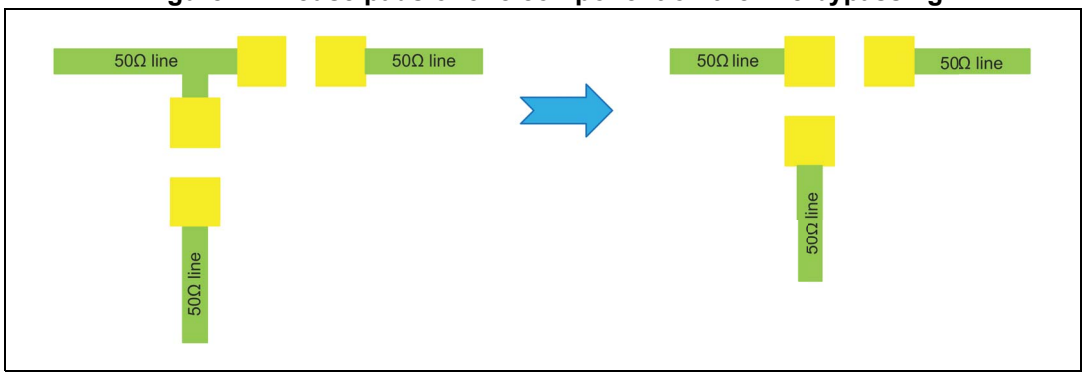
Place parallel components pads on 50 ohms line as in *Figure 13*.

Figure 13. Placing parallel component pads on 50 ohms line



For 50 ohms line bypassing it's suggested to superimpose the pad of one component on the pad of the other one as in *Figure 14*.

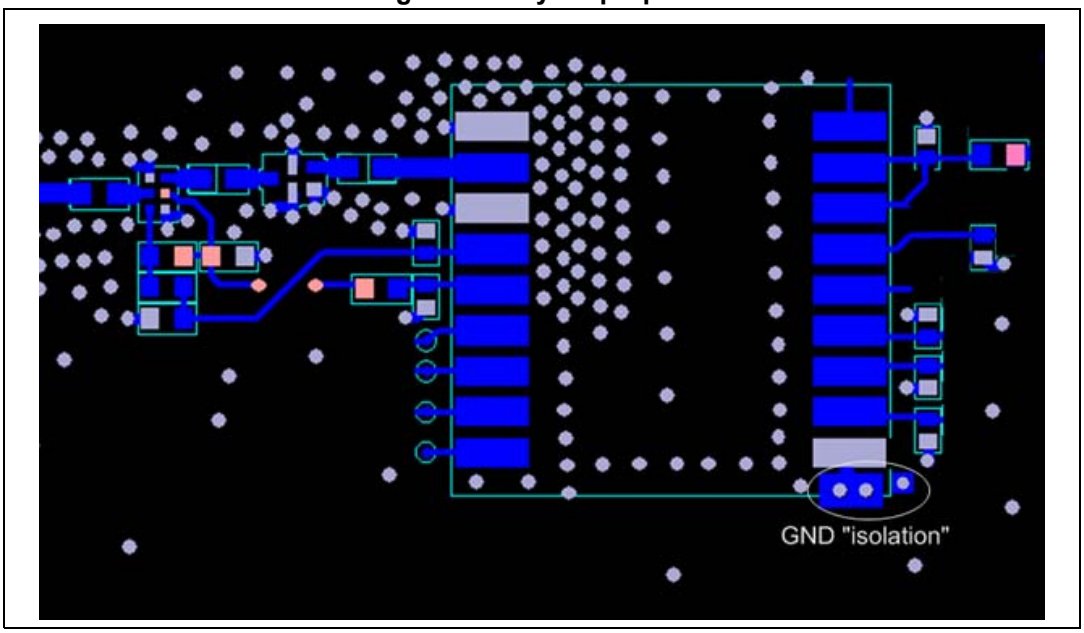
Figure 14. Reuse pads of one component on the line bypassing



Place ground vias below Teseo-LIV3 all around and in the middle and also around the 3 ground pins.

The following layout presents layout recommendation to ensure the best performances of Teseo-LIV3. ST heartily recommends having a maximum of ground vias below the module as illustrated in the *Figure 15*.

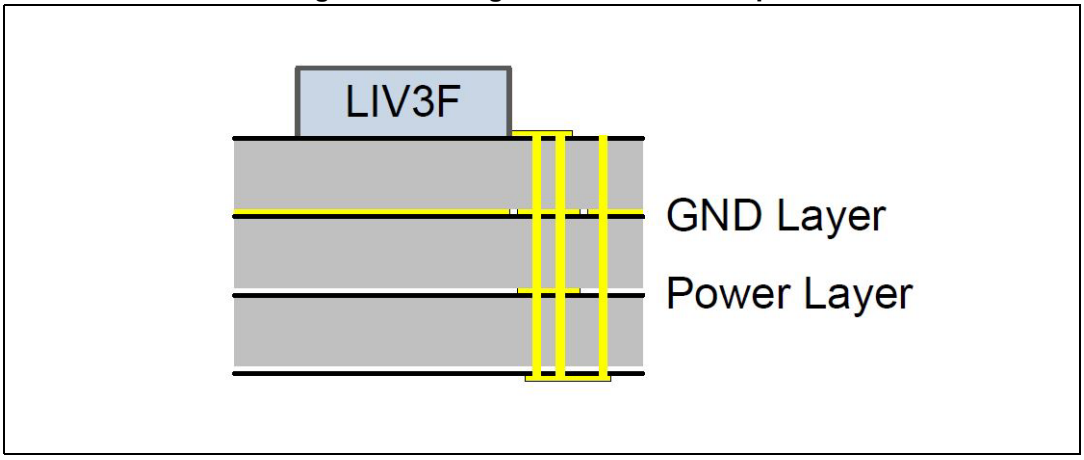
Figure 15. Layout proposal



As GNSS signals are very low, it is important to take care of the layout. There are 2 main recommendations to follow for Teseo-LIV3 layout.

1. Many ground vias have to be placed around the RF ground (Pin10 and 12) to increase ground size.
2. In addition, it is important to have an isolation of the power ground (Pin1).
   Don't connect it directly to ground. One or two vias from Top (assuming Teseo-LIV3 is on Top) to Bottom (without any ground connection) and then a second via from Bottom to GND plane can be used without any connection on top, as shown in *Figure 16*.

Figure 16. Pin1 gnd "isolation" example



It is important to have 50 ohms RF traces width as close as possible to components pads size to avoid too much impedance jumps.

When possible, avoid any trace below Teseo-LIV3 module.

9 Antenna recommendations

9.1 Patch antennas

Patch antennas have different sizes from 25×25mm, 18×18mm and 12×12mm.

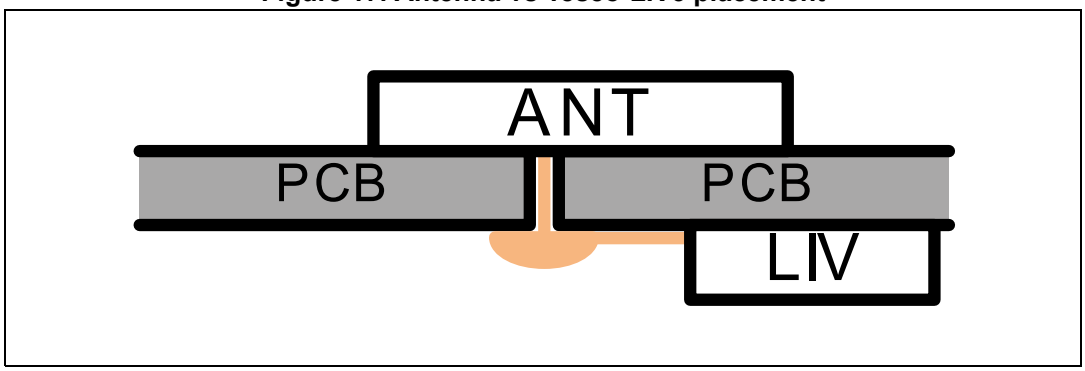
They have the advantage to be cheap, with good efficiency and highly directive. They can be used when mounted on horizontal support.

For performances, the bigger are the antennas and the better are the performances.

9.1.1 Antenna on the opposite side

This implementation allows to obtain the best GNSS performances. Patch antennas are with pin soldered on the PCB on the opposite side, where it is mounted the Teseo-LIV3 and other RF components as shown in figure *Figure 17*.

Figure 17. Antenna vs Teseo-LIV3 placement



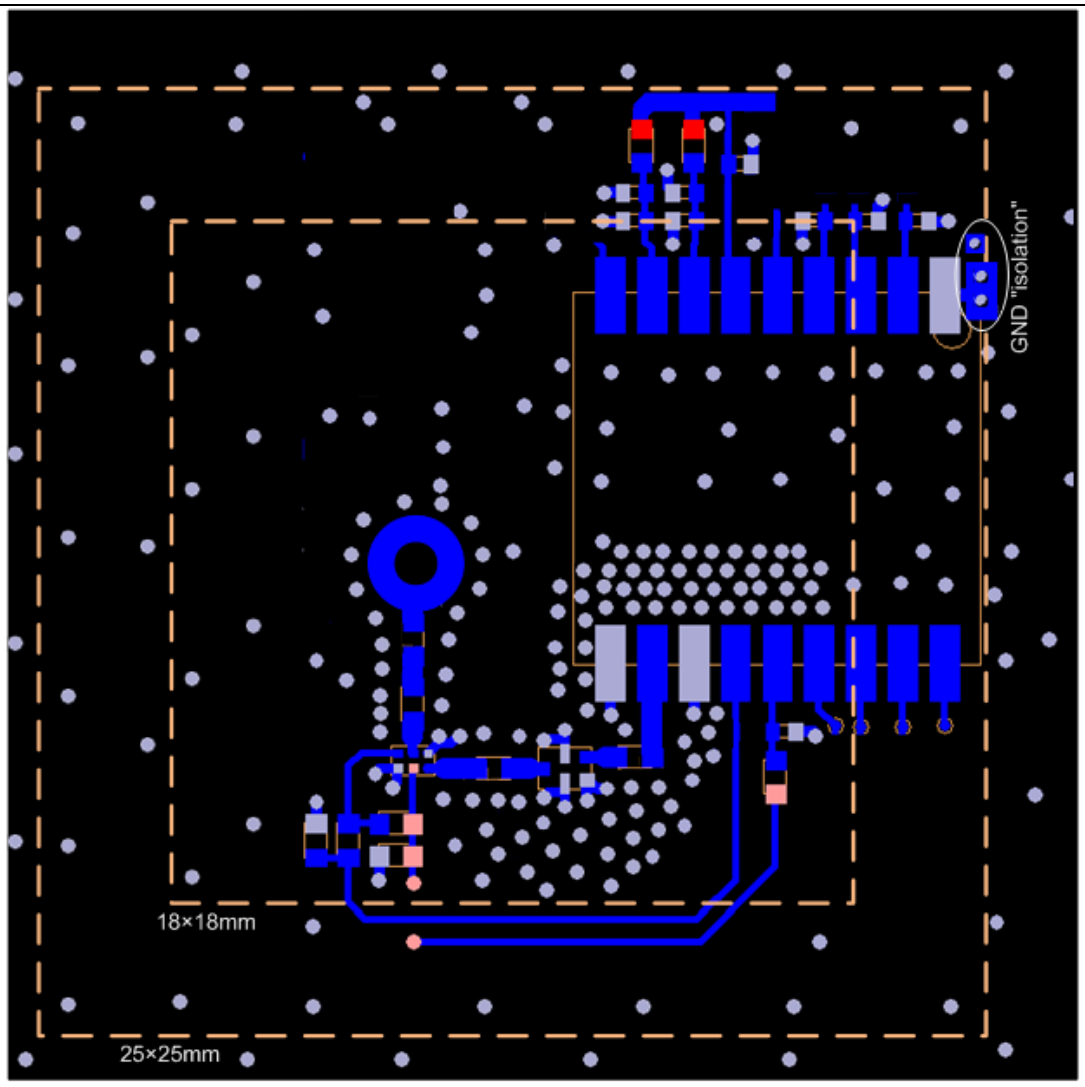
The *Table 3* gives antenna part number compatible.

Table 3. List of suggested antennas

Manufacter	Part number	Constellation	Size
Taoglas	CGGBP.25.4.A.02	GPS+Glonass+Beidou	25×25mm
Taoglas	CGGBP.25.2.A.02	GPS+Glonass+Beidou	25×25mm
Taoglas	CGGP.18.4.C.02	GPS+Glonass	18×18mm
Yageo	ANT2525B00DT1516S	GPS+Glonass	18×18mm
Yageo	ANT1818B00CT1575S	GPS+Glonass	25×25mm

Figure 18 is an example of layout with Antenna on opposite side of the components.

Figure 18. Antenna on bottom layer and Teseo-LIV3 on top layout example



On the antenna side, there's only a ground pad as large as the antenna with one big via for antenna pin. If the ground plane can be larger than the antenna side it will improve the antenna performance.

Antenna is usually glued and soldered with the pin.

It is necessary to follow the layout recommendations in *Chapter 8*.

9.1.2 Antenna on the same side than Teseo-LIV3

In case of antenna on the same side of the Teseo-LIV3, the best performance can be obtained if the antenna is placed more than 2cm far from Teseo-LIV3.

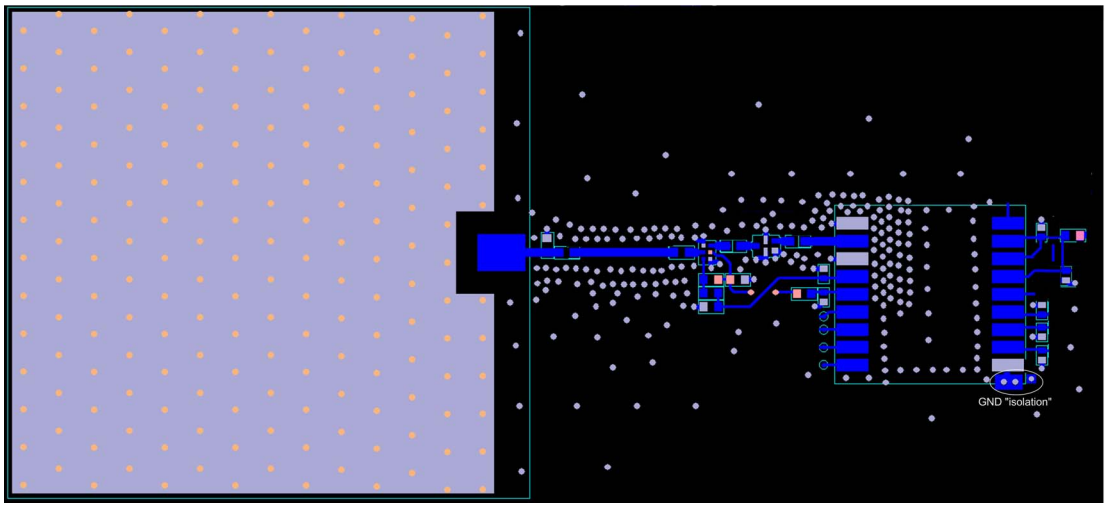
The *Table 4* gives some antenna part numbers compatible with GPS+Glonass.

Table 4. List of SMD antennas

Manufacter	Part number	Constellation	Size
Taoglas	SGGP.25.4.A.02	GPS+Glonass+Galileo	25×25mm
Taoglas	SGGP.18.4.A.02	GPS+Glonass+Galileo	18×18mm
Yageo	ANT1818B00BT1516S	GPS+Glonass	18×18mm
Yageo	ANT2525B00BT1516S	GPS+Glonass	25×25mm

It is important to follow the example of layout with Teseo-LIV3 placed at 2 cm of the antenna, as shown in *Figure 19*.

Figure 19. 25×25mm SMD Antenna and Teseo-LIV3 on same layer example



It is necessary to follow the layout Teseo-LIV3 recommendations in *Chapter 8*.

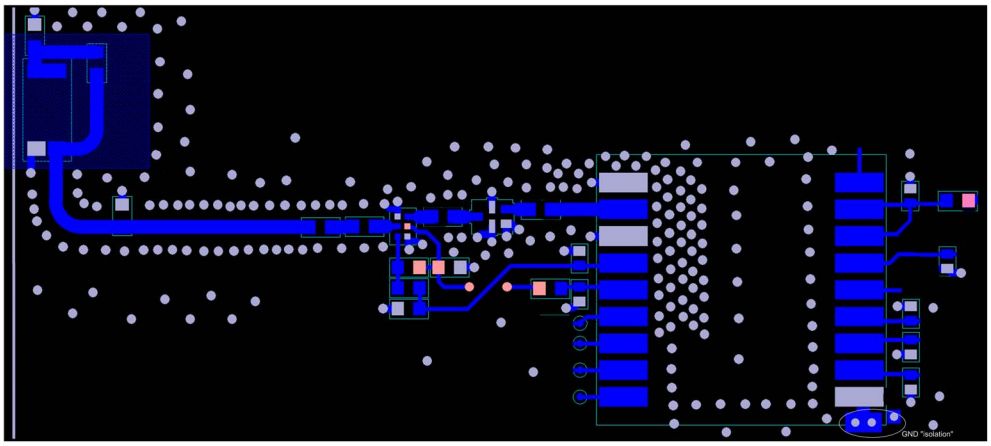
9.2 Chip antenna

Chip antenna has the advantage to be small. They are less directive than patch antenna with spherical radiation. Most of the time PCB has to be empty of copper below the antenna position with a certain aperture.

For Teseo-LIV3 usage, the recommendations to follow are in *Chapter 9.1.2: Antenna on the same side than Teseo-LIV3*. The best performance can be obtained if the antenna is placed more than 2cm far from Teseo-LIV3.

The *Figure 20* shows the example of chip antenna (Taoglas GGBLA.01.A - GPS+Glonass+Beidou) mounted on the edge of the PCB:

Figure 20. Chip Antenna and Teseo-LIV3 on same layer example



It is necessary to follow the layout Teseo-LIV3 recommendations in *Chapter 8*.

9.3 Remote antenna

Remote antenna means antenna connected to PCB where Teseo-LIV3 is soldered with an RF connector. The best performance can be obtained if the remote antenna is placed more than 2cm far from Teseo-LIV3.

In case of active antenna, there's no need to mount LNA on the PCB.

In case of passive antenna, it is much better to mount external LNA and SAW filter in front of the Teseo-LIV3.

10 Revision history

Table 5. Document revision history

Date	Revision	Changes
08-Sep-2017	1	Initial release.
09-May-2018	2	Added *Chapter 8: Layout recommendation*.
02-Jul-2018	3	Updated *Chapter 8: Layout recommendation*. Updated *Figure 13: Placing parallel component pads on 50 ohms line*, *Figure 14: Reuse pads of one component on the line bypassing* and *Figure 15: Layout proposal*. Minor text changes.
05-Oct-2018	4	Updated *Section 1.4: VCC_RF (pin14)* and *Section 1.5: Power supply design reference*. Updated *Figure 3*, *Figure 4* and *Figure 5*. Updated *Section 3.2: UART (pin2, 3)* and added *Section 4.1: PPS (pin4)*. Updated value in *Section 6.1: External LNA* and updated *Section 6.2: Active antenna*. Updated *Section 7: Reference schematic and BOM*. Added *Section 9: Antenna recommendations*. Minor text changes.
29-Nov-2018	5	Updated *Figure 1*, *Figure 5*, *Figure 12*, *Figure 15*, *Figure 18*, *Figure 19* and *Figure 20*. Added *Figure 16*. Updated *Table 2* and *Table 4*.
20-Feb-2019	6	Updated *Introduction*. Replaced “Teseo-LIV3F” with “Teseo-LIV3”. Added *Table 1: Teseo-LIV3 supported devices*.