CMX90A702 ● 28 GHz 5G Medium Power Amplifier (MPA)

Description

The CMX90A702 is a highly linear medium power amplifier operating in Frequency Range 2 (FR2) from 26.5 to 29.5 GHz, addressing the needs of 5G New Radio (NR) band n257 and n261.

CMX90A702 is a three-stage GaAs MMIC amplifier delivering +25 dBm (0.3 W) of output power at 1 dB gain compression, 21 dB of small signal gain and +32.5 dBm output third order intercept (OIP3). RF ports are matched to 50 Ω with an integrated DC blocking capacitor at the output.

The MPA is easy to monitor and control with an on-chip temperature-compensated RF power detector and fast-switching enable circuit.

Using an enhancement mode (E-mode) pHEMT process ensures only positive supply voltages are required, thus making single DC supply operation possible.

4x4mm VQFN-20 Package

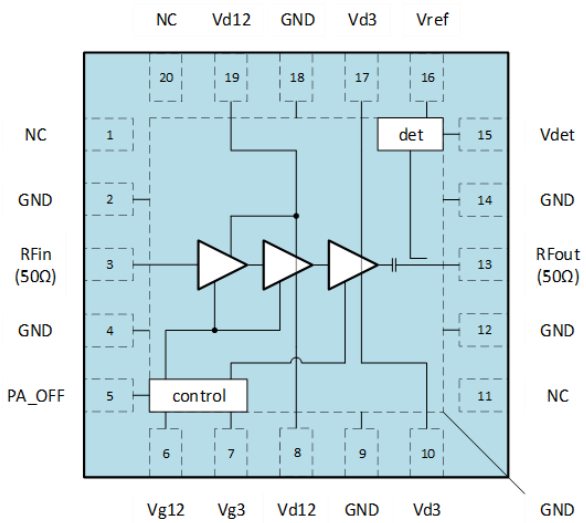
Product Features

- Frequency range 26.5 – 29.5 GHz
- Small signal gain 21 dB
- Output P1dB +25 dBm (0.3 W)
- Power added efficiency 28 %
- EVM 4 % @ 18 dBm mean power
- Quiescent Supply +4 V @ 182 mA
- Vd applied either side of package

Applications

- 5G mmWave infrastructure
- Fixed wireless access (FWA)
- Repeaters & small cells
- 5G backhaul
- Customer premises equipment (CPE)
- Passive phased array antenna

Block Diagram



Ordering Information

Part Number	Description
CMX90A702QH-R701	7” Reel with 100 pieces
CMX90A702QH-R705	7” Reel with 500 pieces
EV90A702	Evaluation board

Absolute Maximum Ratings

Parameter	Rating
RF Input Power	+10dBm
Device Voltage (Vd, Ven)	+4.5V
Case Temperature (Tc)	-40 to +85 °C
Junction Temperature (Tjmax)	150 °C (MTTF > 10^7 hours)
Storage Temperature	-40 to +125 °C
ESD Sensitivity	HBM 250V (Class 1A), CDM 500V (Class C2a)
MSL Level	Level 3

Exceeding the maximum ratings may result in damage or reduced device reliability.

Thermal Characteristics

Parameter	Rating
Thermal Resistance (Rjc)	31 °C/W (Tc = 85˚C)

Thermal resistance is junction-to-case, where case refers to the exposed die pad on the backside which is in contact with the board.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Frequency Range	26.5		29.5	GHz
Case Temperature (Tc)	-40		+85	°C
Device Voltage (Vd)	3	4	4.2	V
Gate Voltage (Vg12): Idq12 = 73 mA	0	0.415	0.55	V
Gate Voltage (Vg3): Idq3 = 109 mA	0	0.415	0.55	V
Power down Voltage (PA_OFF)	0	2.5	3.3	V

The device will be tested under certain conditions, but performance is not guaranteed over the full range of recommended operating conditions.

ESD Caution

CMX90A702 incorporates ESD protection circuitry however ESD precautions are strongly recommended for handling and assembly. Ensure that devices are protected from ESD in antistatic bags or carriers when being transported. Personal grounding is to be worn at all times when handling these devices.

RoHS Compliance

All devices supplied by CML Microcircuits are compliant with RoHS directive (2011/65/EU), containing less than the permitted levels of hazardous substances

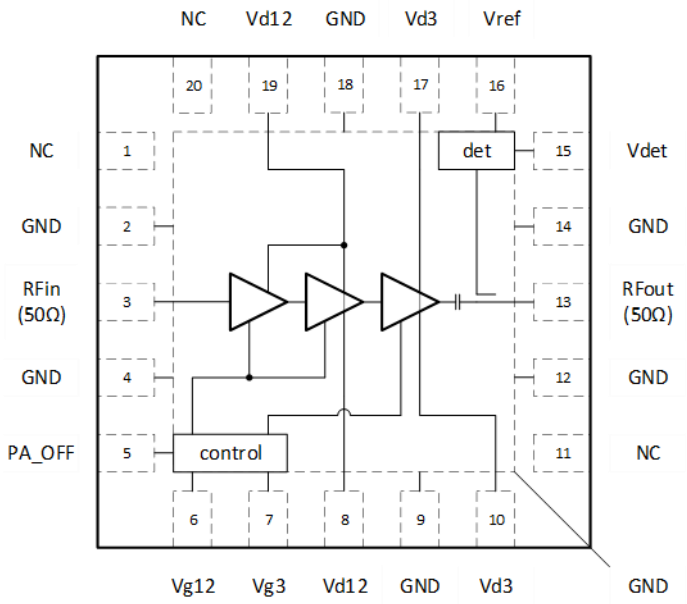
Electrical Specification

Results taken on the EV90A702 EVB, board losses have been de-embedded using a TRL calibration board.

Zo = 50 Ω, Vd = +4 V, Idq12 = 73 mA, Idq3 = 109 mA, Ta = +25 °C (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Frequency		26.5		29.5	GHz
Small Signal Gain	26.5 GHz 28.0 GHz 29.5 GHz		20.9 22.5 20.5		dB
Reverse Isolation	26.5 GHz to 29.5 GHz		50		dB
P1dB	26.5 GHz 28.0 GHz 29.5 GHz		26.7 25.6 24.3		dBm
P3dB	28.0 GHz		26.3		dBm
PAE at P1dB	28 GHz		28		%
OIP3	Two-tone test Δf = 100 MHz, Pout/Tone = 15dBm		32.5		dBm
Input Return Loss	26.5 GHz to 29.5 GHz		10		dB
Output Return Loss	26.5 GHz to 29.5 GHz		7		dB
Device Current (Idq12)	PA_OFF = 0 V, No RF Input		73		mA
Device Current (Idq3)	PA_OFF = 0 V, No RF Input		109		mA
Standby Current	PA_OFF = +2.5 V, No RF Input		1.2		mA
Drain Current (Id)	PA_OFF = 0V, at P1dB		360		mA
PA_OFF (Logic 0 = Enabled)	Amplifier normal operation	0		0.5	V
PA_OFF (Logic 1 = Standby)	Amplifier in standby mode	2	2.5	3.3	V
Power detector Vref			2		V
Power detector Vdet	No RF Input		2		V
Power detector Output Voltage (Vref - Vdet)	No RF Input		10		mV
Power detector Output Voltage (Vref - Vdet)	At P1dB		0.9		V

Pin Assignments



Top View

Pin	Name	Description
1	NC	Connect to GND
2	GND	Connect to GND
3	RFin	RF input. Internally matched to 50 Ω. (DC path to ground)
4	GND	Connect to GND
5	PA_OFF	Amplifier enable/disabled input
6	Vg12	Stage 1 and 2 gate voltage
7	Vg3	Stage 3 gate voltage
8	Vd12	Stage 1 and 2 drain voltage (or use pin 19)
9	GND	Connect to GND
10	Vd3	Stage 3 drain voltage (or use pin 17)
11	NC	Connect to GND
12	GND	Connect to GND
13	RFout	RF output. Internally matched to 50 Ω with integrated DC-blocking capacitor
14	GND	Connect to GND
15	Vdet	Power detector output
16	Vref	Power detector reference voltage
17	Vd3	Stage 3 drain voltage (or use pin 10)
18	GND	Connect to GND
19	Vd12	Stage 1 and 2 drain voltage (or use pin 8)
20	NC	Connect to GND
Die pad	GND	DC and RF ground. Exposed die pad must be connected to GND.

Notes
CML recommends that all no connect (NC) pins are connected to ground.
The bottom exposed die pad must be connected to the ground plane on the board.

Typical Performance

The following plots show typical performance characteristics of CMX90A702 measured on the evaluation board (Part Number EV90A702). Board losses have been de-embedded from the measurements, and s-parameter results are taken using TRL calibration technique.

Test conditions unless otherwise noted:-
Vd12 = Vd3 = 4.0 V, Idq12 = 73 mA, Idq3 = 109 mA, Ta = 25 ˚C, Zo = 50 Ω

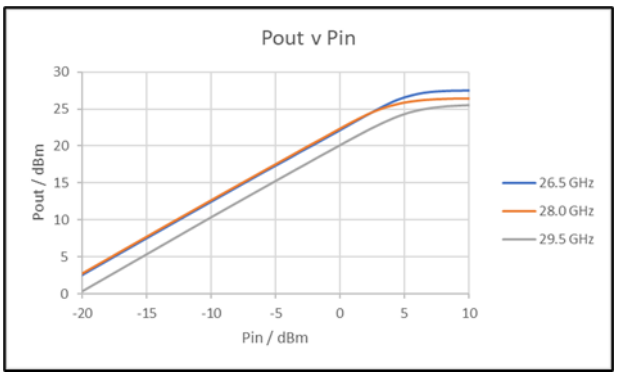


Figure 1: Pout v Pin

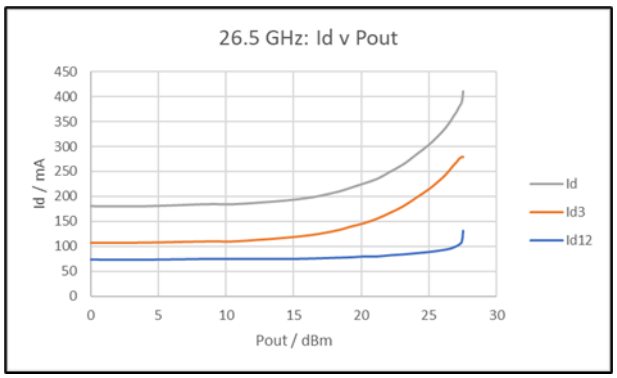


Figure 2: 26.5 GHz: Id v Pout

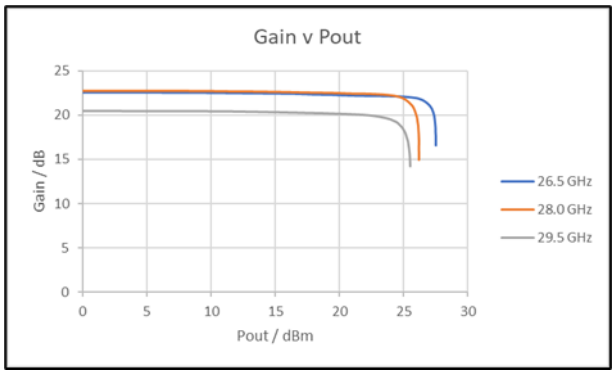


Figure 3: Gain v Pout

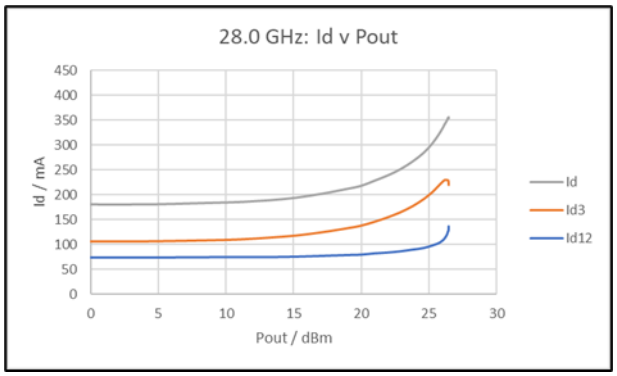


Figure 4: 28.0 GHz: Id v Pout

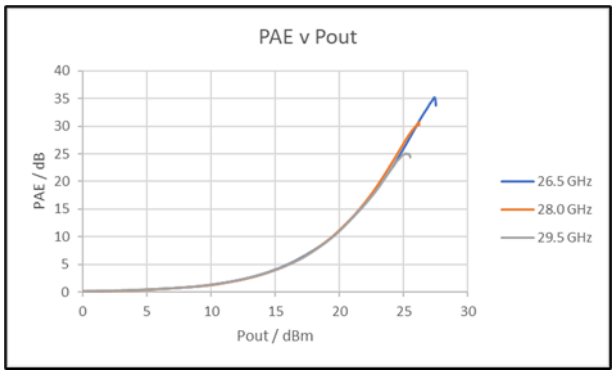


Figure 5: PAE v Pout

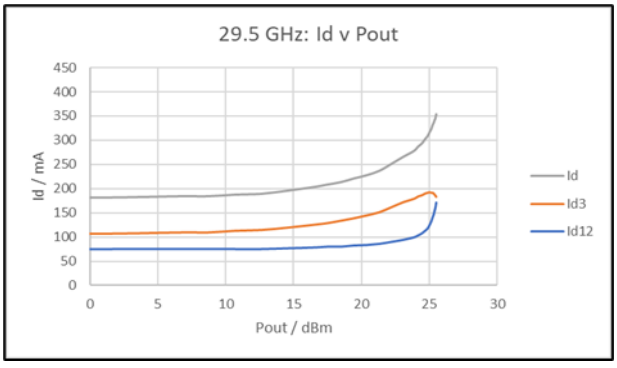


Figure 6: 29.5 GHz: Id v Pout

Test conditions unless otherwise noted:-
Vd12 = Vd3 = 4.0 V, Idq12 = 73 mA, Idq3 = 109 mA, Ta = 25 ˚C, Zo = 50 Ω

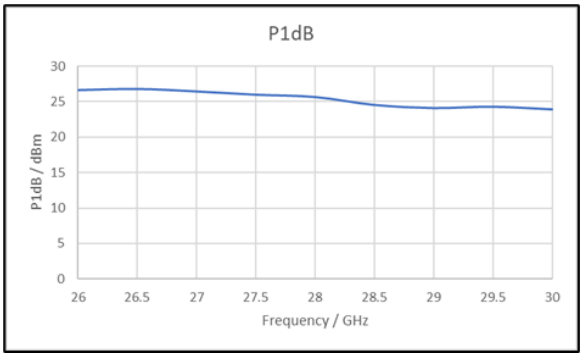


Figure 7: P1dB

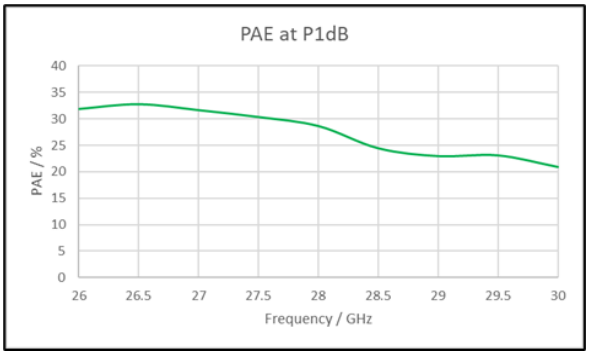


Figure 8: PAE at P1dB

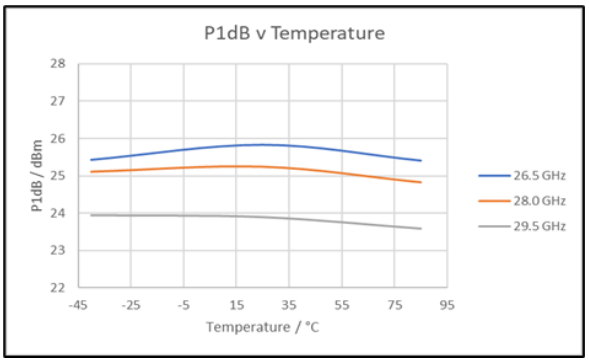


Figure 9: P1dB v Temperature

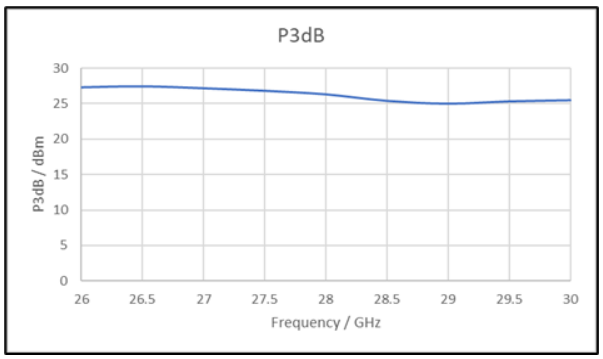


Figure 10: P3dB

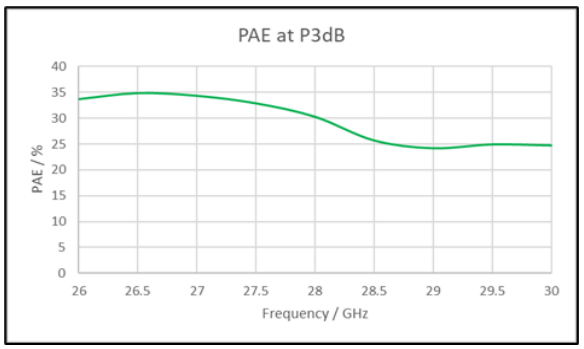


Figure 11: PAE at P3dB

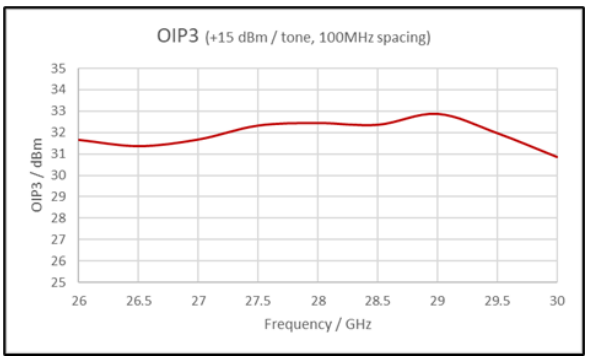


Figure 12: OIP3

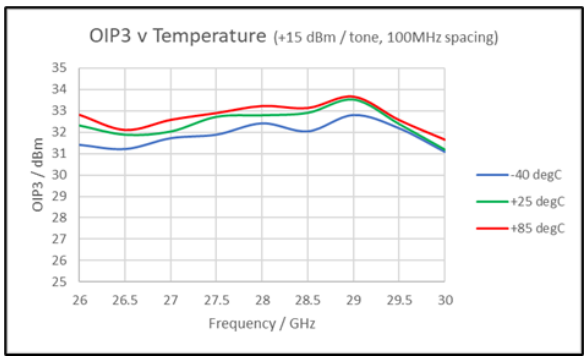


Figure 13: OIP3 v Temperature

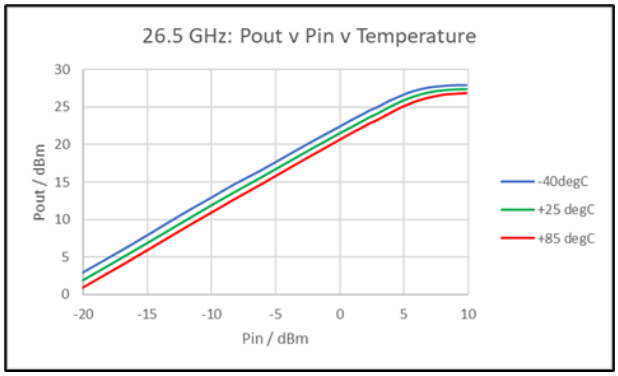


Figure 14: 26.5 GHz – Pout v Pin v Temperature

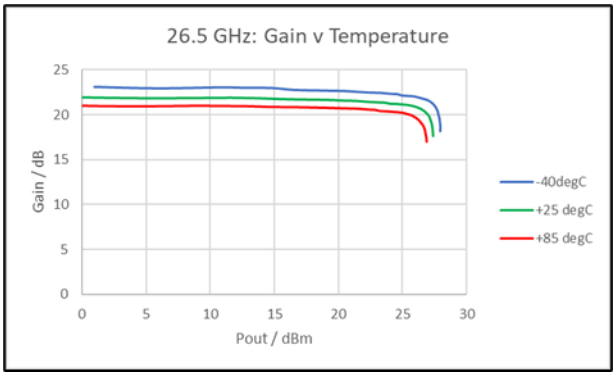


Figure 15: 26.5 GHz – Gain v Temperature

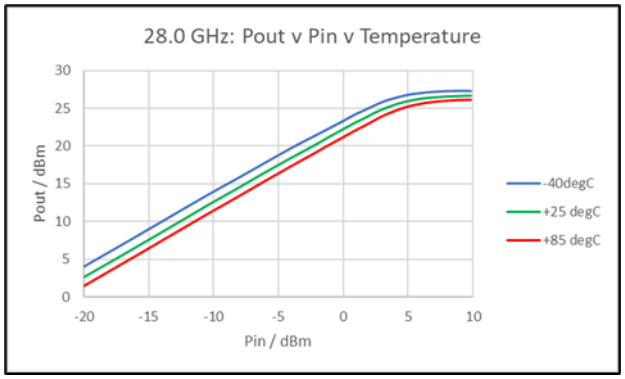


Figure 16: 28.0 GHz – Pout v Pin v Temperature

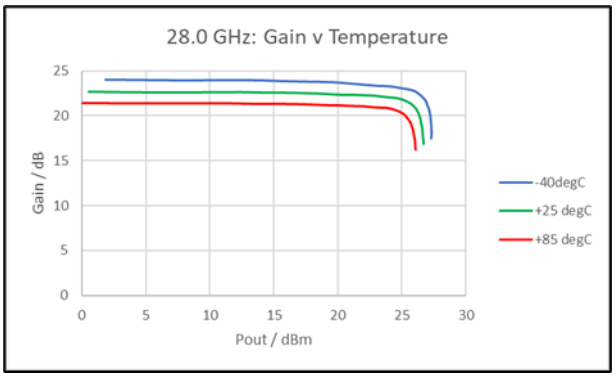


Figure 17: 28.0 GHz – Gain v Temperature

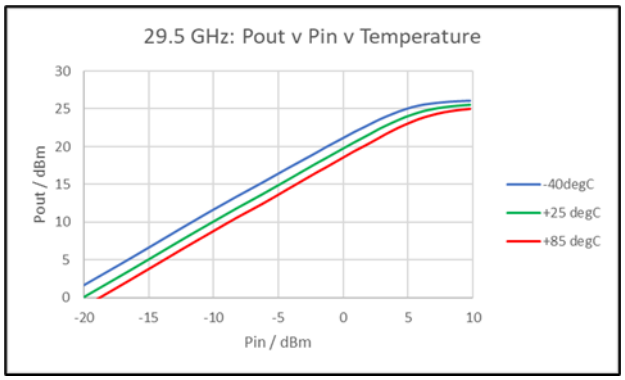


Figure 18: 29.5 GHz – Pout v Pin v Temperature

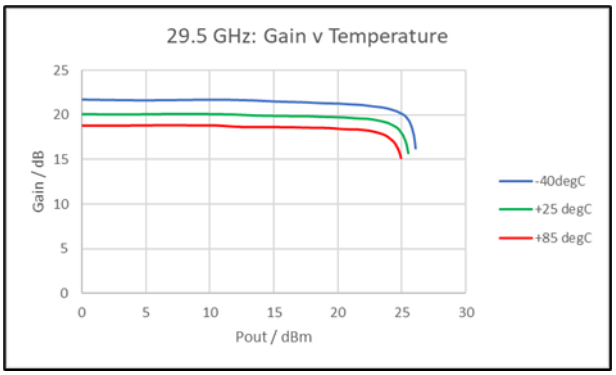


Figure 19: 29.5 GHz – Gain v Temperature

Test conditions unless otherwise noted:-
Vd12 = Vd3 = 4.0 V, Idq12 = 73 mA, Idq3 = 109 mA, Ta = 25 ˚C, Zo = 50 Ω

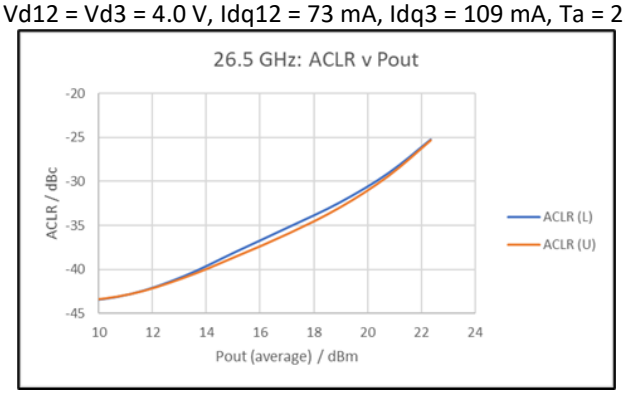


Figure 20: 26.5 GHz: ACLR v Pout

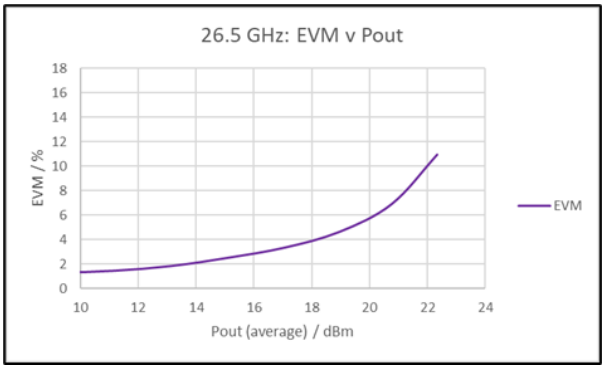


Figure 21: 26.5 GHz: EVM v Pout

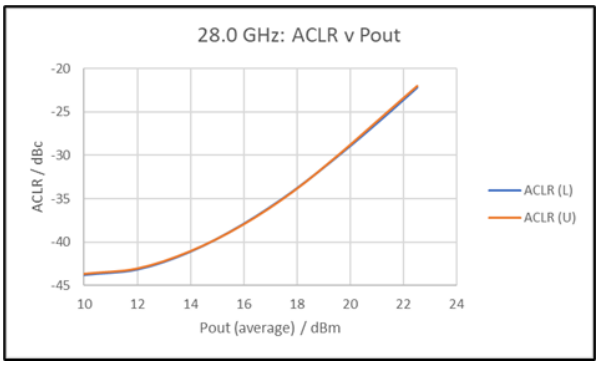


Figure 22: 28.0 GHz: ACLR v Pout

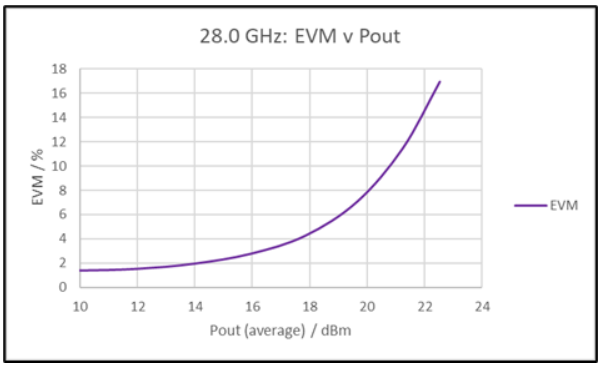


Figure 23: 28.0 GHz: EVM v Pout

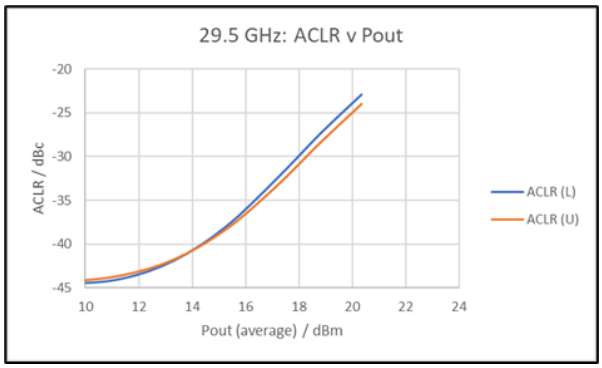


Figure 24: 29.5 GHz: ACLR v Pout

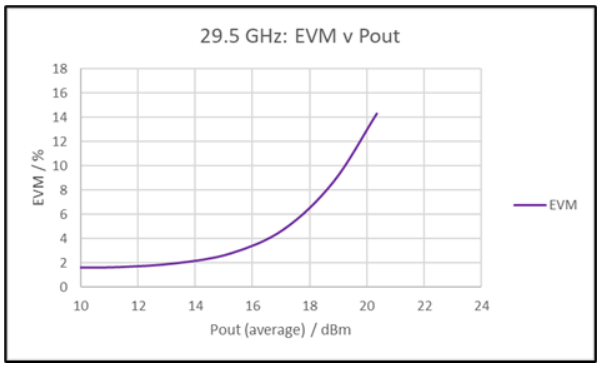


Figure 25: 29.5 GHz: EVM v Pout

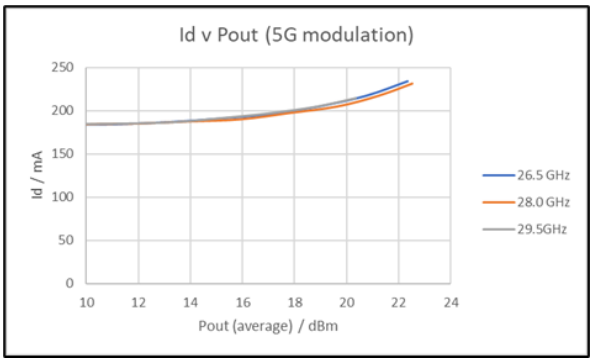


Figure 26: Id v Pout (5G modulation)

5G Test Signal:

Model: NR FR2 TM1.1
Bandwidth: 100MHz
Modulation: QPSK
Subcarrier Spacing: 60KHz
Number of frames: 1
Nominal PAR: 12.89

Test conditions unless otherwise noted:
Vd12 = Vd3 = 4.0 V, Idq12 = 73 mA, Idq3 = 109 mA, Ta = 25 ˚C, Zo = 50 Ω

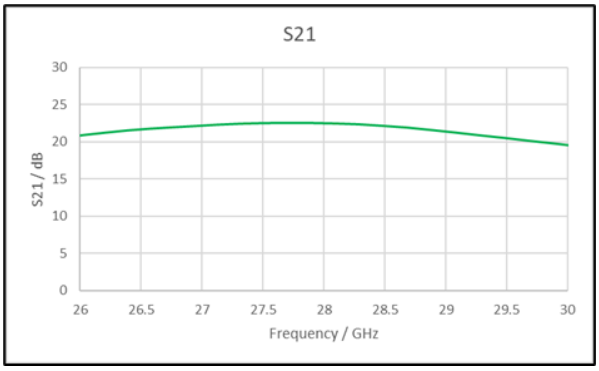


Figure 27: S21

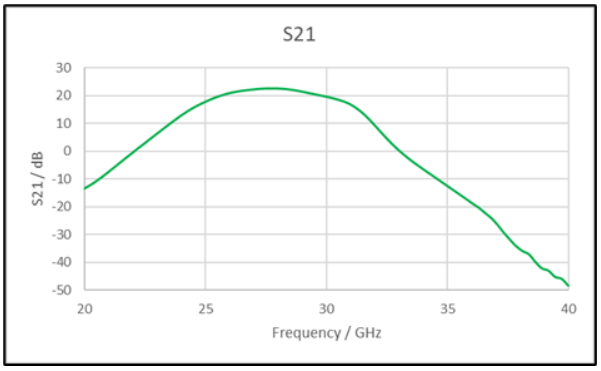


Figure 28: S21

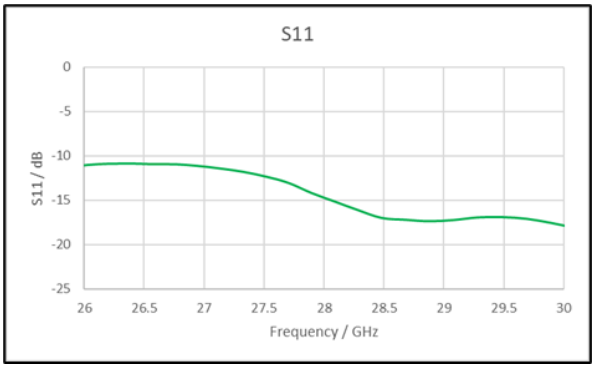


Figure 29: S11

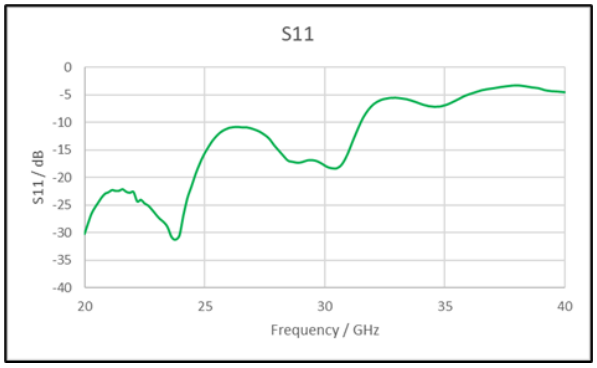


Figure 30: S11

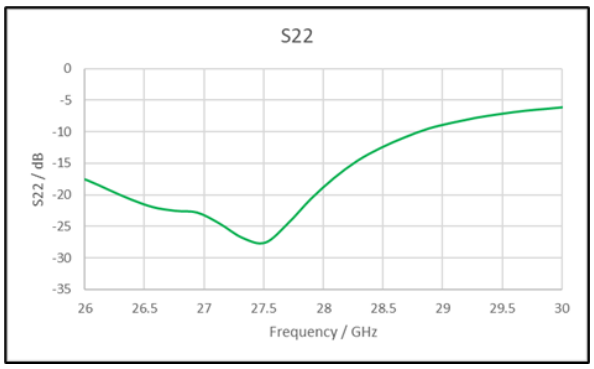


Figure 31: S22

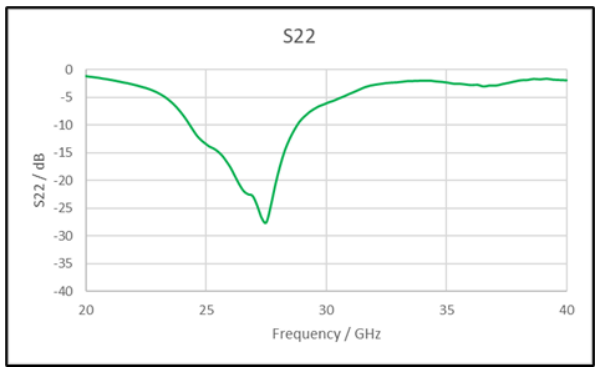


Figure 32: S22

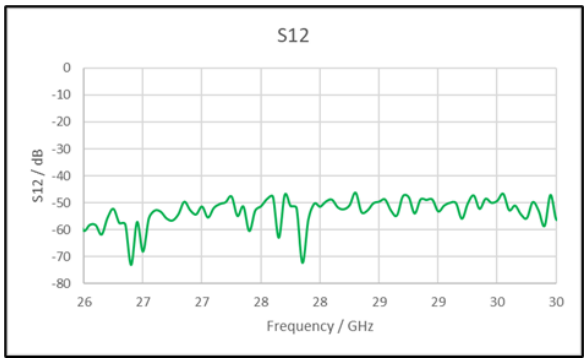


Figure 33: S12

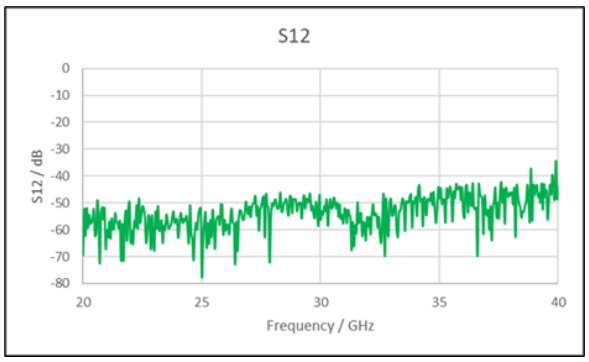


Figure 34: S12

Test conditions unless otherwise noted:
Vd12 = Vd3 = 4.0 V, Idq12 = 73 mA, Idq3 = 109 mA, Ta = 25 ˚C, Zo = 50 Ω

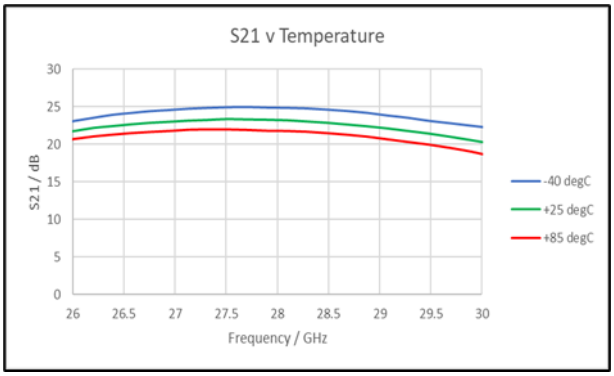


Figure 35: S21 v Temperature

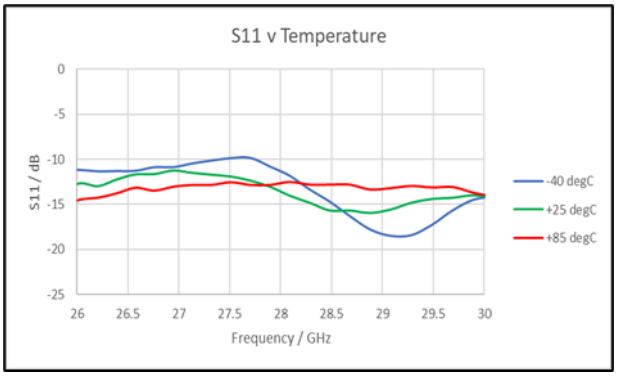


Figure 36: S11 v Temperature

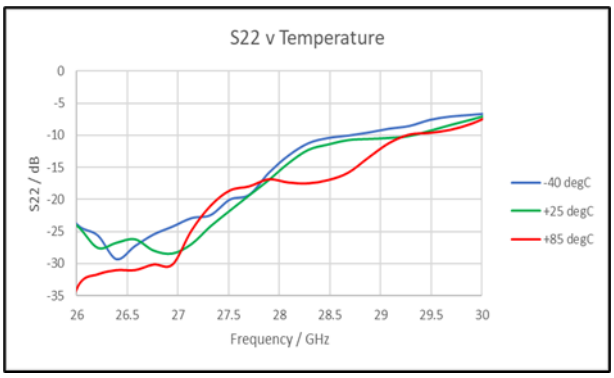


Figure 37: S22 v Temperature

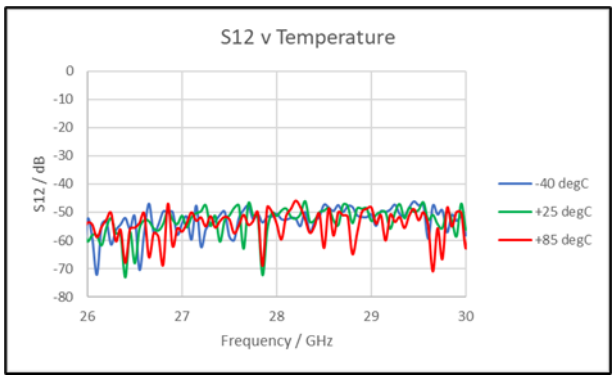


Figure 38: S12 v Temperature

Test conditions unless otherwise noted:
Vd12 = Vd3 = 4.0 V, Idq12 = 73 mA, Idq3 = 109 mA, Ta = 25 ˚C, Zo = 50 Ω

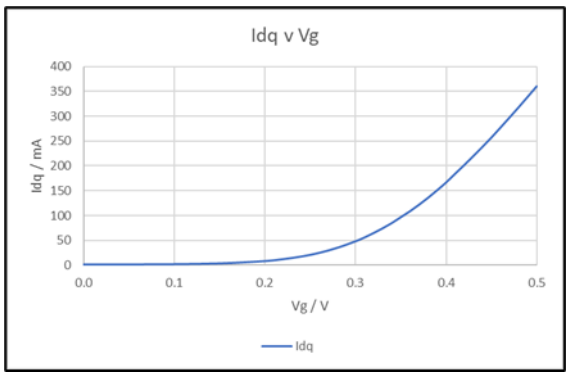


Figure 39: Idq v Vg

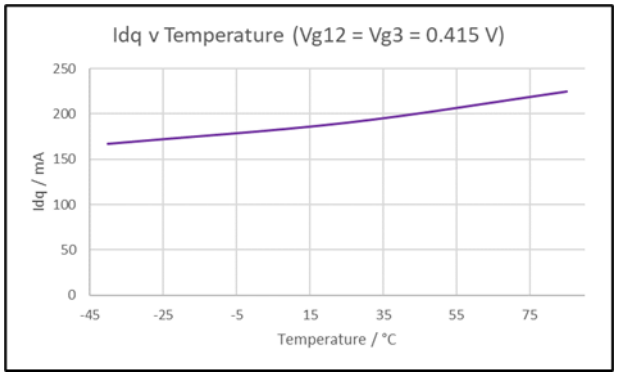


Figure 40: Idq v Temperature (Vg = 0.415 V)

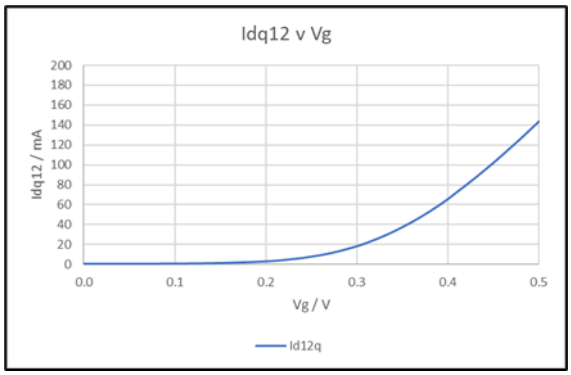


Figure 41: Idq12 v Vg

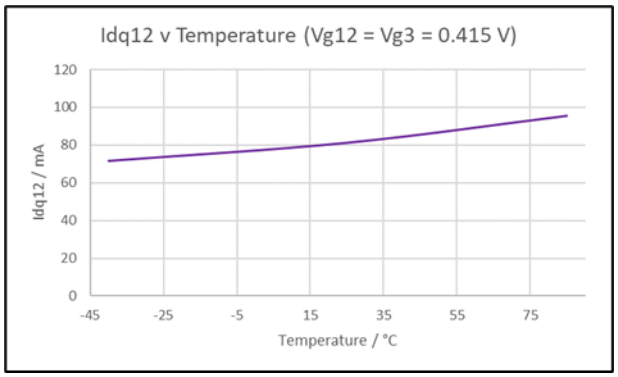


Figure 42: Idq12 v Temperature (Vg = 0.415 V)

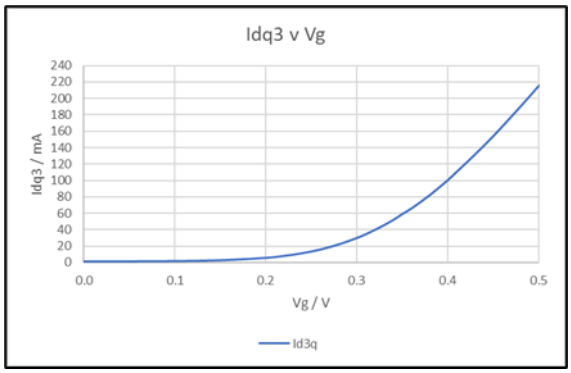


Figure 43: Idq3 v Vg

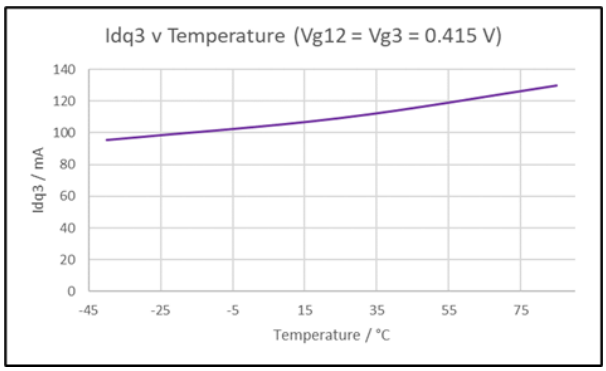


Figure 44: Idq3 v Temperature (Vg = 0.415 V)

Test conditions unless otherwise noted:-
Vd12 = Vd3 = 4.0 V, Idq12 = 73 mA, Idq3 = 109 mA, Ta = 25 ˚C, Zo = 50 Ω

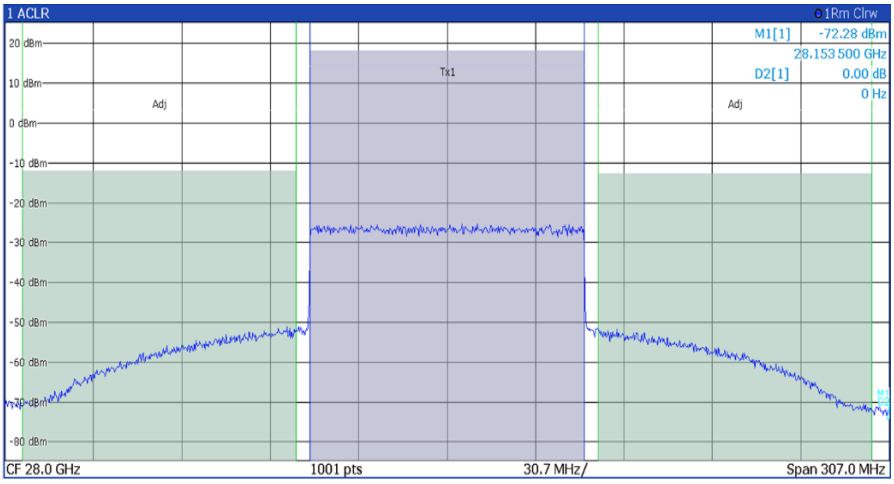


Figure 45: ACLR at +18dBm

5G Test Signal:
Model: NR FR2 TM1.3
Bandwidth: 100 MHz
Modulation: 64QAM
Subcarrier Spacing: 60 kHz
Number of frames: 1
Nominal PAR: 14.62 dB

Pout (mean): +18 dBm

ACLR Lower: -30.05 dBc
ACLR Upper: -30.57 dBc

EVM PDSCH 64QAM: 5.9 % Mean
Measured Crest Factor: 8.62 dB

Application Information

Schematic Diagram

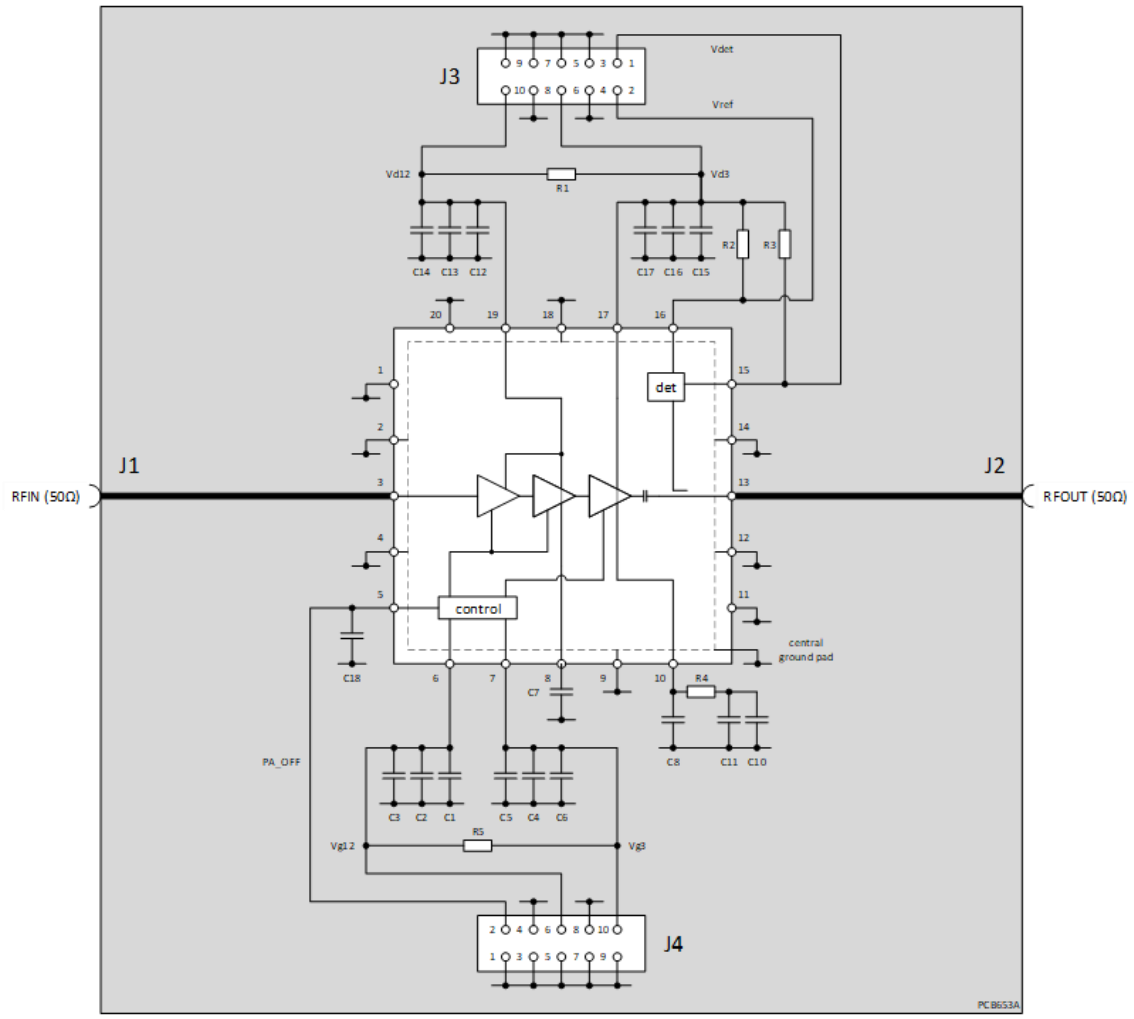


Figure 46: EV90A702 Schematic

Bill Of Materials (BOM)

Reference Designator	Value	Size	Description
C1, C5	100 pF	0402	100V, COG, +/-10 %
C7, C8, C13, C17	1 nF	0402	100V, X7R, +/-10 %
C3, C6, C14, C15	10 uF	TajA	10V, Tant
C2, C4, C11, C12, C16, C18	DNF	0402	100V, X7R, +/-10 %
C10	DNF	TajA	10V, Tant
R1, R4, R5	DNF		
R2, R3	7k5	0402	0.063 W, +/-1%
J1, J2	FL38J7-LS502SQA06	2.92mm	Frontlynk, 2.92 mm Connector
J3, J4	TFM-105-02-L-DH		Samtec 10-way Connector
IC1	CMX90A702QH		

Notes

- DNF = Do not fit component
- The DC headers on the EV90A702 are Samtec Tiger-Eye TFM-105-02-L-DH and should be used with Samtec SFSD-05[1] sockets.

[1] Pre-made cables in different lengths can be purchased with SAMTEC connector to free end configuration – for example part# SFSD-05-28-H-10.00-SR is 10” length (see Digikey site SFSD-05-28-H-10.00-SR Samtec Inc. | Cable Assemblies | DigiKey)

PCB Layout

Careful layout of the printed circuit board (PCB) is essential for optimum RF and thermal performance. The recommended layout, including ground via pattern underneath the device, may be taken from the evaluation board (Part Number EV90A702).

The PCB is a single layer of R04003, 8 thou thickness with ½ copper mounted to aluminium carrier with Ablefilm adhesive (0.05mm thick CF3350) which provides rigidity and thermal dissipation (Figure 47) and the EV90A702 PCB (Figure 48) is 26 mm x 50 mm. The coplanar RF transmission lines have a width of 0.33 mm with a gap of 0.21 mm to ground either side.

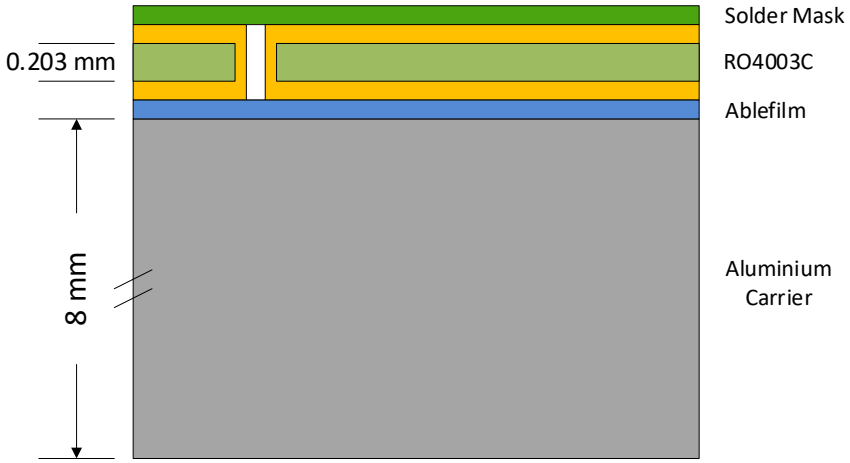


Figure 47: EV90A702 Layer Stack

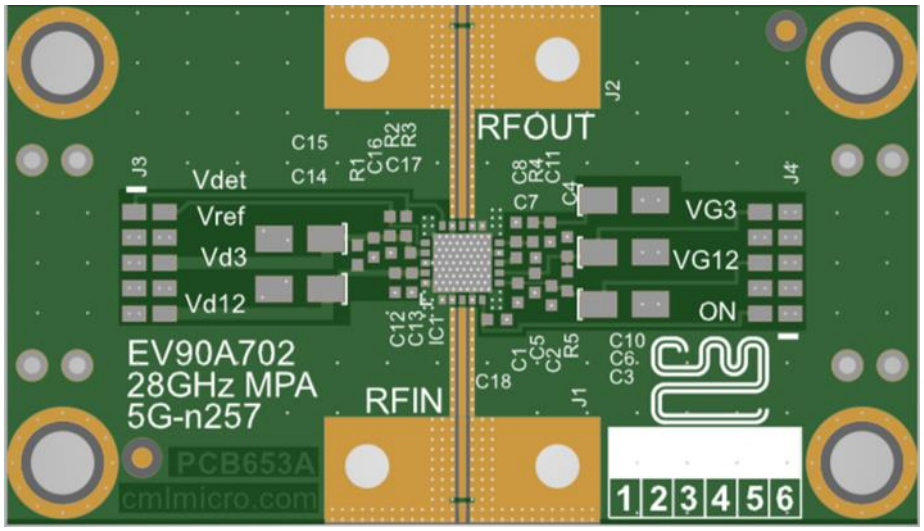


Figure 48: EV90A702 PCB Top Layer View

Thermal Design

The primary RF/DC ground and thermal path is via the exposed die pad on the back side of the package, which must be connected to the PCB ground plane. An array of plated and copper filled through-hole vias directly underneath the die pad area is needed to conduct heat away and minimise ground inductance. The PCB layout should provide a thermal radiator appropriate for the intended operation, adding as much copper to inner and outer layers as possible to avoid excessive junction temperature.

Device junction temperature (Tj) can be calculated using Tj = Tc + (Pdiss x Rjc) where Pdiss = Pdc + Pin – Pout and Tc is the case temperature on the backside of the package (die pad) in contact with the PCB.

Bias Procedure

The CMX90A702 is a three-stage enhancement mode amplifier and therefore requires positive gate voltage to set the quiescent drain currents. Stages 1 and 2 have common gate and drain connections and Stage 3 has separate gate and drain connections.

Power-up:

- Connect the amplifier in a 50Ω environment, with no RF input.
- Ensure the gate voltages (Vg12 and Vg3) are set to 0 V.
- Apply drain supplies (Vd12 and Vd3) at 4V.
- Increase Vg12 to set Id12 to 73 mA (Vg12 ~ 0.415 V).
- Increase Vg3 to set Id3 to 109 mA (Vg3 ~ 0.415 V).
- A suitable RF input can now be applied.

Power -down:

- Turn off the applied RF input.
- Decrease Vg12 and Vg3 to 0 V.
- Switch off drain supplies (Vd12 and Vd3).
- Switch off Vg12 and Vg3.

RFin

RFin (pin 3) is internally matched to 50 Ω. Note that at DC this pin is resistive to ground (approximately 50 Ω) and therefore DC voltages should not be applied to this pin.

RFout

RFout (pin 13) is internally matched to 50 Ω and DC blocking with an integrated blocking capacitor.

Vd12 and Vd3

The drain supply pins are replicated on both sides of the device and are connected internally. The drain connections only need to be made to one side, therefore for Vd12 either pin 8 or pin 19 can be used for stages 1 and 2. For Vd3 either pin 10 or pin 17 can be used for stage 3.

Vg12, Vg3 and PA_OFF

When PA_OFF (pin 5) is connected to ground, the gate voltages pass through the control circuit on to their relevant stages. When PA_OFF (pin 5) is high (nominally 2.5V), the gates voltages are disconnected from the stage gates which are also shorted to ground.

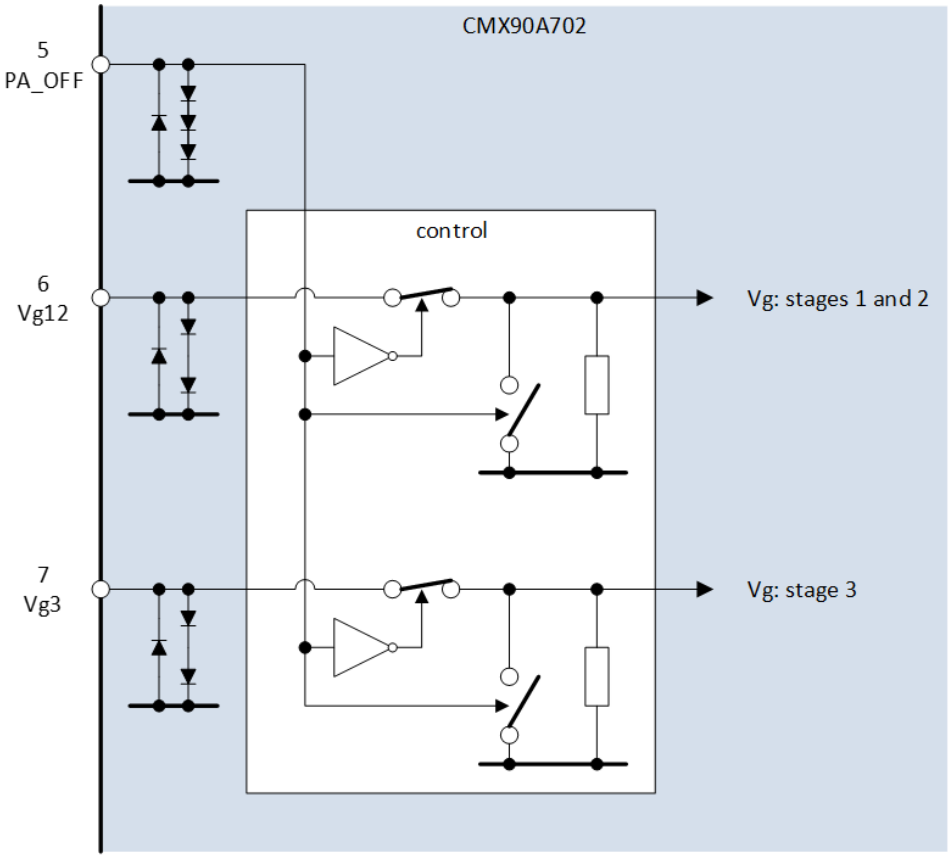


Figure 49: Control Circuit

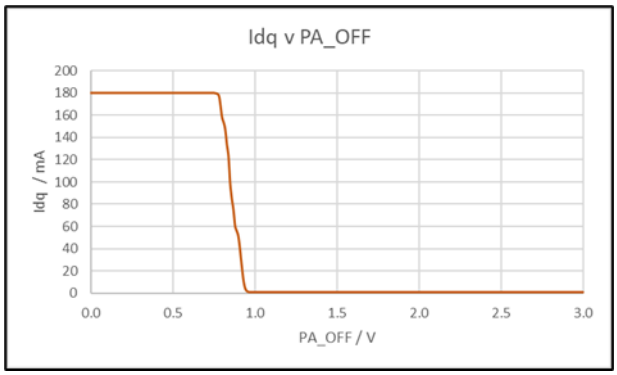


Figure 50: Idq v PA_OFF

Gate Current

With no or low levels of RF applied to the input and under the normal quiescent bias conditions, the current into the Vg12 and Vg3 pins will typically be between -25 µA and +25 µA.

As the RF input power is increased, the gate currents will change, initially moving negative and then positive as the input power reaches the datasheet maximum limit. There will be some variations with frequency, modulation and temperature. The range of gate currents to expect is:

	Low	High
Ig12	-0.3 mA	0.5 mA
Ig3	-0.75 mA	8 mA

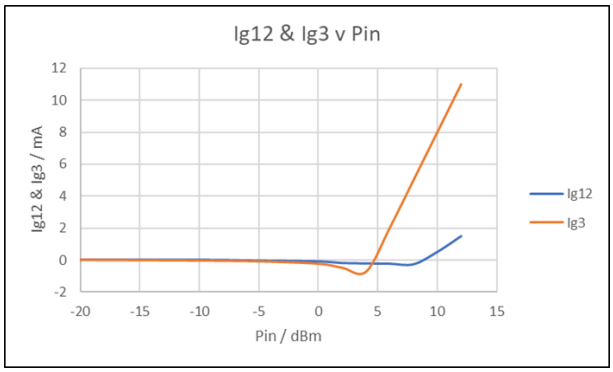


Figure 51: Ig12 & Ig3 v Pin

As the gate currents can be negative, a gate supply that can both sink and source current is needed. Many test power supplies have this capability however some may not. In that case a pull-down resistor can be used between the gate connection and ground with a value chosen to ensure that the most negative gate current through it does not generate a gate voltage high enough to interfere with the normal biasing. Suggested values are 1 kΩ (Vg12) and 400 Ω (Vg3).

If the gate supply is not capable of sourcing sufficient positive current, an op-amp with an emitter follower can be used. The emitter follower both increases the source current capability and buffers the op-amp from capacitive loads that are likely to cause instability if connected directly to the op-amp output. A suggested gate driver is shown in Figure 52 below.

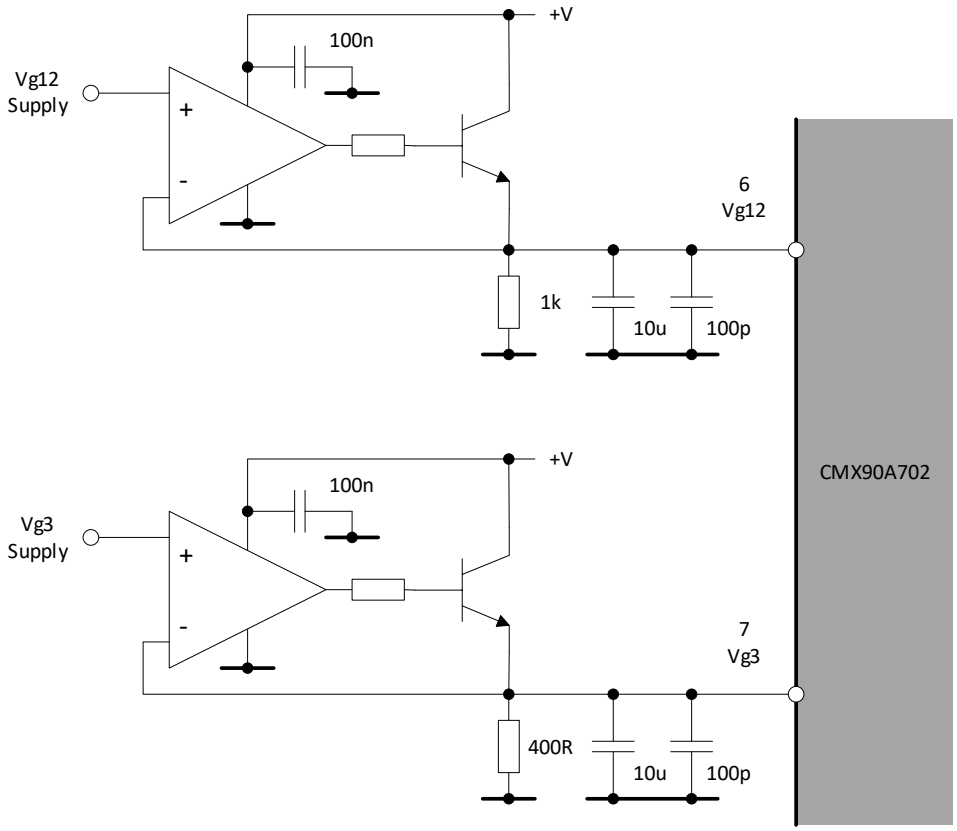


Figure 52: Suggested Gate Driver

With a suitable choice of low voltage, single supply op-amp, the +V supply can be derived from a convenient low voltage supply. For example, the OPA990 operates down to 2.7 V making operation from a 3.3V supply or from the Vd supply suitably decoupled. The NPN transistor needs to be capable of operating with a collector current at the highest expected Ig. Note that the transistor also needs to be capable of operating with a power dissipation of Ic x Vce. For a case of Ig at 8 mA and Vg of 0.415 V from a 4 V supply, the dissipation would be 0.008 x (4 – 0.415) = 29 mW.

Output Detector

The integrated detector is coupled to the RFout. With no RF output and an external 7.5 kΩ connected to 4 V, the detector gives approximately a 2 V output, which is temperature dependent due to the detector diode. An additional reference diode and equal value resistors are also included. This allows the detector to be temperature compensated by taking the differential voltage Vref - Vdet.

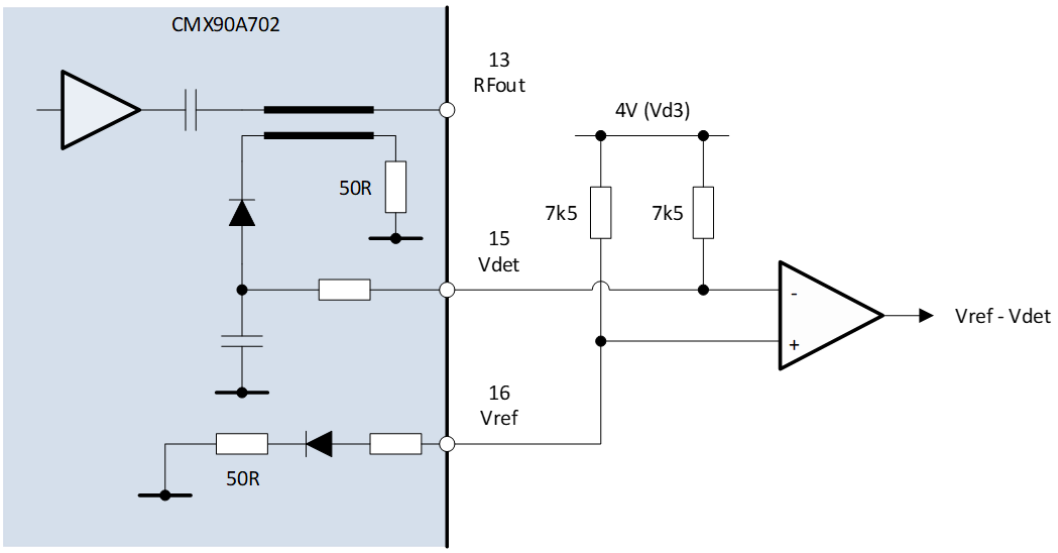


Figure 53: Output Detector

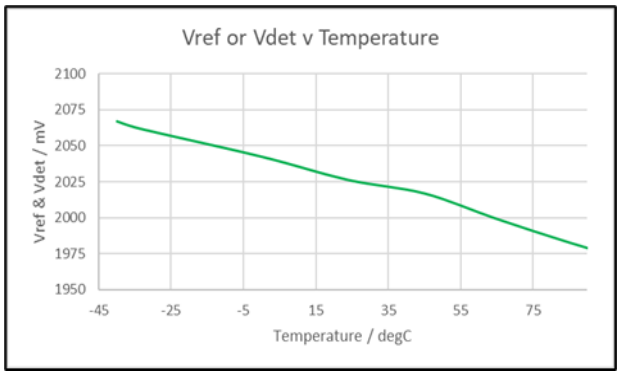


Figure 54: Vref or Vdet v Temperature

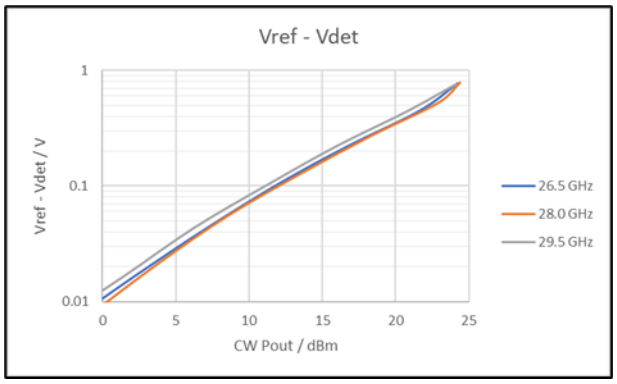
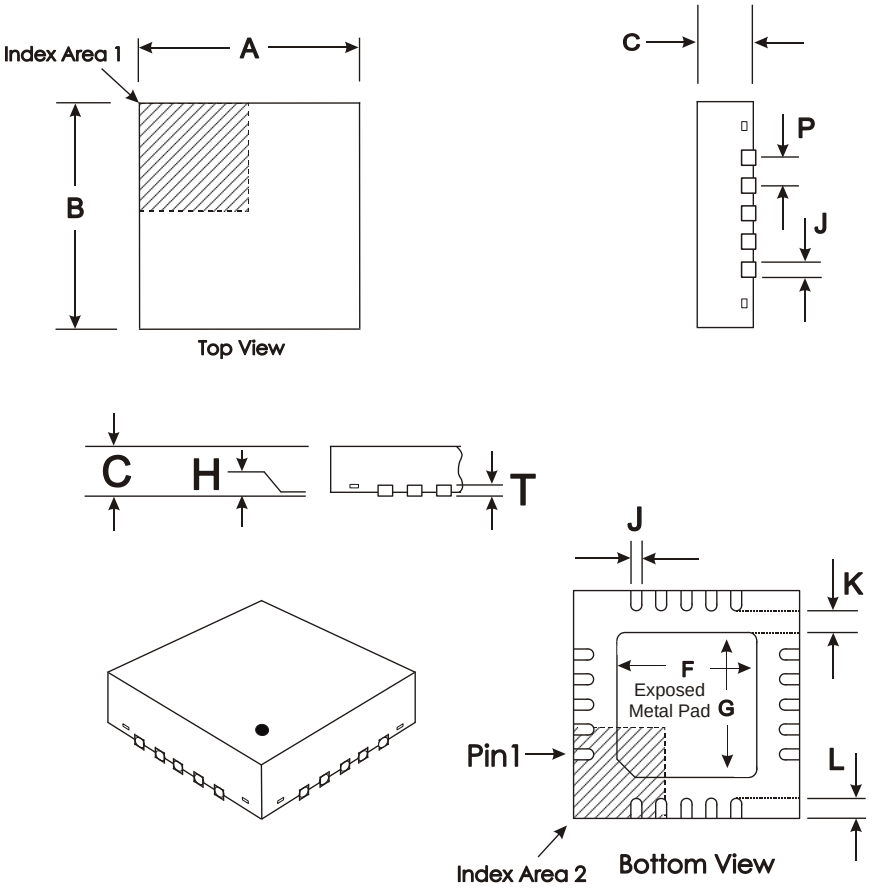


Figure 55: Detector Output (Vref – Vdet)

Package Outline

20-lead 4x4mm VQFN Package (QH)

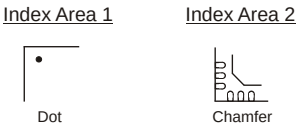


	DIM.	MIN.	TYP.	MAX.
*	A		4.00 BSC	
*	B		4.00 BSC	
	C	0.80	0.90	1.00
	F	2.55		2.80
	G	2.55		2.80
	H	0.00		0.05
	J	0.18	0.25	0.30
	K	0.20		
	L	0.225	0.325	0.425
	P		0.50	
	T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

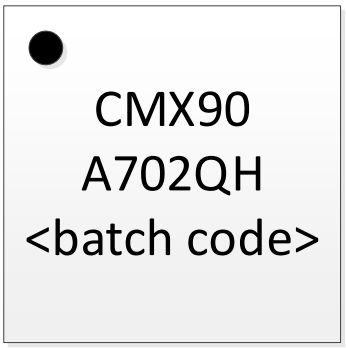
All dimensions in mm
Angles are in degrees



Index Area 1 is located directly above Index Area 2

Package Marking

Pin 1 indicator (dot) and 3 rows of text for device identification.



Line 1: CMX90 SµRF series

Line 2: 6-character part code

Line 3: Batch code

Revision History

Issue	Description	Date
2	Information on gate current added to Application section ESD data added to Absolute Maximum Ratings section	August 2022
1	Advance Information	June 2022

Contact Information

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