

Dual N-Channel Power MOSFET

20V, 6.0A, 30mΩ

FEATURES

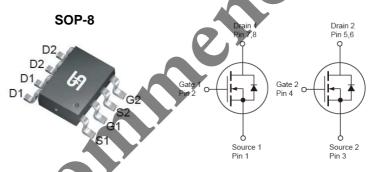
- Advance Trench Process Technology
- High Density Cell Design for Ultra Low Onresistance

KEY PERFORMANCE PARAMETERS				
PARAMETER		VALUE	UNIT	
V_{DS}		20	٧	
D (****)	$V_{GS} = 4.5V$	30		
$R_{DS(on)}$ (max)	$V_{GS} = 2.5V$	40	mΩ	
Q_g		4.86	nC	

APPLICATION

- Specially Designed for Li-on Battery Packs
- Battery Switch Application





Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current (Note 1)	$T_C = 25^{\circ}C$	I _D	6	Α
Pulsed Drain Current (Note 2)		I _{DM}	30	Α
Continuous Source Current (Diode Conduction)		I _S	1.7	Α
Tatal David Station	$T_A = 25^{\circ}C$	P _{DTOT}	1.6	W
Total Power Dissipation	T _A = 75°C		1.1	
Operating Junction and Storage Temperature Range		T _J , T _{STG}	- 55 to +150	°C

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	LIMIT	UNIT	
Junction to Case Thermal Resistance	R _{eJC}	40	°C/W	
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	77	°C/W	

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.



PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 3)		•				
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV _{DSS}	20			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	$V_{GS(TH)}$	0.6			V
Gate Body Leakage	$V_{GS} = \pm 12V, V_{DS} = 0V$	I _{GSS}			±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 20V, V_{GS} = 0V$	I _{DSS}			1	μA
On-State Drain Current	$V_{DS} = 5V, V_{GS} = 4.5V$	I _{D(ON)}	30	🔌		Α
	$V_{GS} = 4.5V, I_D = 6.0A$	R _{DS(ON)}		21	30	mΩ
Drain-Source On-State Resistance	$V_{GS} = 2.5V, I_D = 5.2A$			30	40	
Forward Transconductance	$V_{DS} = 10V, I_{D} = 6A$	g _{fs}		30		S
Dynamic (Note 4)				.		
Total Gate Charge		Q_g	/	4.86		
Gate-Source Charge	$V_{DS} = 10V, I_{D} = 6A,$	Q _{gs}		0.92		nC
Gate-Drain Charge	$V_{GS} = 4.5V$	Q_{gd}		1.4		
Input Capacitance		C _{iss}		562		
Output Capacitance	$V_{DS} = 8V, V_{GS} = 0V,$ F = 1.0MHz	Coss		106		pF
Reverse Transfer Capacitance	F = 1.UIVID2	C _{rss}		75		
Switching (Note 5)	4					
Turn-On Delay Time		t _{d(on)}		8.1		
Turn-On Rise Time	$V_{DD} = 10V$	t _r		9.95		
Turn-Off Delay Time	$R_{GEN} = 6\Omega$,	t _{d(off)}		21.85		ns
Turn-Off Fall Time	$I_D = 1A$, $V_{GS} = 4.5V$,	t _f		5.35		
Source-Drain Diode (Note 3)						
Forward Voltage	I _S = 1.7A, V _{GS} = 0V	V _{SD}		0.7	1.2	V

Notes:

- 1. Pulse width limited by the Maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 5 sec.
- 3. Pulse test: PW \leq 300µs, duty cycle \leq 2%.
- 4. For DESIGN AID ONLY, not subject to production testing.
- 5. Switching time is essentially independent of operating temperature.



ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM9926DCS RLG	SOP-8	2,500pcs / 13" Reel

Note:

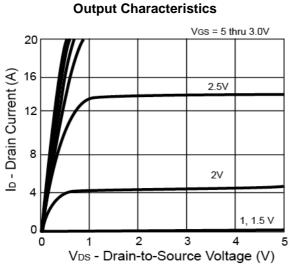
- 1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21 definition

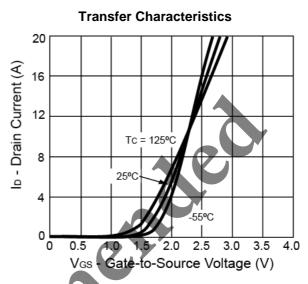


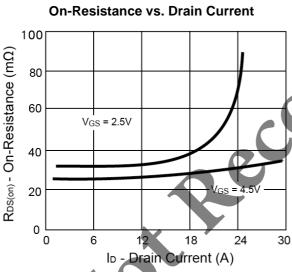


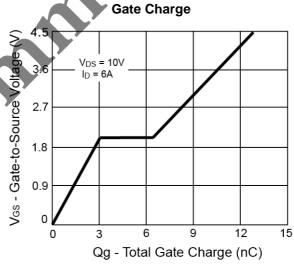
CHARACTERISTICS CURVES

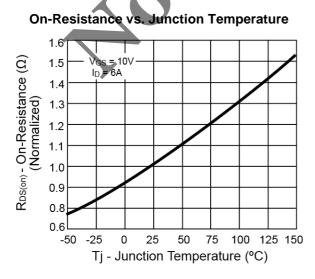
 $(T_A = 25^{\circ}C \text{ unless otherwise noted})$

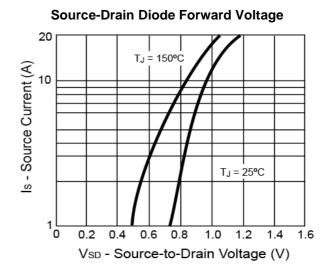








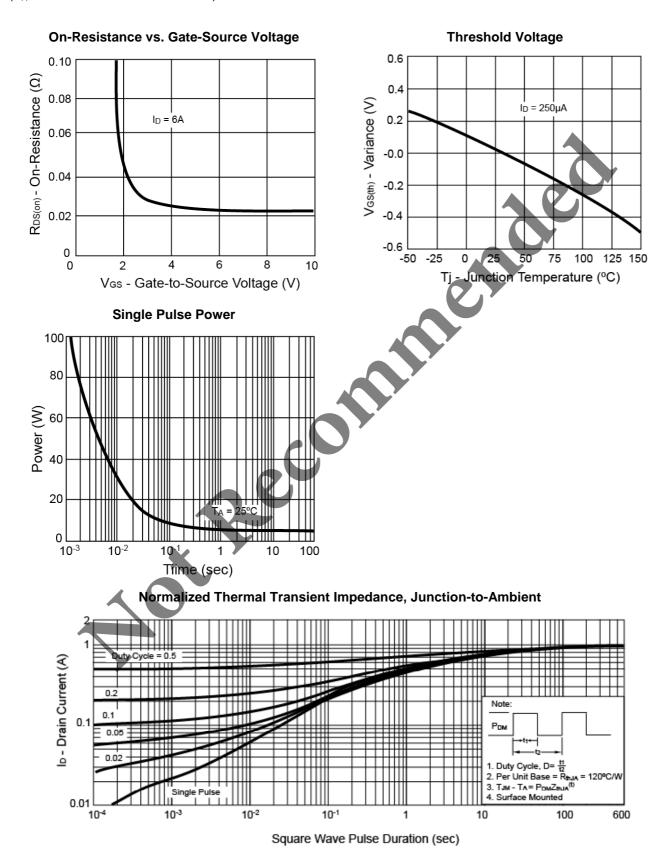






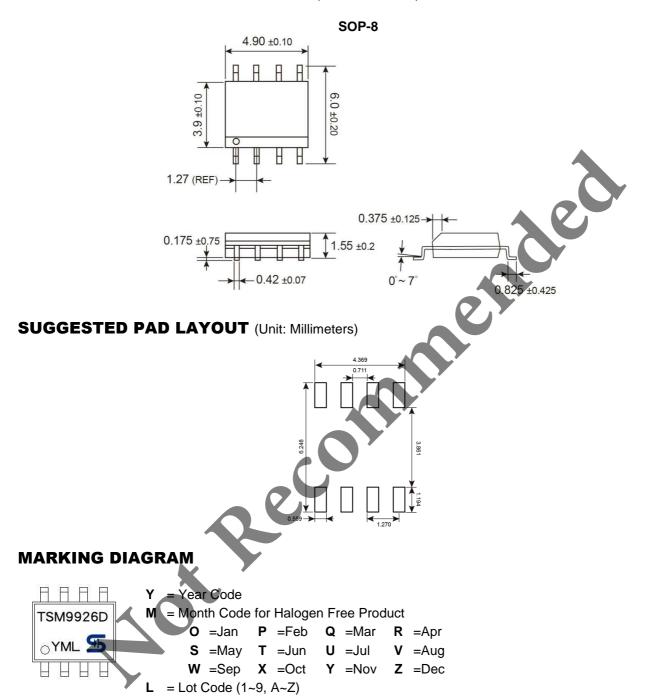
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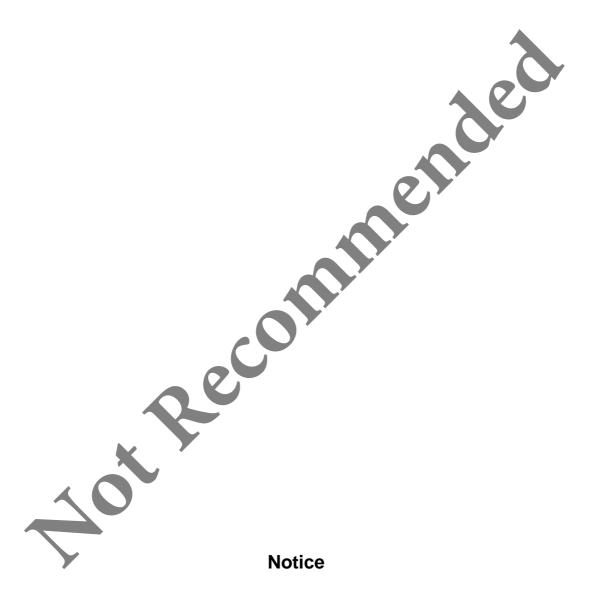




PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)







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