- **Qualified for Automotive Applications**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C_L = 200 pF, R_L = 0)**
- **2.7-V Operation**
- **Two Differential Microphone Inputs, One Differential Earphone Output, and One Single-Ended Earphone Output**
- **Programmable Gain Amplifiers for Transmit, Receive, Sidetone, and Volume Control**
- **Earphone Mute and Microphone Mute**
- **On-Chip I^2C Bus, Which Provides a Simple, Standard, Two-Wire Serial Interface With Digital ICs**
- **Programmable for 15-Bit Linear Data or 8-Bit Companded (μ-Law or A-Law) Data**
- **Available in a 32-Pin Thin Quad Flatpack (TQFP) Package**
- **Designed for Analog and Digital Wireless Handsets and Telecommunications Applications**
- **Dual-Tone Multifrequency (DTMF) and Single Tone Generator**
- **Pulse Density Modulated (PDM) Buzzer Output**

description

The voice-band audio processor (VBAP) is designed to perform transmit encoding analog/digital (A/D) conversion, receive decoding digital/analog (D/A) conversion, and transmit and receive filtering for voice-band communications systems. The device operates in either the 15-bit linear or 8-bit companded (μ-law or A-Law) mode, which is selectable through the I^2C interface. The VBAP generates its own internal clocks from a 2.048-MHz master clock input.

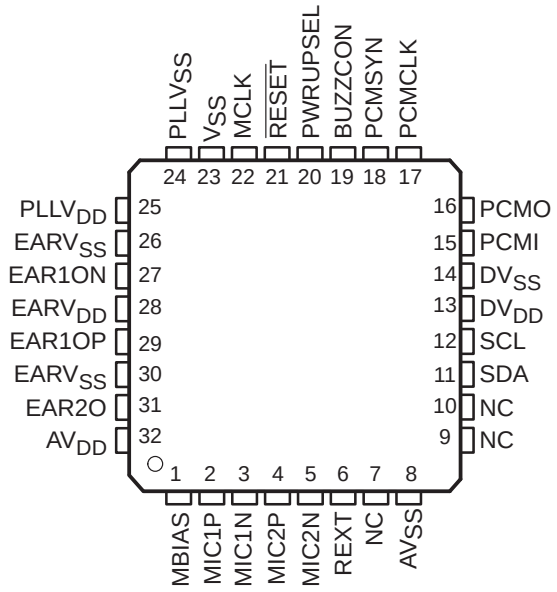
AVAILABLE OPTIONS†

T_A	TQFP PBS PACKAGE‡	PART NO.	TOP-SIDE MARKING
−40°C to 105°C	Tube	TWL1103TPBSQ1	TWL1103T
	Tape and Reel	TWL1103TPBSRQ1	TWL1103T

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

PBS PACKAGE
(TOP VIEW)



NC − No internal connection

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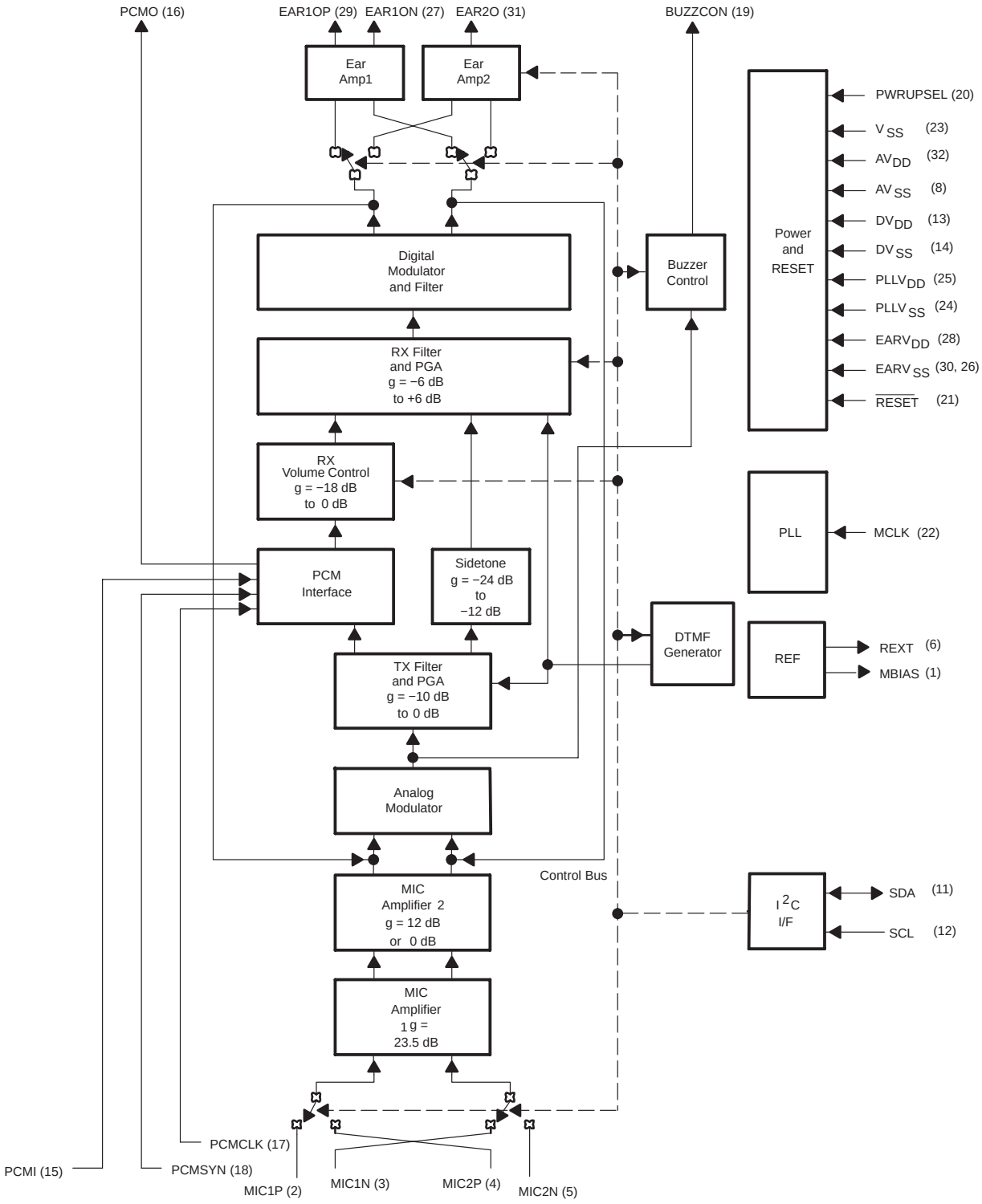
functional block diagram



functional description

power on/reset

The power for the various digital and analog circuits is separated to improve the noise performance of the device. An external reset must be applied to the active low $\overline{\text{RESET}}$ terminal to guarantee reset upon power on. After the initial power-on sequence the TWL1103 can be functionally powered up and down by writing to the power control register through the I^2C interface. There is a hardwired selectable power-up terminal in default mode option. The PWRUPSEL function allows the VBAP to power up in the default mode and allows use without a microcontroller.

reference

A precision band gap reference voltage is generated internally and supplies all required voltage references to operate the transmit and receive channels. The reference system also supplies bias voltage for use with an electret microphone at terminal MBIAS. An external precision resistor is required for reference current setting at terminal REXT.

control interface

The I^2C interface is a two-wire bidirectional serial interface that controls the VBAP by writing data to the six control registers:

- Power control
- Mode control
- Transmit PGA and sidetone control
- Receive PGA gain and volume control
- DTMF high tone
- DTMF low tone

There are two power-up modes which may be selected at the PWRUPSEL terminal:

- The PWRUPSEL state (V_{DD} at terminal 20) causes the device to power up in the default mode when power is applied. In the default mode, the I^2C interface is not required, and the device may be used without an I^2C interface. The programmable functions are fixed in the default modes.
- The PWRUPSEL state (ground at terminal 20) causes the device to go to a power-down state when power is applied. In this mode an I^2C interface is required to power up the device.

phase-locked loop

The internal digital filters and modulators require a 10.24-MHz clock that is generated by phase locking to the 2.048-MHz master clock input.

PCM interface

The PCM interface transmits and receives data at the PCMO and PCMI terminals respectively. The data is transmitted or received at the PCMCLK speed once every PCMSYN cycle. The PCMCLK can be tied directly to the 2.048-MHz master clock (MCLK). The PCMSYN can be driven by an external source or derived from the master clock and used as an interrupt to the host controller.

microphone amplifiers

The microphone input is a switchable interface for two differential microphone inputs. The first stage is a low-noise differential amplifier that provides a gain of 23.5 dB. The second stage amplifier has a selectable gain of 0 dB or 12 dB.

functional description (continued)

analog modulator

The transmit channel modulator is a third-order sigma-delta design.

transmit filter and PGA

The transmit filter is a digital filter designed to meet CCITT G.714 requirements. The device operates in either the 15-bit linear or 8-bit companded μ-law or A-law mode that is selectable through the I^2C interface. The transmit PGA defaults to 0 dB.

sidetone

A portion of the transmitted audio is attenuated and fed back to the receive channel through the sidetone path. The sidetone path defaults to −12 dB. The sidetone path can be enabled by writing to the power control register.

receive volume control

The receive volume control block acts as an attenuator with a range of −18 dB to 0 dB in 2 dB steps for control of the receive channel volume. The receive volume control gain defaults to 0 dB.

receive filter and PGA

The receive filter is a digital filter that meets CCITT G.714 requirements with a high-pass filter that is selectable through the I^2C interface. The device operates in either the 15-bit linear or 8-bit μ-law or A-law companded mode, which is selectable through the I^2C interface. The gain defaults to −1 dB representing a 3-dBm0 level for a 32-Ω load impedance and the corresponding digital full scale PCMI code. The gain may be set to −2 dB for the respective 3-dBm0 level for a 16-Ω load impedance.

digital modulator and filter

The second-order digital modulator and filter convert the received digital PCM data to the analog output required by the earphone interface.

earphone amplifiers

The analog signal can be routed to either of two earphone amplifiers, one with differential output (EAR1ON and EAR1OP) and one with single-ended output (EAR2O). Clicks and pops are suppressed for EAR1 differential output only.

tone generator

The tone generator provides generation of standard DTMF tones and single tone frequencies which are output to the following devices: 1) The buzzer driver, as a pulse density modulation (PDM) signal 2) The receive path digital/analog converter (DAC) for outputting through the earphone. There are 255 possible single tones. The tone integer value is determined by the following formula:

Round (Tone Freq (Hz)/7.8135 Hz)

The value is loaded into one of two 8-bit registers, the high-tone register (04), or the low-tone register (05). The tone output is 2 dB higher when applied to the high-tone register (04). When generating DTMF tones, the high DTMF tone must be applied to the high-tone register and the low frequency tone to the low-tone register.

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	μBGA	PBS		
AV_{DD}	A1	32	I	Analog positive power supply
AV_{SS}	J1	8	I	Analog negative power supply
BUZZCON	F9	19	O	Buzzer output, a pulse-density modulated signal to apply to external buzzer driver
DV_{DD}	J6	13	I	Digital positive power supply
DV_{SS}	J7	14	I	Digital negative power supply
EAR1ON	A6	27	O	Earphone 1 amplifier output (−)
EAR1OP	A4	29	O	Earphone 1 amplifier output (+)
EAR2O	A2	31	O	Earphone 2 amplifier output
$EARV_{DD}$	A5	28	I	Analog positive power supply for the earphone amplifiers
$EARV_{SS}$	A3, A7	30, 26	I	Analog negative power supply for the earphone amplifiers
MBIAS	B1	1	O	Microphone bias supply output, no decoupling capacitors
MCLK	C9	22	I	Master system clock input (2.048 MHz) (digital)
MIC1P	C1	2	I	MIC1 input (+)
MIC1N	D1	3	I	MIC1 input (−)
MIC2P	E1	4	I	MIC2 input (+)
MIC2N	F1	5	I	MIC2 input (−)
PCMI	J8	15	I	Receive PCM input
PCMO	J9	16	O	Transmit PCM output
PCMSYN	G9	18	I	PCM frame synchronization
PCMCLK	H9	17	I	PCM data clock
$PLLV_{SS}$	A9	24	I	PLL negative power supply
$PLLV_{DD}$	A8	25	I	PLL digital power supply
PWRUPSEL	E9	20	I	Selects the power-up default mode
REXT	G1	6	I/O	Internal reference current setting terminal—use precision 100-kΩ resistor and no filtering capacitors
$\overline{\text{RESET}}$	D9	21	I	Active low reset
SCL	J5	12	I	I^2C-bus serial clock—this input is used to synchronize the data transfer from and to the VBAP
SDA	J4	11	I/O	I^2C-bus serial address/data input/output—this is a bidirectional terminal used to transfer register control addresses and data into and out of the CODEC. It is an open-drain terminal and therefore requires a pullup resistor to V_{DD} (typical 10 kΩ for 100 kHz)
V_{SS}	B9	23	I	Ground return for bandgap internal reference

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, AV_{DD}, DV_{DD}, $PLLV_{DD}$, $EARV_{DD}$ . . . . . −0.5 V to 4 V
Output voltage range, V_O . . . . . −0.5 V to 4 V
Input voltage range, V_F . . . . . −0.5 V to 4 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free air temperature range, T_A (extended temperature) . . . . . −40°C to 105°C
Storage temperature range, testing, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 105°C$ POWER RATING
PBS	680 mW	6.8 mW/°C	270 mW	134 mW

recommended operating conditions (see Notes 1 and 2)

	MIN	NOM	MAX	UNIT
Supply voltage, AV_{DD}, DV_{DD}, $PLLV_{DD}$, $EARV_{DD}$	2.7		3.3	V
High-level input voltage (V_{IH})	0.7 x V_{DD}			V
Low-level input voltage (V_{IL})			0.3 x V_{DD}	V
Load impedance between EAR1OP and EAR1ON-R_L	16		32	Ω
Load impedance for EAR2OP-R_L		32		Ω
Operating free-air temperature, T_A	−40		105	°C

NOTES: 1. To avoid possible damage and resulting reliability problems to these CMOS devices, the power-on initialization paragraph must be followed, described in the Principles of Operations.
2. Voltages are with respect to AV_{SS}, DV_{SS}, $PLLV_{SS}$, and $EARV_{SS}$.

electrical characteristics, V_{DD} = 2.7 V, T_A = −40°C to 105°C (unless otherwise noted)

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current from V_{DD}	Operating, EAR1 selected, MicBias disabled		6	7	mA
		Operating, EAR2 selected, MicBias disabled		5.4	6	mA
		Power down, Reg 2 bit 7 = 1, MClk not present (see Note 3)		0.5	18	µA
		Power down, Reg 2 bit 7 = 0, MClk not present (see Note 3)		25	40	µA
$t_{on(i)}$	Power-up time from power down			5	10	ms

NOTE 3: $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$

digital interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, PCMO and BuzzCon	I_{OH} = −3.2 mA, V_{DD} = 3 V	2			V
V_{OL}	Low-level output voltage, PCMO and BuzzCon	I_{OL} = 3.2 mA, V_{DD} = 3 V			0.8	V
I_{IH}	High-level input current, any digital input	$V_I = V_{DD}$			10	µA
I_{IL}	Low-level input current, any digital input	$V_I = V_{SS}$			10	µA
C_I	Input capacitance				10	pF
C_o	Output capacitance				20	pF
R_L	Load impedance (BuzzCon)				5	kΩ

microphone interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage at MIC1N, MIC2N	See Note 4	−5		5	mV
I_{IB}	Input bias current at MIC1N, MIC2N		−600		600	nA
C_i	Input capacitance at MIC1N, MIC2N			5		pF
V_n	Microphone input referred noise, psophometric weighted (C-message weighted is similar)	Micamp 1 gain = 23.5 dB Micamp 2 gain = 0 dB		3.0	7.7	μV_{rms}
$I_O$max	Output source current MBIAS		1		1.2	mA
$V_{(mbias)}$	Microphone bias supply voltage (see Note 5)		2.35	2.5	2.6	V
	MICMUTE				−80	dB
	Input impedance	Fully differential	35	60	100	kΩ

NOTES: 4. Measured while MIC1P and MIC1N are connected together. Less than 5 mV offset results in 0 value code on PCMOUT.
5. Not a JEDEC symbol.

speaker interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Earphone AMP1 output power (See Note 6)		V_{DD} = 2.7 V, fully differential, 16-Ω load, 3-dBm0 output, RGXPA = −2 dB		120.9	151.1	mW
		V_{DD} = 2.7 V, fully differential, 32-Ω load, 3-dBm0 output, RGXPA = −1 dB		76.1	95.1	mW
Earphone AMP2 output power (See Note 6)		V_{DD} = 2.7 V, single ended, 32-Ω load, 3-dBm0 output		10	12.5	mW
V_{OO}	Output offset voltage at EAR1	Fully differential		±5	±30	mV
$I_O$max	Maximum output current for EAR1(rms)	3-dBm0 input, 16-Ω load		86.9	108.6	mA
		3-dBm0 input, 32-Ω load		48.7	60.8	
	Maximum output current for EAR2 (rms)	3-dBm0 input		17.7	22.1	
	EARMUTE				−80	dB

NOTE 6: Maximum power is with a load impedance of approximately 12 Ω.

electrical characteristics, V_{DD} = 2.7 V, T_A = −40°C to 105°C (unless otherwise noted) (continued)

transmit gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, transmit slope filter bypassed (see Notes 7 and 8)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit reference-signal level (0 dB)	Differential			175	mV_{pp}
Overload-signal level (3 dBm0)	Differential, normal mode			248	mV_{pp}
	Differential, extended mode			63	mV_{pp}
Absolute gain error	0 dBm0 input signal, V_{DD} = 2.7 V (minimum)	−1		1	dB
Linear mode gain error with input level relative to gain at −10 dBm0 MIC1N, MIC1P to PCMO	MIC1N, MIC1P to PCMO at 3 dBm0 to −30 dBm0	−0.5		0.5	dB
	MIC1N, MIC1P to PCMO at −31 dBm0 to −45 dBm0	−1		1	
	MIC1N, MIC1P to PCMO at −46 dBm0 to −55 dBm0	−1.2		1.2	

NOTES: 7. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.
8. The reference signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 88-mV_{rms}.

transmit gain and dynamic range, companded mode (μ-law or A-law) or linear mode selected, transmit slope filter enabled (see Notes 7 and 8)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit reference-signal level (0dB)	Differential			175	mV_{pp}
Overload-signal level (3 dBm0)	Differential, normal mode			248	mV_{pp}
	Differential, extended mode			63	mV_{pp}
Absolute gain error	0-dBm0 input signal, V_{DD} = 2.7 V (minimum)	−1		1	dB
Linear mode gain error with input level relative to gain at −10-dBm0 MIC1N, MIC1P to PCMO	MIC1N, MIC1P to PCMO at 3 dBm0 to −30 dBm0	−0.5		0.5	dB
	MIC1N, MIC1P to PCMO at −31 dBm0 to −45 dBm0	−1		1	
	MIC1N, MIC1P to PCMO at −46 dBm0 to −55 dBm0	−1.2		1.2	

NOTES: 7. Unless otherwise noted, the analog input is 0 dB, 1020-Hz sine wave, where 0 dB is defined as the zero-reference point of the channel under test.
8. The reference signal level, which is input to the transmit channel, is defined as a value 3 dB below the full-scale value of 88-mV_{rms}.

transmit filter transfer, linear mode selected, transmit slope filter bypassed, external high pass filter bypassed (MCLK = 2.048 MHz)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain relative to input signal gain at 1020 Hz, internal high-pass filter disabled	f_{MIC1} or f_{MIC2} <100 Hz	−8.5		−6	dB
	f_{MIC1} or f_{MIC2} = 200 Hz	−4.5		−3	
	f_{MIC1} or f_{MIC2} > 700 Hz to 3 kHz	−0.5		0.5	
	f_{MIC1} or f_{MIC2} = 3.4 kHz	−1.5		0	
	f_{MIC1} or f_{MIC2} = 4 kHz			−14	
	f_{MIC1} or f_{MIC2} = 4.6 kHz			−35	
	f_{MIC1} or f_{MIC2} = 8 k Hz			−47	
Gain relative to input signal gain at 1020 Hz, internal high-pass filter enabled	f_{MIC1} or f_{MIC2} <100 Hz			−15	dB
	f_{MIC1} or f_{MIC2} = 200 Hz			−5	

electrical characteristics, V_{DD} = 2.7 V, T_A = −40°C to 105°C (unless otherwise noted) (continued)

transmit filter transfer, linear mode selected, transmit slope filter selected (MCLK = 2.048 MHz) (see Note 9)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain relative to input signal gain at 1000 Hz, with slope filter selected	f_{MIC1} or f_{MIC2} =100 Hz			−27	dB
	f_{MIC1} or f_{MIC2} = 200 Hz			−8	dB
	f_{MIC1} or f_{MIC2} = 250 Hz			−4	dB
	f_{MIC1} or f_{MIC2} = 300 Hz		−1.80		dB
	f_{MIC1} or f_{MIC2} = 400 Hz		−1.50		dB
	f_{MIC1} or f_{MIC2} = 500 Hz		−1.30		dB
	f_{MIC1} or f_{MIC2} = 600 Hz		−1.1		dB
	f_{MIC1} or f_{MIC2} = 700 Hz		−0.8		dB
	f_{MIC1} or f_{MIC2} = 800 Hz		−0.57		dB
	f_{MIC1} or f_{MIC2} = 900 Hz		−0.25		dB
	f_{MIC1} or f_{MIC2} = 1000 Hz		0		dB
	f_{MIC1} or f_{MIC2} = 1500 Hz		1.8		dB
	f_{MIC1} or f_{MIC2} = 2000 Hz		4.0		dB
	f_{MIC1} or f_{MIC2} = 2500 Hz		6.5		dB
	f_{MIC1} or f_{MIC2} = 3000 Hz		7.6		dB
	f_{MIC1} or f_{MIC2} = 3100 Hz		7.7		dB
	f_{MIC1} or f_{MIC2} = 3300 Hz		8.0		dB
	f_{MIC1} or f_{MIC2} = 3500 Hz		6.48		dB
	f_{MIC1} or f_{MIC2} = 4000 Hz			−13	dB
	f_{MIC1} or f_{MIC2} = 4500 Hz			−35	dB
	f_{MIC1} or f_{MIC2} = 5000 Hz			−45	dB
	f_{MIC1} or f_{MIC2} = 8000 Hz			−50	dB

NOTE 9: The pass-band tolerance is ± 0.25 dB from 300 Hz to 3500 Hz.

transmit idle channel noise and distortion, linear mode selected, slope filter bypassed

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit idle channel noise	TXPGA gain = 0 dB, micamp 1 gain = 23.5 dB, micamp 2 gain = 0.0 dB		−86.6	−78	$dBm0_p$
Transmit signal-to-total distortion ratio with 1020-Hz sine-wave input	MIC1N, MIC1P to PCMO at 3 dBm0	40	50		dB
	MIC1N, MIC1P to PCMO at 0 dBm0	50	65		
	MIC1N, MIC1P to PCMO at −5 dBm0	60	68		
	MIC1N, MIC1P to PCMO at −10 dBm0	55	70		
	MIC1N, MIC1P to PCMO at −20 dBm0	58	65		
	MIC1N, MIC1P to PCMO at −30 dBm0	50	60		
	MIC1N, MIC1P to PCMO at −40 dBm0	38	50		
	MIC1N, MIC1P to PCMO at −45 dBm0	30	45		

electrical characteristics, V_{DD} = 2.7 V, T_A = −40°C to 105°C (unless otherwise noted) (continued)

transmit idle channel noise and distortion, linear mode selected, slope filter enabled

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit idle channel noise	TXPGA gain = 0 dB, micamp 1 gain = 23.5 dB, micamp 2 gain = 0.0 dB		−86.6	−78	$dBm0_p$
Transmit signal-to-total distortion ratio with 1020-Hz sine-wave input	MIC1N, MIC1P to PCMO at 3 dBm0	40	50		dB
	MIC1N, MIC1P to PCMO at 0 dBm0	50	65		
	MIC1N, MIC1P to PCMO at −5 dBm0	55	68		
	MIC1N, MIC1P to PCMO at −10 dBm0	55	70		
	MIC1N, MIC1P to PCMO at −20 dBm0	58	65		
	MIC1N, MIC1P to PCMO at −30 dBm0	48	60		
	MIC1N, MIC1P to PCMO at −40 dBm0	38	50		
	MIC1N, MIC1P to PCMO at −45 dBm0	30	45		

receive gain and dynamic range, EAR1 selected, linear or companded (μ-law or A-law) mode selected (see Note 10)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overload-signal level (3.0 dB)	16-Ω load RXPGA = −2.0 dB		3.93		V_{pp}
	32-Ω load RXPGA = −1.0 dB (default gain)		4.41		
Absolute gain error	0-dBm0 input signal, V_{DD} = 2.7 V (minimum)	−1		1	dB
Linear mode gain error with output level relative to gain at −10 dBm0	PCMIN to EAR1ON, EAR1OP at 3 dBm0 to −40 dBm0	−0.5		0.5	dB
	PCMIN to EAR1ON, EAR1OP at −41 dBm0 to −50 dBm0	−1		1	
	PCMIN to EAR1ON, EAR1OP at −51 dBm0 to −55 dBm0	−1.2		1.2	

NOTE 10: RXPGA = -1 dB for 32 Ω default mode or RXPGA = -2 dB for 16 Ω, RXVOL = 0 dB, 1020 Hz input signal at PCMI, output measured differentially between EAR1ON and EAR1OP

receive gain and dynamic range, EAR2 selected, linear or companded (μ-law or A-law) mode selected (see Note 11)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receive reference-signal level (0 dB)	0-dBm0 PCM input signal		1.1		V_{pp}
Overload-signal level (3 dB)			1.6		V_{pp}
Absolute gain error	0-dBm0 input signal, V_{DD} = 2.7 V (minimum)	−1		1	dB
Linear mode gain error with output level relative to gain at −10 dBm0	PCMIN to EAR2O at 3 dBm0 to −40 dBm0	−0.5		0.5	dB
	PCMIN to EAR2O at −41 dBm0 to −50 dBm0	−1		1	
	PCMIN to EAR2O at −51 dBm0 to −55 dBm0	−1.2		1.2	

NOTE 11: RXPGA = -1 dB, RXVOL = 0 dB

electrical characteristics, V_{DD} = 2.7 V, T_A = −40°C to 105°C (unless otherwise noted) (continued)

receive filter transfer, linear mode selected (MCLK = 2.048 MHz) (see Note 11)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain relative to input signal gain at 1020 Hz, internal high-pass filter disabled	f_{EAR1} or f_{EAR2} < 100 Hz	−0.5		0.5	dB
	f_{EAR1} or f_{EAR2} = 200 Hz	−0.5		0.5	
	f_{EAR1} or f_{EAR2} = 300 Hz to 3 kHz	−0.5		0.5	
	f_{EAR1} or f_{EAR2} = 3.4 kHz	−1.5		0	
	f_{EAR1} or f_{EAR2} = 4 kHz			−14	
	f_{EAR1} or f_{EAR2} = 4.6 kHz			−35	
	f_{EAR1} or f_{EAR2} = 8 kHz			−47	
Gain relative to input signal gain at 1020 Hz, internal high-pass filter enabled	f_{EAR1} or f_{EAR2} < 100 Hz			−15	dB
	f_{EAR1} or f_{EAR2} = 200 Hz			−5	

NOTE 11: RXPGA = -1 dB, RXVOL = 0 dB

receive idle channel noise and distortion, EAR1 selected, linear mode selected (see Note 12)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receive noise, (20 Hz to 20 kHz brickwall window)	PCMIN = 0000000000000		−86	−83	dBm0
Receive signal-to-distortion ratio with 1020 Hz sine-wave input	PCMIN to EAR1ON, EAR1OP at 3 dBm0	65	78		dB
	PCMIN to EAR1ON, EAR1OP at 0 dBm0	73	80		
	PCMIN to EAR1ON, EAR1OP at −5 dBm0	72	78		
	PCMIN to EAR1ON, EAR1OP at −10 dBm0	70	78		
	PCMIN to EAR1ON, EAR1OP at −20 dBm0	60	76		
	PCMIN to EAR1ON, EAR1OP at −30 dBm0	50	67		
	PCMIN to EAR1ON, EAR1OP at −40 dBm0	40	60		
	PCMIN to EAR1ON, EAR1OP at −45 dBm0	33	55		
Intermodulation distortion, 2-tone CCITT method, composite power level, −13 dBm0	CCITT G.712 (7.1), R2	50			dB
	CCITT G.712 (7.2), R2	54			

NOTE 12: RXPGA = -1 dB for 32 Ω default mode or RXPGA = -2 dB for 16 Ω, RXVOL = 0 dB, 1020 Hz input signal at PCMI, output measured differentially between EAR1ON and EAR1OP.

receive idle channel noise and distortion, EAR2 selected, linear mode selected (see Note 11)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receive noise, (20 Hz to 20 kHz brickwall window)	PCMIN = 0000000000000		−86	−82	dBm0
Receive signal-to-distortion ratio with 1020-Hz sine-wave input	PCMIN to EAR2O at 3 dBm0	45	60		dB
	PCMIN to EAR2O at 0 dBm0	60	65		
	PCMIN to EAR2O at −5 dBm0	58	62		
	PCMIN to EAR2O at −10 dBm0	55	60		
	PCMIN to EAR2O at −20 dBm0	53	60		
	PCMIN to EAR2O at −30 dBm0	52	58		
	PCMIN to EAR2O at −40 dBm0	44	57		
	PCMIN to EAR2O at −45 dBm0	33	52		
Intermodulation distortion, 2-tone CCITT method, composite power level, −13 dBm0	CCITT G.712 (7.1), R2	50			dB
	CCITT G.712 (7.2), R2	54			

NOTE 11: RXPGA = -1 dB, RXVOL = 0 dB

electrical characteristics, V_{DD} = 2.7 V, T_A = −40°C to 105°C (unless otherwise noted) (continued)

power supply rejection and crosstalk attenuation

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage rejection, transmit channel	MIC1N, MIC1P =0 V, V_{DD} = 2.7 V + 100 $mV_{peak\ to\ peak}$, f = 0 to 50 kHz		−80	−45	dB
Supply voltage rejection, receive channel, EAR1 selected (differential)	PCM code = positive zero, V_{DD} = 2.7 V + 100 $mV_{peak\ to\ peak}$, f = 0 to 50 kHz		−90	−45	dB
Crosstalk attenuation, transmit-to-receive (differential)	MIC1N, MIC1P = 0 dB, f = 300 to 3400 Hz measured differentially between EAR1ON and EAR1OP	70			dB
Crosstalk attenuation, receive-to-transmit	PCMIN = 0 dBm0, f = 300 to 3400 Hz measured at PCMO, EAR1 amplifier	70			dB

DTMF generator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DTMF high to low tone relative amplitude (preemphasis)		1.5	2	2.5	dB

MICBIAS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Load impedance		2.0		2.5	kΩ

timing requirements

clock

		MIN	NOM	MAX	UNIT
t_t	Transition time, MCLK			10	ns
	MCLK frequency	2.048		2.048	MHz
	MCLK jitter			37%	
	Number of PCMCLK clock cycles per PCMSYN frame	256		256	
$t_{c(PCMCLK)}$	PCMCLK clock period	156	488	512	ns
	Duty cycle, PCMCLK	45%	50%	68%	

transmit (see Figure 6)

		MIN	MAX	UNIT
$t_{su(PCMSYN)}$	Setup time, PCMSYN high before PCMCLK↓	20	$t_{c(PCMCLK)}$−20	ns
$t_{h(PCMSYN)}$	Hold time, PCMSYN high after PCMCLK↓	20	$t_{c(PCMCLK)}$−20	

receive (see Figure 5)

		MIN	MAX	UNIT
$t_{su(PCSYN)}$	Setup time, PCMSYN high before PCMCLK↓	20	$t_{c(PCMCLK)}$−20	ns
$t_{h(PCSYN)}$	Hold time, PCMSYN high after PCMCLK↓	20	$t_{c(PCMCLK)}$−20	ns
$t_{su(PCMI)}$	Setup time, PCMI high or low before PCMCLK↓	20		ns
$t_{h(PCMI)}$	Hold time, PCMI high or low after PCMCLK↓	20		ns

timing requirements (continued)

I²C bus (see Figure 6)

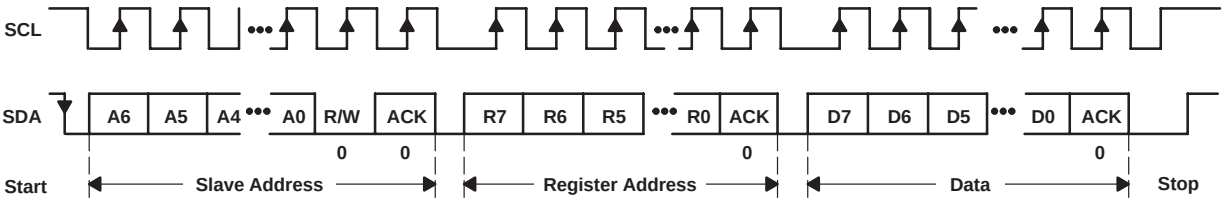
		MIN	MAX	UNIT
SCL	Clock frequency		400	kHz
t_{HIGH}	Clock high time	600		ns
t_{LOW}	Clock low time	1300		ns
t_R	SDA and SCL rise time		300	ns
t_F	SDA and SCL fall time		300	ns
$t_{hD:STA}$	Hold time (repeated) START condition. After this period the first clock pulse is generated.	600		ns
$t_{su:STA}$	Setup time for repeated START condition	600		ns
$t_{hD:DAT}$	Data input hold time	0		ns
$t_{su:DAT}$	Data input setup time	100		ns
$t_{su:STO}$	STOP condition setup time	600		ns
t_{BUF}	Bus free time	1300		ns

switching characteristics

propagation delay times, C_{Lmax} = 10 pF (see Figure 5)

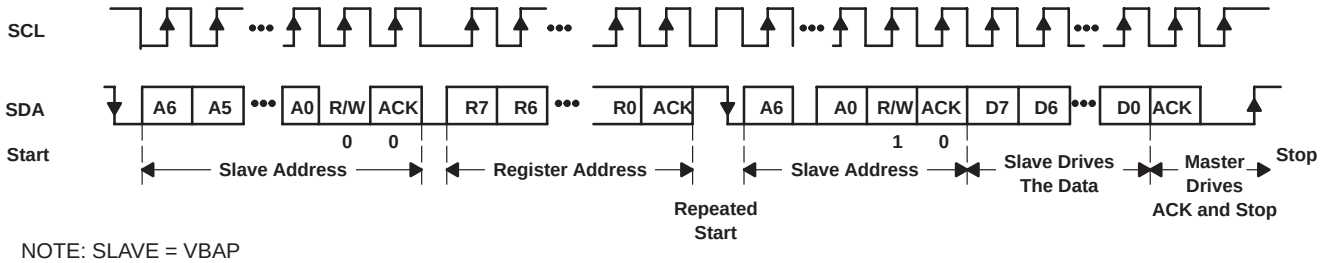
		MIN	MAX	UNIT
t_{pd1}	From PCMCLK bit 1 high to PCMO bit 1 valid		35	ns
t_{pd2}	From PCMCLK high to PCMO valid, bits 2 to n		35	ns
t_{pd3}	From PCMCLK bit n low to PCMO bit n Hi-Z	30		ns

PARAMETER MEASUREMENT INFORMATION



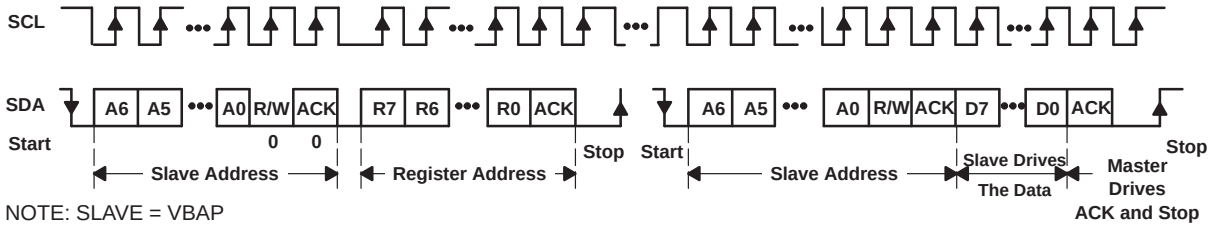
NOTE: SLAVE = VBAP

Figure 1. I²C Bus Write to VBAP



NOTE: SLAVE = VBAP

Figure 2. I²C Read From VBAP: Protocol A



NOTE: SLAVE = VBAP

Figure 3. I²C Read From VBAP: Protocol B

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PARAMETER MEASUREMENT INFORMATION

register map addressing

	REG	07	06	05	04	03	02	01	00
Power control	00	Sidetone En	TXEn	RXEn	MICSEL	BIASEn	RXEn	EAROUT Sel	PWRUP
Mode control	01	Comp Sel	TMEn	PCMLB	Comp En	BUZZEn	RXFLTR En	TXFLTR En	TXSLOPE En
TXPGA	02	PD0	TP3	TP2	TP1	TP0	ST2	ST1	ST0
RXPGA	03	RP3	RP2	RP1	RP0	RV3	RV2	RV1	RV0
High DTMF	04	HIFREQ Sel7	HIFREQ Sel6	HIFREQ Sel5	HIFREQ Sel4	HIFREQ Sel3	HIFREQ Sel2	HIFREQ Sel1	HIFREQ Sel0
Low DTMF	05	LOFREQ Sel7	LOFREQ Sel6	LOFREQ Sel5	LOFREQ Sel4	LOFREQ Sel3	LOFREQ Sel2	LOFREQ Sel1	LOFREQ Sel0

register power-up defaults

	REG	07	06	05	04	03	02	01	00
Power control†	00	1	1	1	1	0	1	1	0
Power control‡	00	1	0	0	1	1	0	1	1
Mode control	01	0	0	0	0	0	0	1	0
TXPGA	02	0	1	0	0	0	0	0	0
RXPGA	03	0	1	1	1	0	0	0	0
High DTMF	04	0	0	0	0	0	0	0	0
Low DTMF	05	0	0	0	0	0	0	0	0

† Value when PWRUPSEL = 0
‡ Value when PWRUPSEL = 1

PARAMETER MEASUREMENT INFORMATION

register map

Table 1. Power Control Register: Address {00} HEX

BIT NUMBER								DEFINITIONS
7	6	5	4	3	2	1	0	
1	1	1	1	0	1	1	0	Default setting PWRUPSEL = 0
1	0	0	1	1	0	1	1	Default setting PWRUPSEL = 1
X	X	X	X	X	X	X	0	Reference system, power down
X	X	X	X	X	X	X	1	Reference system, power up
X	X	X	X	X	X	1	X	EAR AMP1 selected, EAR AMP2 power down
X	X	X	X	X	X	0	X	EAR AMP2 selected, EAR AMP1 power down
X	X	X	X	X	0	X	X	Receive channel enabled
X	X	0	X	X	1	X	X	Receive channel muted
X	X	1	X	X	1	X	0	Receive channel, power down
X	X	X	X	1	X	X	X	MICBIAS selected
X	X	X	X	0	X	X	X	MICBIAS power down
X	X	X	1	X	X	X	X	MIC1 selected
X	X	X	0	X	X	X	X	MIC2 selected
X	0	X	X	X	X	X	X	Transmit channel enabled
X	1	0	X	X	X	X	X	Transmit channel muted
X	1	1	X	X	X	X	X	Transmit channel power down
0	X	X	X	X	X	X	X	Sidetone enabled
1	X	X	X	X	X	X	X	Sidetone muted

Table 2. Mode Control Register: Address {01} HEX

BIT NUMBER								DEFINITIONS
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	1	0	Default setting
X	X	X	X	X	X	0	0	TX channel high-pass filter enabled and slope filter enabled
X	X	X	X	X	X	0	1	TX channel high-pass filter enabled and slope filter disabled
X	X	X	X	X	X	1	0	TX channel high-pass filter disabled and slope filter enabled
X	X	X	X	X	X	1	1	TX channel high-pass filter disabled and slope filter disabled
X	X	X	X	X	0	X	X	RX channel high-pass filter disabled (low pass only)
X	X	X	X	X	1	X	X	RX channel high-pass filter enabled
X	X	X	X	0	X	X	X	BUZZCON disabled
X	X	X	X	1	X	X	X	BUZZCON enabled
X	X	X	0	X	X	X	X	Linear mode selected
1	X	X	1	X	X	X	X	A-law companding mode selected
0	X	X	1	X	X	X	X	μ-law companding mode selected
X	X	0	X	X	X	X	X	TX and RX channels normal mode
X	X	1	X	X	X	X	X	PCM loopback mode
X	0	X	X	X	X	X	X	Tone mode disabled
X	1	X	X	X	X	X	X	Tone mode enabled

PARAMETER MEASUREMENT INFORMATION

Transmit PGA and sidetone control register: Address {02}HEX

Bit definitions:

7	6	5	4	3	2	1	0	DEFINITION
PDO	TP3	TP2	TP1	TP0	ST2	ST1	ST0	See Table 2 and Table 4
0	1	0	0	0	0	0	0	Default setting

Receive volume control register: Address {03}HEX

Bit definitions :

7	6	5	4	3	2	1	0	DEFINITION
RP3	RP2	RP1	RP0	RV3	RV2	RV1	RV0	See Table 3 and Table 5
0	1	1	1	0	0	0	0	Default setting

High tone selection control register: Address {04}HEX

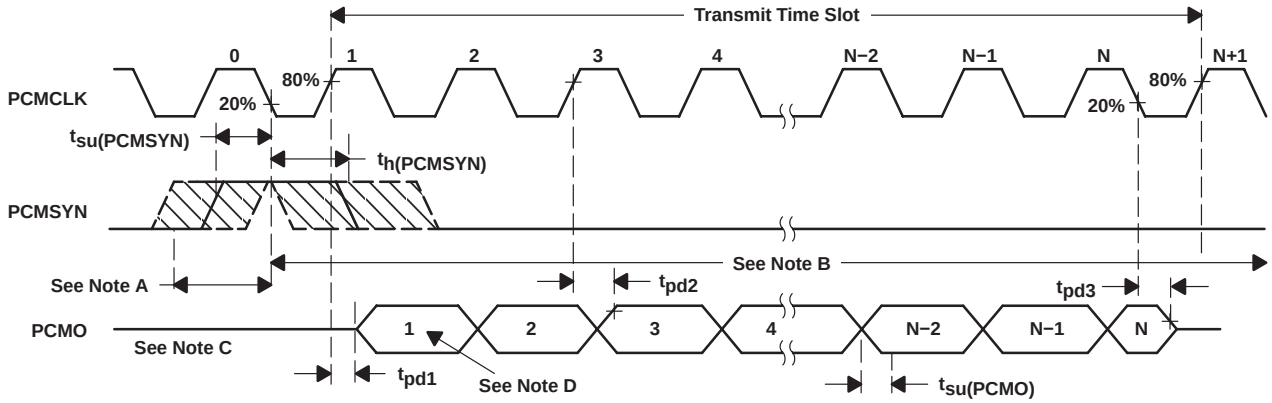
Bit definitions:

7	6	5	4	3	2	1	0	DEFINITION
X	X	X	X	X	X	X	X	DTMF (see Table 7)
0	0	0	0	0	0	0	0	Default setting

Low tone selection control register: Address {05}HEX

Bit definitions:

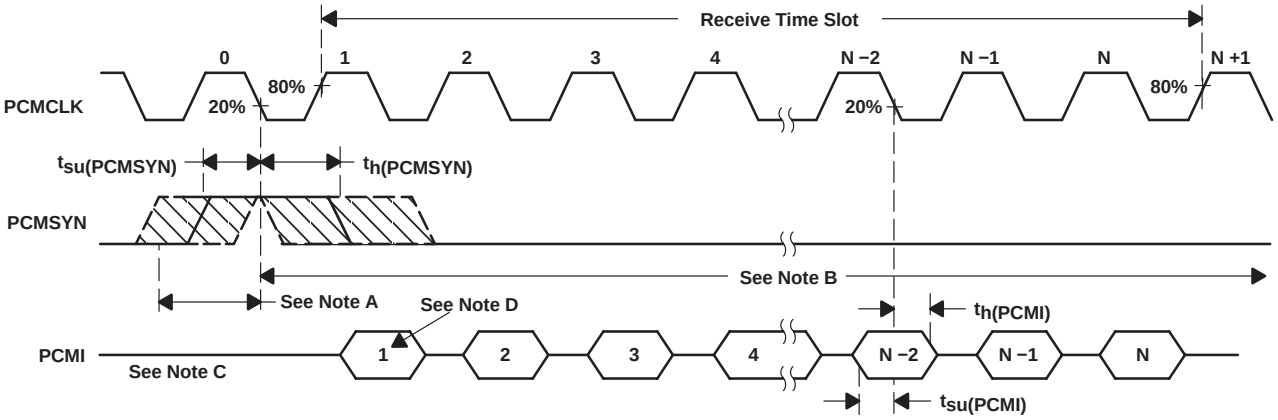
7	6	5	4	3	2	1	0	DEFINITION
X	X	X	X	X	X	X	X	DTMF (see Table 7)
0	0	0	0	0	0	0	0	Default setting



NOTES: A. This window is allowed for PCMSYN high.
B. This window is allowed for PCMSYN low ($t_{h(PCMSYN)}$max determined by data collision considerations).
C. Transitions are measured at 50%.
D. Bit 1 = MSB, Bit N = LSB

Figure 4. Transmit Timing Diagram

PARAMETER MEASUREMENT INFORMATION



A. This window is allowed for PCMSYN high.
B. This window is allowed for PCMSYN low.
C. Transitions are measured at 50%.
D. Bit 1 = MSB, Bit N = LSB

Figure 5. Receive Timing Diagram

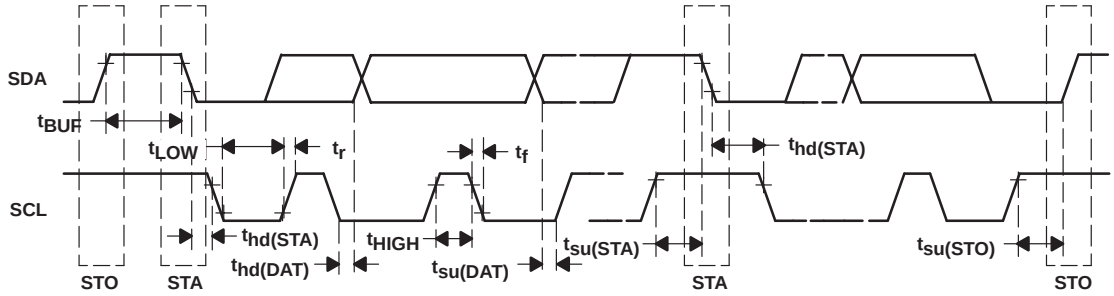


Figure 6. I²C Bus Timing Diagram

PRINCIPLES OF OPERATION

power-on initialization

An external reset with a minimum pulse width of 500 ns must be applied to the active low $\overline{\text{RESET}}$ terminal to guarantee reset upon power on. All registers are set with default values upon external reset initialization.

The desired selection for all programmable functions can be initialized prior to a power-up command using the I^2C interface.

Table 3. Power-Up and Power-Down Procedures (V_{DD} = 2.7 V, Earphone amplifier unloaded)

DEVICE STATUS	PROCEDURE	MAXIMUM POWER CONSUMPTION
Power up	Set bit 1 = 1 in power control register, EAR1 enabled	16.2 mW
	Set bit 1 = 0 in power control register, EAR2 enabled	14.6 mW
Power down	Set bit 7 = 1 in TXPGA control register and bit 0 = 0	1.35 μW
	Set bit 7 = 0 in TXPGA control register and bit 0 = 0	67.5 μW

In addition to resetting the power-down bit in the power control register, loss of MCLK (no transition detected) automatically enters the device into a power-down state with PCMO in the high impedance state. If during a pulse code modulation (PCM) data transmit cycle an asynchronous power down occurs, the PCM interface remains powered up until the PCM data is completely transferred.

An additional power-down mode overrides the MCLK detection function. This allows the device to enter the power-down state without regard to MCLK. Setting bit 7 of the TX filter and PGA sidetone register to logic high enables this function.

conversion laws

The device can be programmed either for a 15-bit linear or 8-bit (μ-law or A-law) companding mode. The companding operation approximates the CCITT G.711 recommendation. The linear mode operation uses a 15-bit twos-complement format.

transmit operation

microphone input

The microphone input stage is a low noise differential amplifier that provides a preamplifier gain of 23.5 dB. A microphone can be capacitively connected to the MIC1N and MIC1P inputs, while the MIC2N and MIC2P inputs can be used to capacitively connect a second microphone or an auxiliary audio circuit.

PRINCIPLES OF OPERATION

transmit operation (continued)

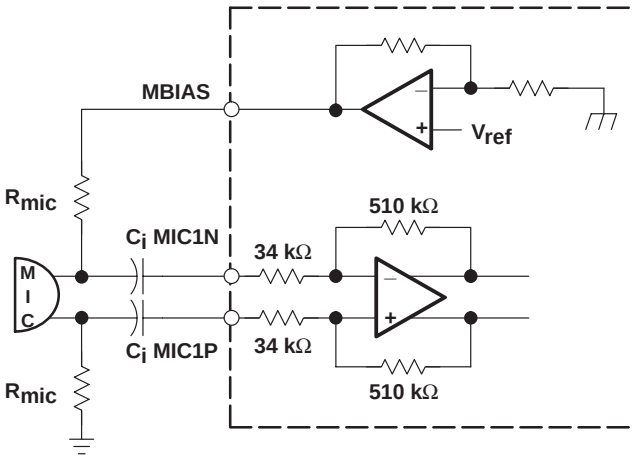


Figure 7. Typical Microphone Interface

microphone mute function

Transmit channel muting provides 80-dB attenuation of input microphone signal. The MICMUTE function can be selected by setting bit 6 of the power control register through the I^2C interface.

transmit channel gain control

The values in the transmit PGA control registers control the gain in the transmit path. The total TX channel gain can vary from 35.5 dB to 13.5 dB. The default total TX channel gain is 23.5 dB

Table 4. Transmit Gain Control

BIT NAME				MIC AMP1	MIC AMP2	TX PGA	GAIN MODE	TOTAL TX GAIN			
TP3	TP2	TP1	TP0	GAIN	GAIN	GAIN		MIN	TYP	MAX	UNIT
0	0	0	0	23.5	12	0	Extended	35.3	35.5	35.7	dB
0	0	0	1	23.5	12	−2	Extended	33.3	33.5	33.7	dB
0	0	1	0	23.5	12	−4	Extended	31.3	31.5	31.7	dB
0	0	1	1	23.5	12	−6	Extended	29.3	29.5	29.7	dB
0	1	0	0	23.5	12	−8	Extended	27.3	27.5	27.7	dB
0	1	0	1	23.5	12	−10	Extended	25.3	25.5	25.7	dB
1	0	0	0	23.5	0	0	Normal	23.3	23.5	23.7	dB
1	0	0	1	23.5	0	−2	Normal	21.3	21.5	21.7	dB
1	0	1	0	23.5	0	−4	Normal	19.3	19.5	19.7	dB
1	0	1	1	23.5	0	−6	Normal	17.3	17.5	17.7	dB
1	1	0	0	23.5	0	−8	Normal	15.3	17.5	17.7	dB
1	1	0	1	23.5	0	−10	Normal	13.3	13.5	13.7	dB

PRINCIPLES OF OPERATION

receive operation

receive channel gain control

The values in the receive PGA control registers control the gain in the receive path. PGA gain is set from −6 dB to 6 dB in 1-dB steps through the I^2C interface. The default receive channel gain is −1 dB.

Table 5. Receive PGA Gain Control

BIT NAME				RELATIVE GAIN			
RP3	RP2	RP1	RP0	MIN	TYP	MAX	UNIT
0	0	0	0	5.8	6	6.2	dB
0	0	0	1	4.8	5	5.2	dB
0	0	1	0	3.8	4	4.2	dB
0	0	1	1	2.8	3	3.2	dB
0	1	0	0	1.8	2	2.2	dB
0	1	0	1	0.8	1	1.2	dB
0	1	1	0	−0.2	0	0.2	dB
0	1	1	1	−1.2	−1	−0.8	dB
1	0	0	0	−2.2	−2	−1.8	dB
1	0	0	1	−3.2	−3	−2.8	dB
1	0	1	0	−4.2	−4	−3.8	dB
1	0	1	1	−5.2	−5	−4.8	dB
1	1	0	0	−6.2	−6	−5.8	dB

sidetone gain control

The values in the sidetone PGA control registers control the sidetone gain. Sidetone gain is set from −12 dB to −24 dB in 2-dB steps through the I^2C interface. Sidetone can be muted by setting bit 7 of the power control register. The default sidetone gain is −12 dB.

Table 6. Sidetone Gain Control

BIT NAME			RELATIVE GAIN			
ST2	ST1	ST0	MIN	TYP	MAX	UNIT
0	0	0	−12.2	−12	−11.8	dB
0	0	1	−14.2	−14	−13.8	dB
0	1	0	−16.2	−16	−15.8	dB
0	1	1	−18.2	−18	−17.8	dB
1	0	0	−20.2	−20	−19.8	dB
1	0	1	−22.2	−22	−21.8	dB
1	1	0	−24.2	−24	−23.8	dB

PRINCIPLES OF OPERATION

receive operation (continued)

receive volume control

The values in the volume control PGA control registers provide volume control into the earphone. Volume control gain is set from 0 dB to −18 dB in 2-dB steps through the I^2C interface. The default RX volume control gain is 0 dB.

Table 7. rx Volume Control

BIT NAME				RELATIVE GAIN			
RV3	RV2	RV1	RV0	MIN	TYP	MAX	UNIT
0	0	0	0	−0.2	0	0.2	dB
0	0	0	1	−2.2	−2	−1.8	dB
0	0	1	0	−4.2	−4	−3.8	dB
0	0	1	1	−6.2	−6	−5.8	dB
0	1	0	0	−8.2	−8	−7.8	dB
0	1	0	1	−10.2	−10	−9.8	dB
0	1	1	0	−12.2	−12	−11.8	dB
0	1	1	1	−14.2	−14	−13.8	dB
1	0	0	0	−16.2	−16	−15.8	dB
1	0	0	1	−18.2	−18	−17.8	dB

earphone amplifier

The analog signal can be routed to one of two earphone amplifiers: one with differential output (EAR1ON and EAR1OP) capable of driving a 16-Ω load or one with single-ended output (EAR2O) capable of driving a 32-Ω load.

earphone mute function

Muting can be selected by setting bit 3 of the power control register through the I^2C interface.

receive PCM data format

- Companded mode: eight bits are received, the most significant (MSB) first.
- Linear mode: 15 bits are received, MSB first.

PRINCIPLES OF OPERATION

receive operation (continued)

Table 8. Receive-Data Bit Definitions

BIT NO.	COMPANDED MODE	LINEAR MODE
1	CD7	LD14
2	CD6	LD13
3	CD5	LD12
4	CD4	LD11
5	CD3	LD10
6	CD2	LD9
7	CD1	LD8
8	CD0	LD7
9	−	LD6
10	−	LD5
11	−	LD4
12	−	LD3
13	−	LD2
14	−	LD1
15	−	LD0
16	−	−−

Transmit channel gain control bits always follow the PCM data in time:

CD7−CD0 = data word in companded mode

LD14−LD0 = data word in linear mode

DTMF generator operation and interface

The dual-tone multifrequency generator (DTMF) circuit generates the summed DTMF tones for push button dialing and provides the PDM output for the BUZZCON user-alert tone. There are 255 possible single tones. The tone integer value is determined by the formula:

Round (tone frequency (Hz)/7.8125 Hz)

The integer value is loaded into either one of two 8-bit registers, high-tone register (04), or low-tone register (05). The tone output is 2 dB higher when applied to the high-tone register (04). When generating DTMF tones, the high frequency value must be applied to the high-tone register (04) and the low DTMF value to the low-tone register.

PRINCIPLES OF OPERATION

DTMF generator operation and interface (continued)

Table 9. Typical DTMF and Single Tone Control

DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0	INTEGER VALUE	TONE FUNCTION	TONE/Hz
0	0	0	0	0	0	0	0	0	OFF	0
0	0	1	0	1	1	0	1	45	F	349
0	0	1	0	1	1	1	1	47	F#	370
0	0	1	1	0	0	1	0	50	G	392
0	0	1	1	0	1	0	1	53	G#	415
0	0	1	1	1	0	0	0	56	A	440
0	0	1	1	1	1	0	0	60	A#	466
0	0	1	1	1	1	1	1	63	B	494
0	1	0	0	0	0	1	1	67	C	523
0	1	0	0	0	1	1	1	71	C#	554
0	1	0	0	1	0	1	1	75	D	587
0	1	0	1	0	0	0	0	80	D#	622
0	1	0	1	0	1	0	0	84	E	659
0	1	0	1	1	0	0	1	89	F	698
0	1	0	1	1	1	1	1	95	F#	740
0	1	1	0	0	1	0	0	100	G	784
0	1	1	0	1	0	1	0	106	G#	831
0	1	1	1	0	0	0	1	113	A	880
0	1	1	1	0	1	1	1	119	A#	932
0	1	1	1	1	1	1	0	126	B	988
1	0	0	0	0	1	1	0	134	C	1047
1	0	0	0	1	1	1	0	142	C#	1109
1	0	0	1	0	1	1	0	150	D	1175
1	0	0	1	1	1	1	1	159	D#	1245
1	0	1	0	1	0	0	1	169	E	1319
1	0	1	1	0	0	1	1	179	F	1397
1	0	1	1	1	1	0	1	189	F#	1480
1	1	0	0	1	0	0	1	201	G	1568
1	1	0	1	0	1	0	1	213	G#	1661
1	1	1	0	0	0	0	1	225	A	1760
1	1	1	0	1	1	1	1	239	A#	1865
1	1	1	1	1	1	0	1	253	B	1976
0	1	0	1	1	0	0	1	89	DTMF Low	697
0	1	1	0	0	0	1	1	99	DTMF Low	770
0	1	1	0	1	1	0	1	109	DTMF Low	852
0	1	1	1	1	0	0	0	120	DTMF Low	941
1	0	0	1	1	0	1	1	155	DTMF HIgh	1209
1	0	1	0	1	0	1	1	171	DTMF HIgh	1336
1	0	1	1	1	1	0	1	189	DTMF HIgh	1477
1	1	0	1	0	0	0	1	209	DTMF HIgh	1633

PRINCIPLES OF OPERATION

DTMF generator operation and interface (continued)

Tones from the DTMF generator block are present at all outputs and are controlled by enabling or disabling the individual output ports. The values that determine the tone frequency are loaded into the tone registers (high and lo) as two separate values.

The values loaded into the tone registers initiate an iterative table look-up function, placing a 6-bit or 7-bit in twos complement value into the the tone registers. There is a 2 dB difference in the resulting output of the two registers, the high-tone register having the greater result.

The resulting range of a tone set into the low register value is +31 {1F}HEX to −32 {20}HEX for a range of six bits and is in twos complement format. The resulting range of a tone set into the high register value is +39 {27}HEX to −40 {D8}HEX in twos-complement format, as well.

The maximum range is six bits having a maximum value of {31}HEX. The value {31} is represented as 011111. Two zeros are added to the leading side of the value and then the value is padded with seven LSB zeros to create a value of 000 1111 1000 0000. Because the maximum full scale value is 000 1111 1000 0000, the resulting output magnitude is 20 log (input value/maximum value) or 20 log (3968/16783) or −12.31 dB below full scale. This is the result when all gains are set at default.

buzzer logic section

The single-ended output BUZZCON is a PDM signal intended to drive a buzzer through an external driver transistor. The PDM begins as a selected tone, is generated and passed through the receive D/A channel, and is fed back to the transmit channel analog modulator, where a PDM signal is generated and routed to the BUZZCON output.

support section

The clock generator and control circuit uses the master clock input (MCLK) to generate internal clocks to drive internal counters, filters, and converters. Register control data is written into and read back from the VBAP registers via the control interface.

I^2C-bus protocols

The VBAP serial interface is designed to be I^2C bus-compatible and operates in the slave mode. This interface consists of the following terminals:

SCL: I^2C bus serial clock—This input synchronizes the control data transfer from and to the CODEC.

SDA: I^2C bus serial address/data input/output—This is a bidirectional terminal that transfers register control addresses and data into and out of the codec. It is an open drain terminal and therefore requires a pullup resistor to V_{CC} (typical 10 kΩ for 100 kHz).

TWL1103 has a fixed device select address of {E2}HEX for write mode and {E3}HEX for read mode.

For normal data transfer, SDA is allowed to change only when SCL is low. Changes when SCL is high are reserved for indicating the start and stop conditions.

Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is at high. Changes in the data line while the clock line is at high are interpreted as a start or stop condition.

PRINCIPLES OF OPERATION

Table 10. I²C Bus Conditions

CONDITION	STATUS	DESCRIPTION
A	Bus not busy	Both data and clock lines remain at high.
B	Start data transfer	A high to low transition of the SDA line while the clock (SCL) is high determines a start condition. All commands must proceed from a start condition.
C	Stop data transfer	A low to high transition of the SDA line while the clock (SCL) is high determines a stop condition. All operations must end with a stop condition.
D	Data valid	The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the high period of the clock signal.

I²C bus protocols

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition.

When addressed, the VBAP generates an acknowledge after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with this acknowledge bit.

The VBAP must pull down the SDA line during the acknowledge clock pulse so that the SDA line is at stable low state during the high period of the acknowledge related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave (VBAP) must leave the data line high to enable the master to generate the stop condition.

clock frequencies and sample rates

A fixed PCMSYN rate of 8 kHz determines the sampling rate.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TWL1103TPBSQ1	ACTIVE	TQFP	PBS	32	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TWL1103T	Samples
TWL1103TPBSRQ1	ACTIVE	TQFP	PBS	32	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TWL1103T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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