InnoSwitch3-TN Family

High Efficiency Off-line CV/CC QR Flyback Switcher IC with Integrated 725 V Primary MOSFET, Synchronous Rectification and Integrated Secondary-Side Control

Product Highlights

Ideal for Isolated and Non-Isolated Applications

- Flybacks with positive and negative output rails
- Incorporates a multi-mode Quasi Resonant (QR) / CCM flyback controller, 725 V primary MOSFET, secondary voltage and current sensing, SR driver
- Integrated FluxLink™ feedback
- Compact package reduces PCB area
- High efficiency across load range
- Accurate CV/CC independent of transformer design or external components
- Easily meets 20% regulation limit on 5 V output during zero load to full-load transients

EcoSmart™ – Energy Efficient

- Less than 5 mW no-load at 230 VAC
- Enables designs that easily meet global energy efficiency regulations
- Achieves up to 90% full load efficiency

Advanced Protection / Safety Features

- Integrated output OVP
- Open-gate detection for SR FET
- Hysteretic thermal shutdown
- Overload power limited <15 W (5 V and <3 A)
  - Using accurate internal CC (constant-current) limit

Full Safety and Regulatory Compliance

- Reinforced insulation with isolation voltage >4000 VAC
  - 100% production Hipot testing
- UL1577 isolation voltage 4000 VAC (max), TUV (EN62368-1), CQC (GB4943.1) safety approved. VDE 0884-17 (EN60747-17) pending approval
- Enables designs that have "class A" performance criteria for EN61000-4 suite of test standards, including EN61000-4-2, 4-3 (30 V/m), 4-4, 4-5, 4-6, 4-8 (100 A/m) and 4-9 (1000 A/m)

Green Package

- Halogen free and RoHS compliant

Applications

- Auxiliary supplies in appliances and industrial systems

Description

The InnoSwitch™3-TN family dramatically increases the efficiency of auxiliary power supplies used in appliances, consumer products and industrial applications. Ideal for both isolated and non-isolated designs, this advanced flyback controller can achieve up to 90% full load efficiency, flat efficiency across the load range and very low no-load consumption. The InnoSwitch3-TN may be used as an accurate 5 V single-output power supply, with two positive rails or with both positive and negative rails.

The 725 V primary MOSFET, primary and secondary flyback controllers are coupled using the proprietary FluxLink communications channel. Safety-rated FluxLink communication ensures reliable synchronous rectification and accurate output CV and CC. Comprehensive safety features include output over-current protection and over-temperature protection. The small MinSOP package and a low number of external components make the InnoSwitch3-TN ICs ideal for compact designs.

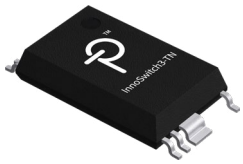


Figure 2. Compact MinSOP-16A M Package.

Maximum Output Power Table

Product[4]	230 VAC	85-265 VAC
	Open Frame[1,2,3]	**Open Frame[1,2,3]**
INN3072M	12 W	10 W
INN3073M	15 W	12 W
INN3074M	21 W	16 W

Table 1. Output Power Table.

Notes:
1. Minimum peak power capability.
2. Max output power is dependent on the design. Limit package temperature to <125 ºC.
3. Assumes internal output current sensing is disabled (IS-GND pins shorted)
4. Package: MinSOP-16A.

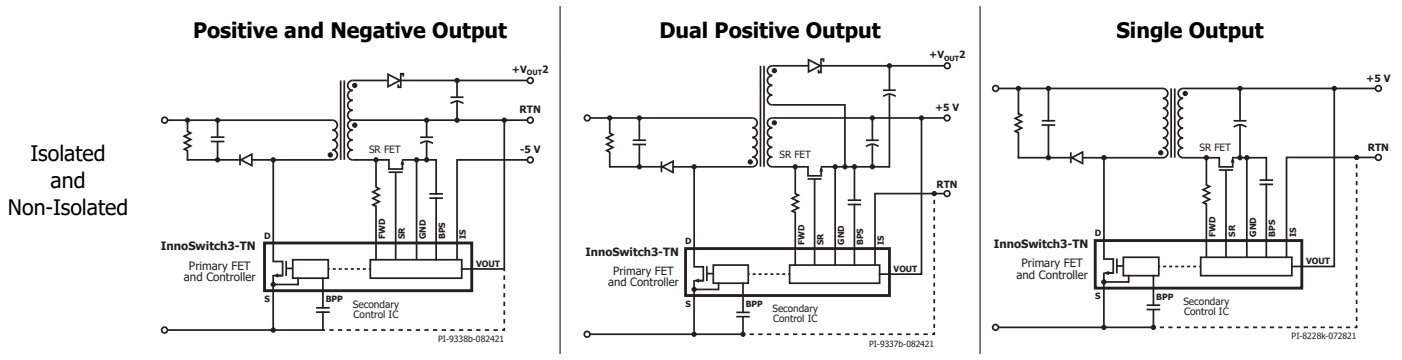


Figure 1. Power Supply Configuration Examples using InnoSwitch3-TN.

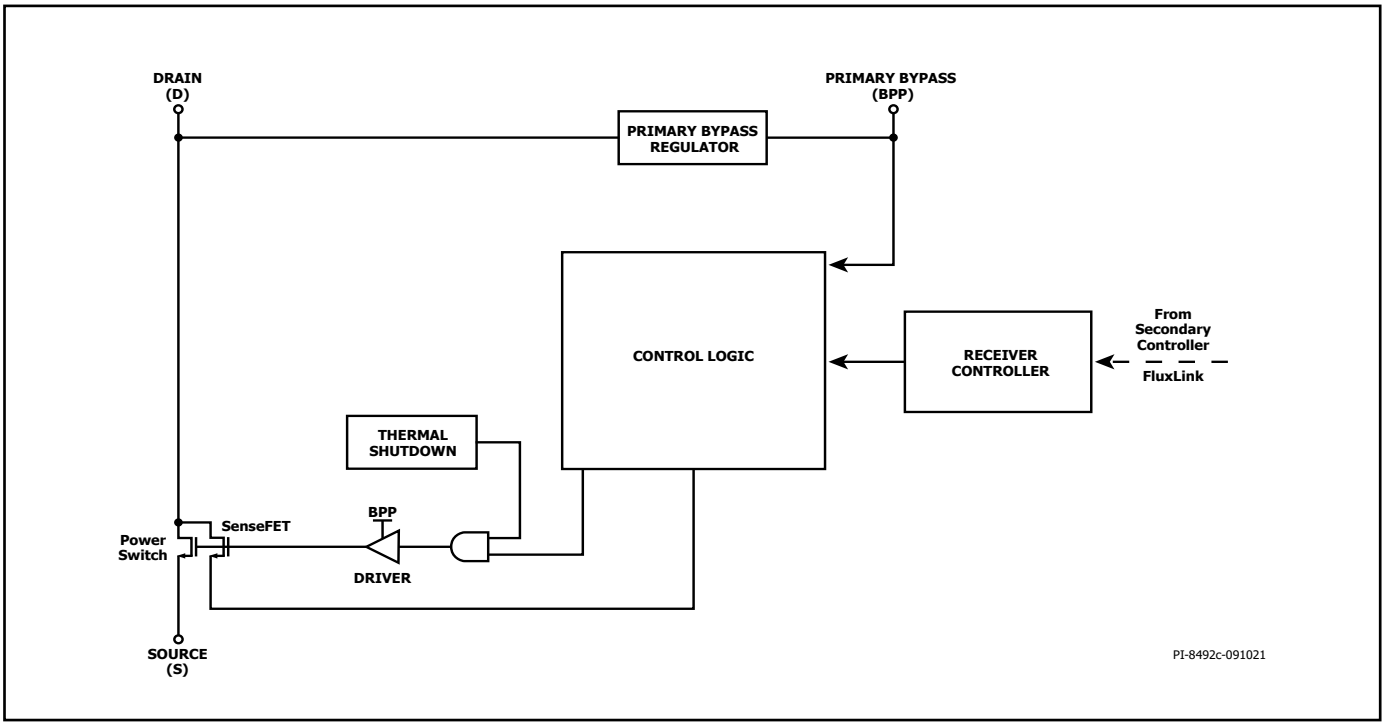


Figure 3. Primary Controller Block Diagram.

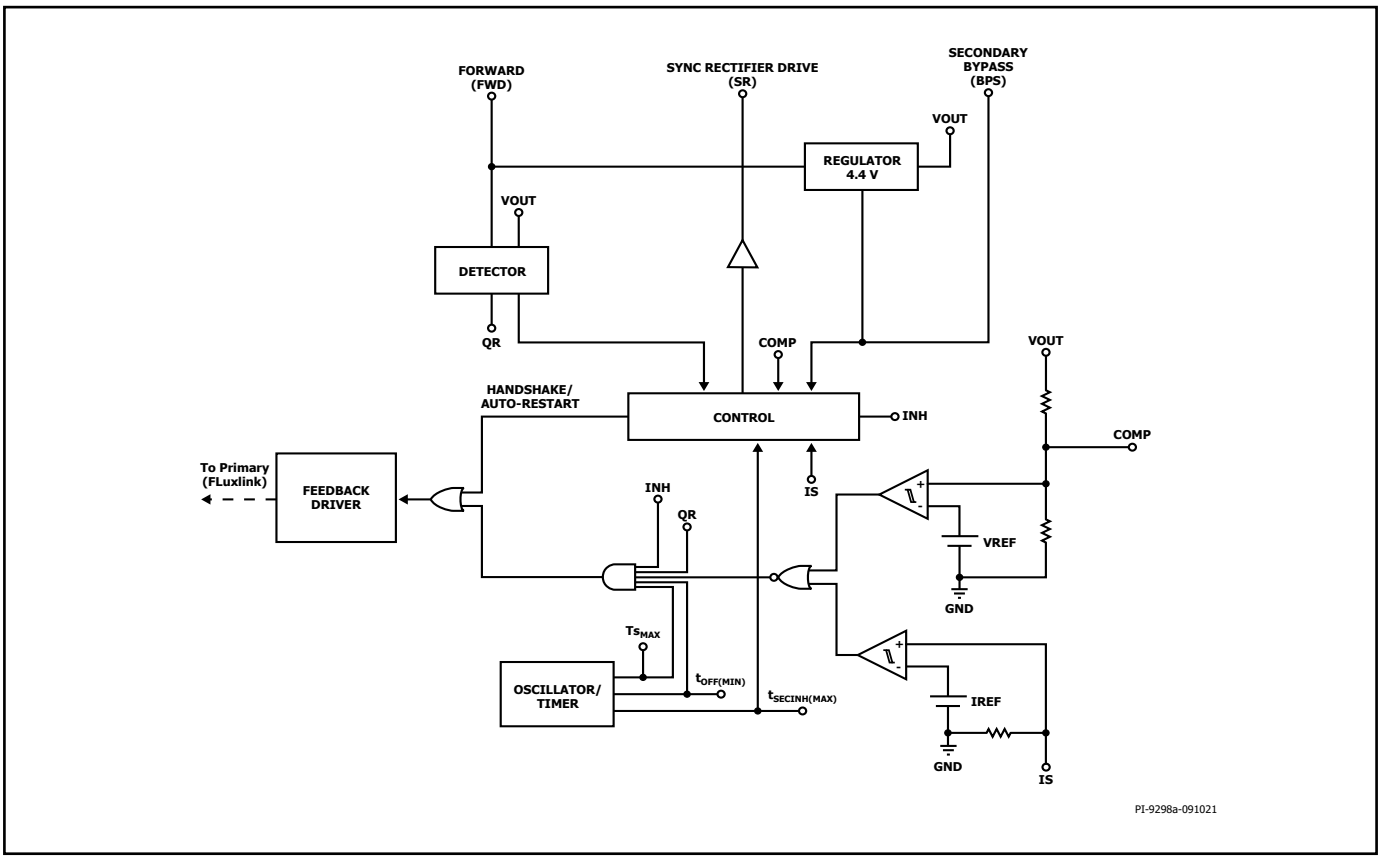


Figure 4. Secondary Controller Block Diagram.

Pin Functional Description

ISENSE (IS) Pin (Pin 1)
Connection to the power supply output terminals. Internal current sense is connected between this pin and the SECONDARY GROUND pin.

SECONDARY GROUND (GND) Pin (Pin 2)
Ground connection for the secondary IC.

COMPENSATION (COMP) Pin (Pin 3)
This pin is connected to internal feedback network. This pin should be left open.

SECONDARY BYPASS (BPS) Pin (Pin 4)
It is the connection point for an external bypass capacitor for the secondary IC supply.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 5)
Connection to gate terminal of external SR FET.

OUTPUT VOLTAGE (VOUT) Pin (Pin 6)
This pin is connected directly to the output voltage of the power supply to provide bias to the secondary IC and an integrated feedback path for accurate regulation of the output voltage.

FORWARD (FWD) Pin (Pin 7)
The connection point to the switching node of the transformer output winding providing information on the primary switch timing plus providing power for the secondary IC when V_{OUT} is below a threshold value.

No Connection (NC) Pin (Pin 8)
Do not connect. This pin should be left open.

No Connection (NC) Pin (Pin 9)
This pin should be tied to SOURCE.

PRIMARY BYPASS (BPP) Pin (Pin 10)
The connection point for an external bypass capacitor for the primary-side supply.

SOURCE (S) Pin (Pin 11-13)
This pin is the power MOSFET source connection. It is also the ground reference for the PRIMARY BYPASS pin.

DRAIN (D) Pin (Pin 16)
This pin is the power MOSFET drain connection.

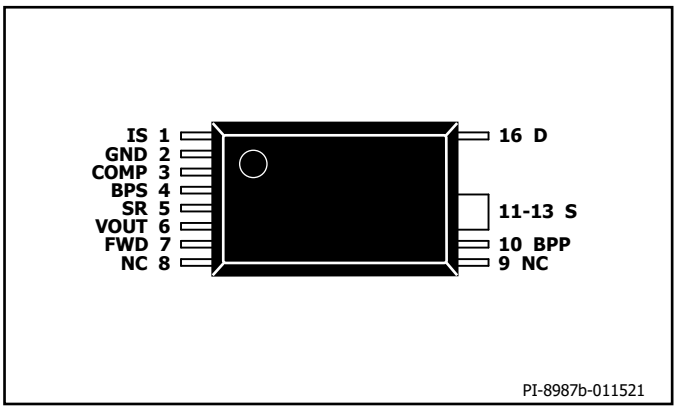


Figure 5. Pin Configuration.

InnoSwitch3-TN Functional Description

The InnoSwitch3-TN IC family combines a high-voltage power MOSFET switch, along with both primary-side and secondary-side controllers with synchronous rectifier (SR) driver.

The architecture incorporates magneto-inductive coupling feedback scheme using FluxLink to provide a safe, reliable and cost-effective means to transmit accurate switching information to the primary-side.

The primary controller on InnoSwitch3-TN is a Quasi-Resonant (QR) flyback controller that has the ability to operate in continuous conduction mode (CCM), boundary mode (CrM) and discontinuous conduction mode (DCM). The controller uses a combination of variable frequency and variable current control. The primary controller consists of an frequency jitter oscillator; a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, audible noise reduction engine for light load operation, bypass overvoltage detection circuit, current limit selection circuitry, over-temperature protection, leading edge blanking, and the power MOSFET.

The InnoSwitch3-TN secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, a constant voltage (CV) and a constant current (CC) control circuit, a 4.4 V regulator on the secondary SECONDARY BYPASS pin, synchronous rectifier (MOSFET) driver, QR mode circuit, oscillator and timing circuits. The secondary controller also provides comprehensive protection features.

Figure 3 and Figure 4 show the functional block diagrams for the primary and secondary controller with the most important features.

Applications Example

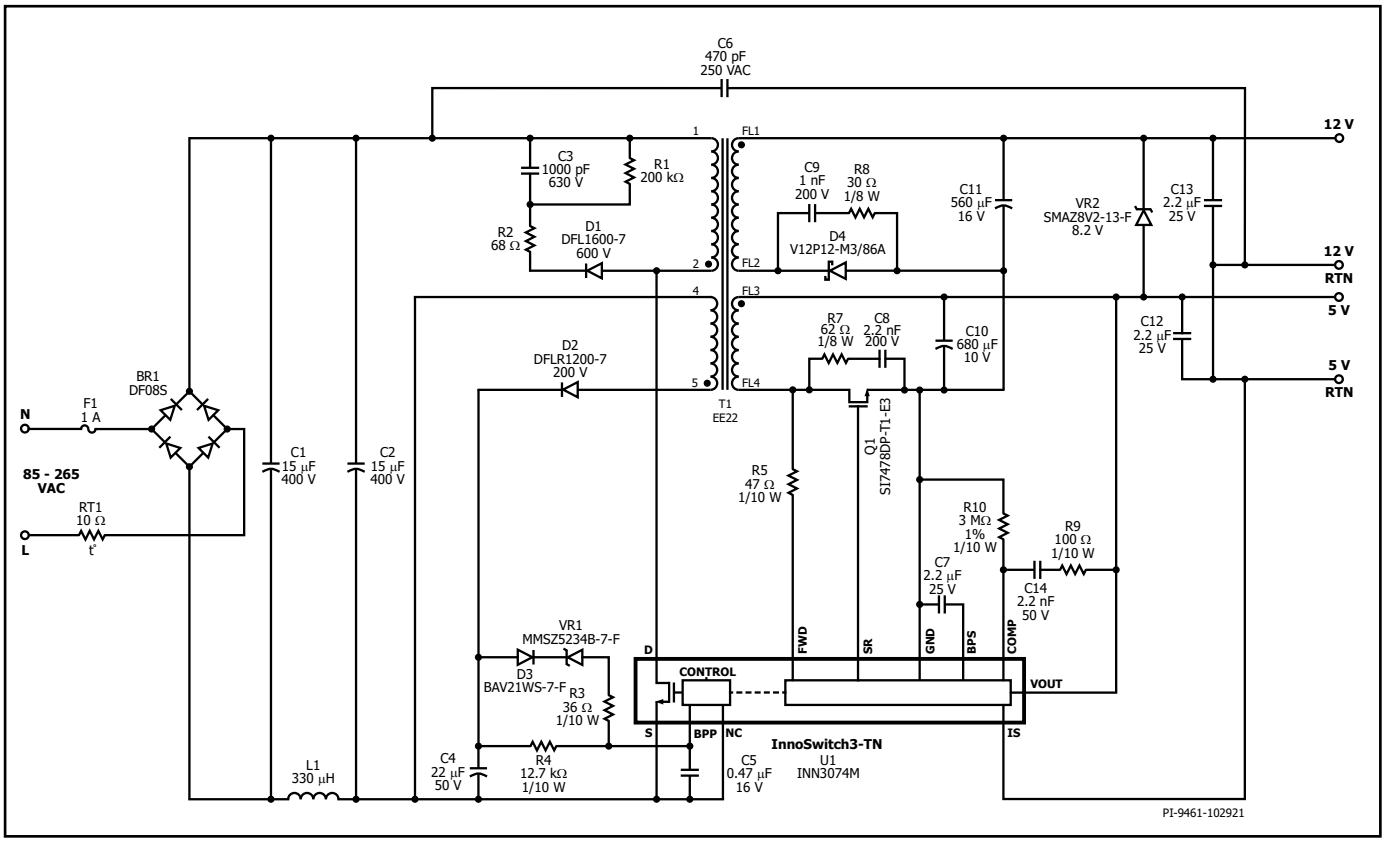


Figure 6. Schematic RDK-710, 5 V, 1.4 A and 12 V, 0.5 A for HVAC (Heating, Ventilation and Air-Conditioning) Application.

The circuit shown in Figure 6 is a low component count 5 V, 1.4 A and 12 V, 0.4 A dual output power supply using the INN3074M IC. This dual output design features a highly efficient design satisfying cross regulation requirements without a post-regulator.

Bridge rectifier BR1 rectifies the AC input supply. Capacitors C1 and C2 provide filtering of the rectified AC input and together with inductor L1 form a pi-filter to attenuate differential mode EMI. Y capacitor C6 connected between the power supply output return and input capacitor help reduce common mode EMI.

Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply.

Input fuse F1 provides protection against excess input current resulting from catastrophic failure of any of the components in the power supply. One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch3-TN IC (U1).

A low-cost RCD clamp formed by diode D1, resistors R2, R1 and capacitor C3 limits the peak drain voltage of U1 at the instant of turn-off of the switch inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The InnoSwitch3-TN IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS pin capacitor (C5) when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer T1.

Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C4. Resistor R4 limits the current being supplied to the PRIMARY BYPASS pin of InnoSwitch3-TN IC (U1). Primary-side overvoltage protection (auto-restart) is obtained using Zener diode VR1 with current limiting resistor R3.

The secondary-side controller of the InnoSwitch3-TN IC provides output voltage sensing, output current sensing and drive to a switch providing synchronous rectification. The 5 V secondary of the transformer is rectified by SR FET Q1 and filtered by capacitor C10. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a snubber (resistor R7 and capacitor C8). The 12 V secondary of the transformer is rectified by Schottky diode D4 (synchronous rectification for the 12 V output is not recommended) and filtered by capacitor C11. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a snubber (resistor R8 and capacitor C9).

Synchronous rectification (SR) is provided by switch Q1. Switch Q1 is turned on by the secondary-side controller inside IC U1, based on the winding voltage sensed via resistor R5 and current is fed into FORWARD pin of the IC. Since the internal feedback circuit of the IC is connected to the 5 V output via VOUT pin, it is recommended to connect the FORWARD pin to the 5 V winding via resistor R5.

In continuous conduction mode of operation, the switch is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous conduction mode of operation,

the power switch is turned off when the voltage drop across the switch falls below 0 V. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectification.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C7 connected to the SECONDARY BYPASS pin of InnoSwitch3-TN IC U1, provides decoupling for the internal circuitry.

Total output current is monitored by an internal sense resistor between the IS and GROUND pins with a voltage threshold of 35 mV typical with minimal loss. The main output is sensed via the VOUT pin, the sensed voltage is processed into the internal feedback resistor divider and compared to internal reference voltage of 1.265 V typical to maintain regulation. Resistor R10 (effectively connected in parallel with the lower internal feedback resistor) can be used to achieve tighter 5 V output regulation. Phase boost circuit, R9 and C14, in parallel with 5 V internal upper feedback resistor reduces the output voltage ripples.

Key Application Considerations

Output Power Table

The data sheet output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following conditions:

1. The minimum DC input voltage is 90 VDC or higher for 85 VAC input, 220 VDC or higher for 230 VAC input or 115 VAC with a voltage-doubler. Input capacitor voltage should be sized to meet these criteria for AC input designs.
2. Efficiency assumption is >82 %.
3. Transformer primary inductance tolerance of ±10%.
4. Reflected output voltage (V_{OR}) is set to maintain K_P = 0.8 at minimum input voltage for universal line and K_P = 1 for high input line designs.
5. Maximum conduction losses for open frame designs = 0.6 W.
6. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink to keep the SOURCE pin temperature at or below 125 °C.
7. Ambient temperature of 40 °C for open frame designs.
8. Below a value of 1, K_P is the ratio of ripple to peak primary current. To prevent reduced power delivery, due to premature termination of switching cycles, a transient K_P limit of ≥0.25 is recommended. This prevents the initial current limit (I_{INT}) from being exceeded at switch turn-on.

Primary-Side Overvoltage Protection (Auto-Restart Mode)

Primary-side sensed output overvoltage protection provided by the InnoSwitch3-TN IC uses an internal protection that is triggered by a threshold current of I_{SD} into the PRIMARY BYPASS pin. In addition to an internal filter, the PRIMARY BYPASS pin capacitor forms an external filter helping noise immunity. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and PRIMARY BYPASS pins of the device. The primary sensed OVP function can be realized by connecting a series combination of a Zener diode, a resistor and a blocking diode from the rectified and filtered bias winding voltage supply to the PRIMARY BYPASS pin. The rectified and filtered bias winding output voltage may be higher than expected (up to 1.5X or 2X the desired value) due to poor coupling of the bias winding with the output winding and the resulting ringing on the bias winding voltage waveform. It is therefore recommended that the rectified bias winding voltage be measured. This measurement should be performed at the lowest input voltage and with highest load on the output. This measured voltage should be used to select the components required to achieve primary sensed OVP. It is recommended that a Zener diode with a clamping voltage approximately 6 V lower than the bias winding rectified voltage at which OVP is expected to be triggered be selected. A forward voltage drop of 1 V can be assumed for the blocking diode. A small signal standard recovery diode is recommended. The blocking diode prevents any reverse current discharging the bias capacitor during start-up. Finally, the value of the series resistor required can be calculated such that a current higher than I_{SD} will flow into the PRIMARY BYPASS pin during an output overvoltage.

Reducing No-load Consumption

The InnoSwitch3-TN IC can start in self-powered mode, drawing energy from the BYPASS pin capacitor charged through an internal current source. Use of a bias winding is however required to provide supply current to the PRIMARY BYPASS pin once the InnoSwitch3-TN IC has started switching. An auxiliary (bias) winding provided on the transformer serves this purpose. A bias winding driver supply to the PRIMARY BYPASS pin enables design of power supplies with low no-load power consumption. Optimization of external components such as the primary snubber and the power transformer will further reduce no-load consumption. Resistor R4 shown in Figure 6 should be adjusted to achieve the lowest no-load input power. For the dual output application, the standby input power, with a 30 mA load on the 5 V output, will be less than 300 mW.

Selection of Components

Components for InnoSwitch3-TN Primary-Side Circuit

BPP Capacitor

A capacitor connected from the PRIMARY BYPASS pin of the InnoSwitch3-TN IC to GND provides decoupling for the primary-side controller. A 0.47 µF capacitor may be used. Though electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use on double sided boards as they enable placement of capacitors close to the IC. Their small size also makes it ideal for compact power supplies. 10 V rated 0805 or larger capacitors with an X5R or X7R dielectric are recommended to ensure that minimum capacitance requirements are met. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 5 V. Do not use Y5U or Z5U / 0603 rated MLCC because this type of SMD ceramic capacitor has very poor voltage and temperature coefficient characteristics.

Bias Winding and External Bias Circuit

The internal regulator connected from the DRAIN pin of the Switch to the PRIMARY BYPASS pin of the InnoSwitch3-TN primary-side controller charges the capacitor connected to the PRIMARY BYPASS pin to achieve start-up. A bias winding should be provided on the transformer with a suitable rectifier and filter capacitor to create a bias supply that can be used to supply at least 1 mA of current to the PRIMARY BYPASS pin.

The turns ratio for the bias winding should be selected such that 7 V is developed across the bias winding when the lowest rated output voltage of the power supply is delivering minimum power to the load. If the voltage is lower than this, no-load input power will increase. The bias current from the external circuit should be set to $I_{S1(MAX)}$ to achieve lowest no-load power consumption when operating the power supply at 230 VAC input, (V_{BPP} > 5 V). A glass passivated standard recovery rectifier diode with low junction capacitance is recommended to avoid the snappy recovery typically seen with fast or ultrafast diodes that can lead to higher radiated EMI. A low ESR

aluminum capacitor of at least 22 μF with a voltage rating 1.2 times greater than the highest voltage developed across the capacitor is recommended. Highest voltage is typically developed across this capacitor when the supply is operated at the highest rated output voltage and load with the lowest input AC supply voltage.

Primary Sensed OVP (Overvoltage Protection)

The voltage developed across the output of the bias winding tracks the power supply output voltage. Though not precise, a reasonably accurate detection of the amplitude of the output voltage can be achieved by the primary-side controller using the bias winding voltage. A Zener diode connected from the bias winding output to the PRIMARY BYPASS pin can reliably detect a secondary overvoltage fault and cause the primary-side controller to enter auto restart. It is recommended that the highest voltage at the output of the bias winding should be measured for normal steady-state conditions (at full load and lowest input voltage) and also under transient load conditions. A Zener diode rated for 1.25 times this measured voltage will typically ensure that OVP protection will only operate in case of a fault.

Primary-Side Snubber Clamp

A snubber circuit should be used on the primary-side as shown in Figure 6. This prevents excess voltage spikes at the drain of the switch at the instant of turn-off of the Switch during each switching cycle though conventional RCD clamps can be used. RCDZ clamps offer the highest efficiency. The circuit example shown in Figure 6 uses an RCD clamp with a resistor in series with the clamp diode. This resistor dampens the ringing at the drain and also limits the reverse current through the clamp diode during reverse recovery. Standard recovery glass passivated diodes with low junction capacitance are recommended as these enable partial energy recovery from the clamp thereby improving efficiency.

Components for InnoSwitch3-TN Secondary-Side Circuit

SECONDARY BYPASS Pin – Decoupling Capacitor

A 2.2 μF, 10 V / X7R or X5R /0805 or larger size multi-layer ceramic capacitor should be used for decoupling the SECONDARY BYPASS pin of the InnoSwitch3-TN IC. Since the SECONDARY BYPASS pin voltage needs to be 4.4 V earlier than output voltage reaches the regulation voltage level, the significantly higher BPS capacitor value could lead to output voltage overshoot during start-up. Values lower than 1.5 μF may not enough capacitance, which can cause unpredictable operation.

The capacitor must be located adjacent to the IC pins. A voltage rating of at least 10 V is recommended at this gives sufficient margin above the BPS voltage. An 0805 size is necessary to ensure sufficient capacitance in operation since the capacitance of ceramic capacitors drops significantly with applied DC voltage especially with small package SMD such as 0603 to give enough margin from BPS voltage, and 0805 size is necessary to guarantee the actual value in operation since the capacitance of ceramic capacitors drops significantly with applied DC voltage especially with small package SMD such as 0603. 6.3 V / 0603 / X5U or Z5U type of MLCC is not recommended for this reason. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 4.4 V. Capacitors with X5R or X7R dielectrics should be used for best results.

FORWARD Pin Resistor

A 47 Ω, 5% resistor is recommended to ensure sufficient IC supply current. A higher or lower resistor value should not be used as it can affect device operation such as the timing of the synchronous rectifier drive. Figures 7, 8, 9 and 10 show examples of unacceptable and acceptable FORWARD pin voltage waveforms. V_D is forward voltage drop across the SR. It is also necessary to ensure that the FORWARD pin voltage is high enough (low VOR) to provide sufficient charging current to the BPS pin capacitor to maintain 4.4 V after handshake during start-up. After the handshake, a high current will flow from the BPS pin capacitor for a short period of time. This energy allows a signal to be sent to the primary-side controller.

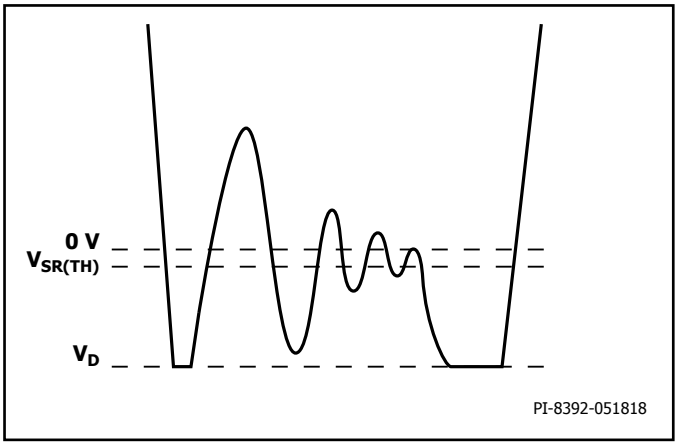


Figure 7. Unacceptable FORWARD Pin Waveform After Handshake with SR Switch Conduction During Flyback Cycle.

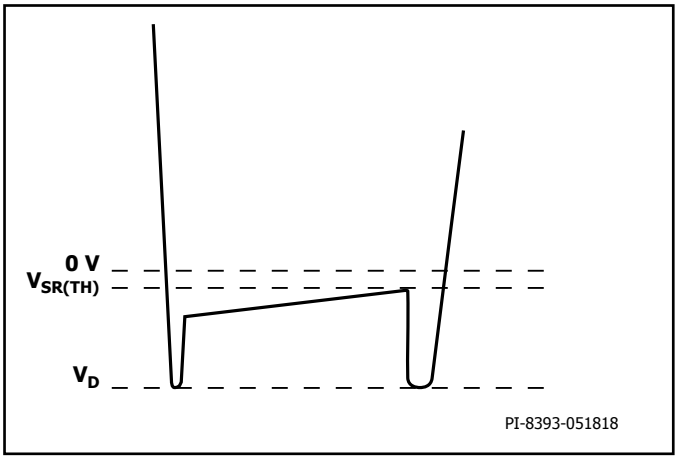


Figure 8. Acceptable FORWARD Pin Waveform After Handshake with SR Switch Conduction During Flyback Cycle.

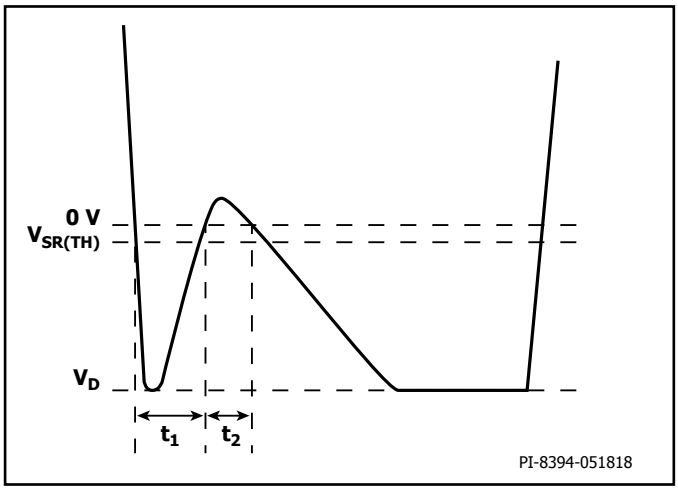


Figure 9. Unacceptable FORWARD Pin Waveform before Handshake with Body Diode Conduction During Flyback Cycle.

Note:
If $t_1 + t_2 > 1.5\ \mu s \pm 50$ ns, the controller may fail the handshake and trigger a primary bias winding OVP latch-off/auto-restart.

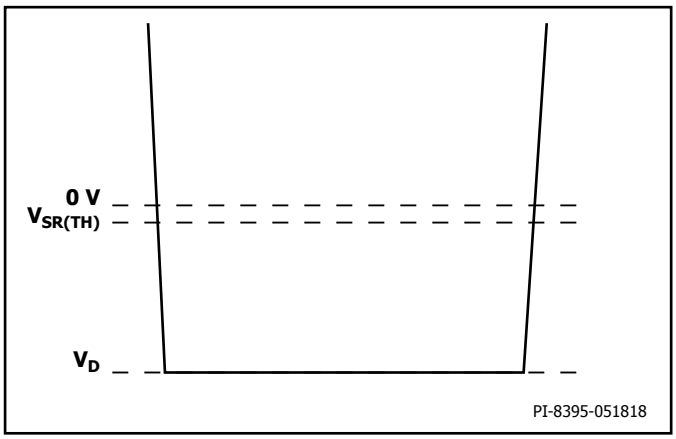


Figure 10. Acceptable FORWARD Pin Waveform before Handshake with Body Diode Conduction During Flyback Cycle.

SR Switch Operation and Selection

Although a simple diode rectifier and filter works for the output, use of an SR FET enables the significant improvement in operating efficiency often necessary to meet the European CoC and the U.S. DoE energy efficiency requirements. The secondary-side controller turns on the SR FET once the flyback cycle begins. The SR FET gate should be tied directly to the SYNCHRONOUS RECTIFIER DRIVE pin of the InnoSwitch3-TN IC (no additional resistors should be connected in the gate circuit of the SR FET). The SR FET is turned off once the V_{DS} of the SR FET reaches 0 V. A FET with 18 mΩ $R_{DS(ON)}$ is appropriate for a 5 V, 2 A output, and a Schottky diode is suitable for designs rated with a 12 V, 0.4 A output. The SR FET driver uses the SECONDARY BYPASS pin for its supply rail, and this voltage is typically 4.4 V. A FET with a high threshold voltage is therefore not suitable; FETs with a threshold voltage of 1.5 V to 2.5 V are ideal. There is a slight delay between the commencement of the flyback cycle and the turn-on of the SR FET. During this time, the body diode of the SR FET conducts. If an external parallel Schottky diode is used, this current mostly flows through the Schottky diode. Once the InnoSwitch3-TN IC detects end of the flyback cycle, voltage across SR FET $R_{DS(ON)}$ reaches 0 V, any remaining portion of the flyback cycle is completed with the current commutating to the body diode of the SR FET or the external parallel Schottky diode. Use of the Schottky diode parallel to the SR FET may provide higher efficiency and typically a 1 A surface mount Schottky diode is adequate. However, the gains are modest. For a 5 V, 2 A design the external diode adds ~0.1% to full load efficiency at 85 VAC and ~0.2% at 230 VAC.

The voltage rating of the Schottky diode and the SR FET should be at least 1.4 times the expected peak inverse voltage (PIV) based on the turns ratio used for the transformer. 60 V rated FETs and diodes are suitable for most 5 V designs that use a V_{OR} <70 V, and 120 V rated Schottky diodes are suitable for 12 V designs.

The interaction between the leakage reactance of the output windings and the SR FET capacitance (C_{OSS}) leads to ringing on the voltage waveform at the instance of voltage reversal at the winding due to primary switch turn-on. This ringing can be suppressed using an RC snubber connected across the SR FET. A snubber resistor in the range of 10 Ω to 47 Ω may be used (higher resistance values lead to noticeable drop in efficiency). A capacitance value of 1 nF to 2.2 nF is adequate for most designs.

Output Capacitor

Low ESR aluminum electrolytic capacitors are suitable for use with most high frequency flyback switching power supplies, though the use of aluminum-polymer solid capacitors have gained considerable popularity due to their compact size, stable temperature characteristics, extremely low ESR and high RMS ripple current rating.

Typically, 200 μF to 300 μF of aluminum-polymer capacitance per ampere of output current is adequate. The other factor that influences choice of the capacitance is the output ripple. Ensure that capacitors with a voltage rating higher than the highest output voltage plus sufficient margin be used.

Internal Output Voltage Feedback Circuit
The output voltage COMP pin voltage is 1.265 V. The VOUT pin should be connected at the output of the power supply such that the voltage at the COMP pin will be 1.265 V when the output is at its desired voltage by the built-in divider. The internal lower feedback divider resistor is connected to the SECONDARY GROUND pin. A resistor between COMP pin and GND pin can be used to increase the 5 V output voltage as shown in Figure 11.

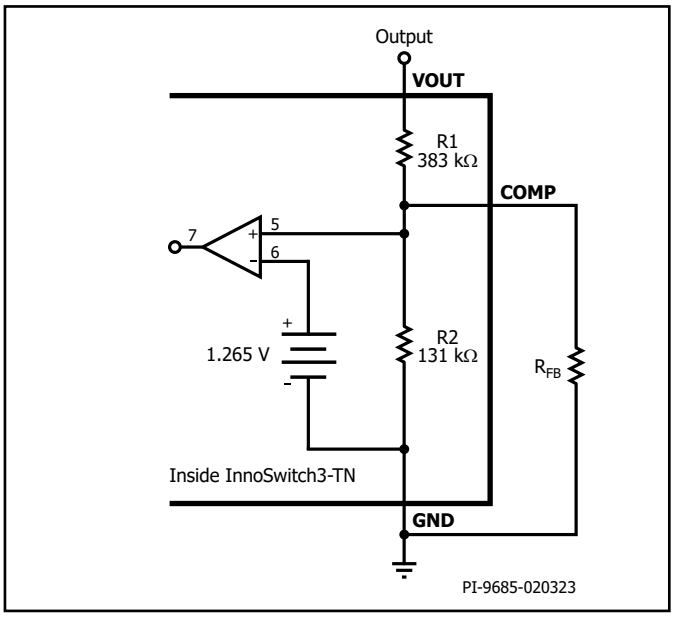


Figure 11. Add a Resistor to Increase the 5 V Output Voltage.

R_{FB} can be calculated to increase output voltage as follows:

Let RT = R2 // R_{FB}

$$= \frac{R2 \times R_{FB}}{R2 + R_{FB}}$$

$$V_{OUT} = \frac{V_R \times (R1 + RT)}{RT}, \text{ where } V_R = 1.265 \text{ V}$$

$$R_{FB} = \frac{V_R \times R1 \times R2}{((V_{OUT} - V_R) \times R2 - V_R \times R1)}$$

V_{OUT}	R_{FB} (Ω)
7 V	238 kΩ
9 V	120 kΩ
12 V	69 kΩ

Recommendations for Circuit Board Layout

See Figure 12 for a recommended circuit board layout for an InnoSwitch3-TN based power supply.

Single-Point Grounding
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitors
The PRIMARY BYPASS and SECONDARY BYPASS pin capacitor must be located directly adjacent to the PRIMARY BYPASS-SOURCE and SECONDARY BYPASS-SECONDARY GROUND pins respectively and connections to these capacitors should be routed with short traces.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and IC should be kept as small as possible.

Primary Clamp Circuit
A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener diode (~200 V) and diode clamp across the primary winding. To reduce EMI, minimize the loop from the clamp components to the transformer and IC.

Thermal Considerations

The SOURCE pin is internally connected to the IC lead frame and provides the main path to remove heat from the device. Therefore, the SOURCE pin should be connected to a copper area underneath the IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, it can be maximized for good heat sinking without compromising EMI performance. Similarly for the output SR Switch, maximize the PCB area connected to the pins on the package through which heat is dissipated from the SR Switch.

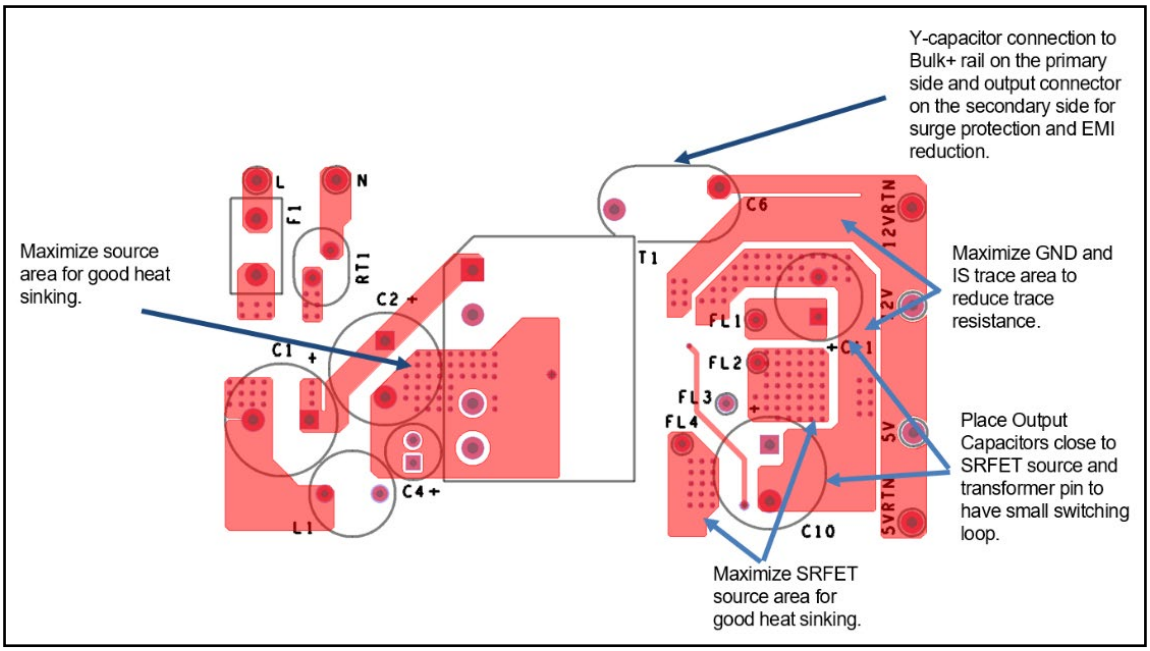
Sufficient copper area should be provided on the board to keep the IC temperature safely below the absolute maximum limits. It is recommended that the copper area provided for the copper plane on which the SOURCE pin of the IC is soldered is sufficiently large to keep the IC temperature below 110 °C when operating the power supply at full rated load and at the lowest rated input AC supply voltage.

Y Capacitor
The Y capacitor should be placed directly between the primary input filter capacitor positive terminal and the output positive or return terminal of the transformer secondary. This routes high amplitude common mode surge currents away from the IC. Note – if an input pi-filter (C, L, C) EMI filter is used then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

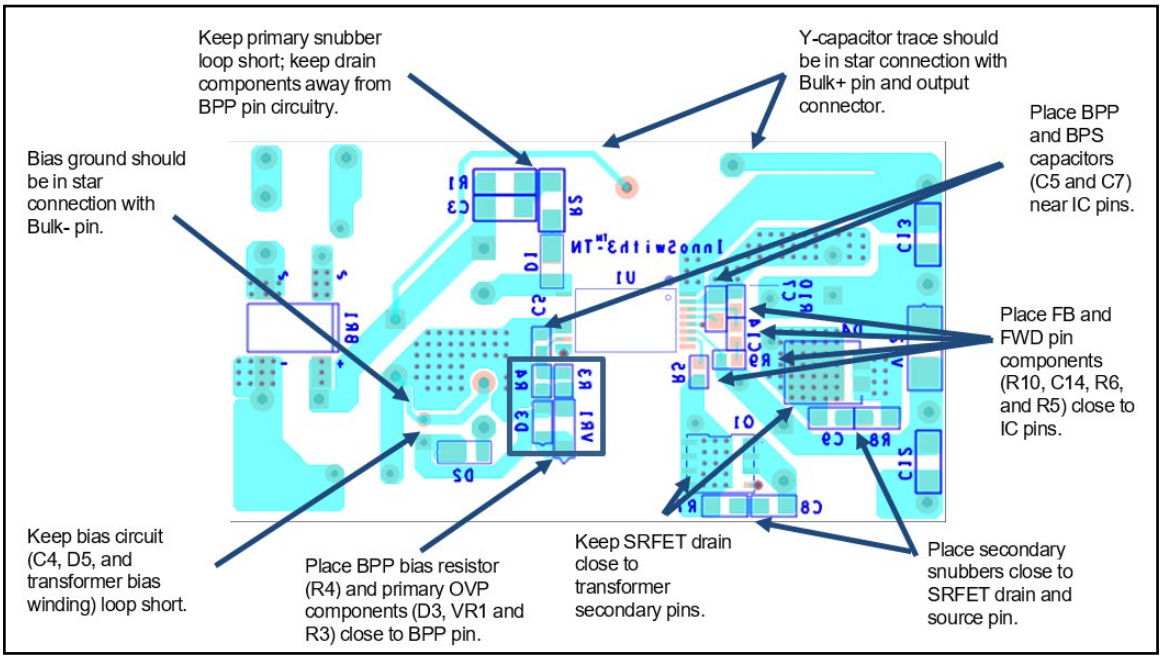
Output SR Switch
For best performance, the area of the loop connecting the secondary winding, the output SR Switch and the output filter capacitor, should be minimized.

Drain Node
The drain switching node is the dominant noise generator. As such the components connected the drain node should be placed close to the IC and away from sensitive feedback circuits. The clamp circuit components should be located physically away from the PRIMARY BYPASS pin and trace lengths minimized. The loop area of the loop comprising of the input rectifier filter capacitor, the primary winding and the IC primary-side switch should be kept as small as possible.

Layout Example



PCB – Top Side



PCB – Bottom Side

Figure 12. PCB Layout Example.

Recommendations for EMI Reduction

1. Appropriate component placement and small loop areas of the primary and secondary power circuits help minimize radiated and conducted EMI. Care should be taken to achieve a compact loop area.
2. A small capacitor in parallel to the clamp diode on the primary-side can help reduce radiated EMI.
3. A resistor in series with the bias winding helps reduce radiated EMI.
4. Common mode chokes are typically required at the input of the power supply to sufficiently attenuate common mode noise. However, the same performance can be achieved by using shield windings on the transformer. Shield windings can also be used in conjunction with common mode filter inductors at input to improve conducted and radiated EMI margins.
5. Adjusting SR switch RC snubber component values can help reduce high frequency radiated and conducted EMI.
6. A pi-filter comprising differential inductors and capacitors can be used in the input rectifier circuit to reduce low frequency differential EMI.
7. A 1 µF ceramic capacitor connected at the output of the power supply helps to reduce radiated EMI.

Recommendations for Transformer Design

Transformer design must ensure that the power supply delivers the rated power at the lowest input voltage. The lowest voltage on the rectified DC bus depends on the capacitance of the filter capacitor used. At least 2 µF / W is recommended to always keep the DC bus voltage above 70 V, though 3 µF / W provides sufficient margin. The ripple on the DC bus should be measured to confirm the design calculations for transformer primary-winding inductance selection.

Switching Frequency (f_{SW})
It is a unique feature in InnoSwitch3-TN that for full load, the designer can set the switching frequency to between 25 kHz to 95 kHz. For lowest temperature, the switching frequency should be set to around 60 kHz. For a smaller transformer, the full load switching frequency needs to be set to 95 kHz. When setting the full load switching frequency it is important to consider primary inductance and peak current tolerances to ensure that average switching frequency does not exceed 110 kHz which may trigger auto-restart due to overload protection.

Reflected Output Voltage, V_{OR} (V)
This parameter describes the effect on the primary switch drain voltage of the secondary-winding voltage during diode/SR conduction which is reflected back to the primary through the turns ratio of the transformer. To ensure flattest efficiency over line/load, set reflected output voltage (V_{OR}) to maintain K_P = 0.8 at minimum input voltage for universal input and K_P = 1 for high-line-only conditions. It is important to note that when the average BPS charging current is less than 2.5 mA after handshake at the minimum input voltage during start up, the power supply may fail to start-up and stay in auto-restart mode. Incrementally lower the V_{OR} to increase FORWARD pin voltage until the average BPS charging current becomes higher than 2.5 mA.

Consider the Following for Design Optimization

1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the value of the input capacitor and maximizes power delivery from a given InnoSwitch3-TN device.
2. Higher V_{OR} reduces the voltage stress on the output diodes and SR switches.
3. Higher V_{OR} increases leakage inductance which reduces power supply efficiency.
4. Higher V_{OR} increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

Ripple to Peak Current Ratio, K_P
A K_P below 1 indicates continuous conduction mode, where K_P is the ratio of ripple-current to peak-primary-current (Figure 13).

$$K_P \equiv K_{RP} = I_R / I_P$$

A value of K_P higher than 1, indicates discontinuous conduction mode. In this case K_P is the ratio of primary Switch off-time to the secondary diode conduction-time.

$$K_P \equiv K_{DP} = (1 - D) \times T/ t = V_{OR} \times (1 - D_{MAX}) / ((V_{MIN} - V_{DS}) \times D_{MAX})$$

It is recommended that a K_P close to 0.9 at the minimum expected DC bus voltage should be used for most InnoSwitch3-TN designs. A K_P value of <1 results in higher transformer efficiency by lowering the primary RMS current but results in higher switching losses in the primary-side Switch resulting in higher InnoSwitch3-TN temperature. The PIXIs spreadsheet can be used to effectively optimize selection of K_P, inductance of the primary winding, transformer turns ratio, and the operating frequency while ensuring appropriate design margins.

Core Type
Choice of a suitable core is dependent on the physical limits of the power supply enclosure. It is recommended that only cores with low loss be used to reduce thermal challenges.

Safety Margin, M (mm)
For designs that require safety isolation between primary and secondary that are not using triple insulated wire, the width of the safety margin to be used on each side of the bobbin is important. For universal input designs a total margin of 6.2 mm is typically required – 3.1 mm being used on either side of the winding. For vertical bobbins the margin may not be symmetrical. However, if a total margin of 6.2 mm is required then the physical margin can be placed on only one side of the bobbin. For designs using triple insulated wire it may still be necessary to add a small margin to meet required creepage distances. Many bobbins exist for each core size and each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance to determine what specific margin is required. As the margin reduces the available area for the windings, the winding area will disproportionately reduce for small core sizes.

It is recommended that for compact power supply designs using an InnoSwitch3-TN IC, triple insulated wire should be used.

Primary Layers, L
Primary layers should be in the range of 1 ≤ L ≤ 3 and in general should be the lowest number that meets the primary current density limit (CMA). A value of ≥200 Cmils / Amp can be used as a starting point for most designs. Higher values may be required due to thermal constraints. Designs with more than 3 layers are possible but the increased leakage inductance and the physical fit of the windings should be considered. A split primary construction may be helpful for designs where clamp dissipation due to leakage inductance is too high. In split primary construction, half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement. This arrangement is often disadvantageous for low power designs as this typically increases common mode noise and adds cost to the input filtering.

Maximum Operating Flux Density, B_M (Gauss)
A maximum value of 3800 gauss at the peak device current limit is recommended to limit the peak flux density at start-up and under output short-circuit conditions. Under these conditions the output voltage is low and little reset of the transformer occurs during the Switch off-time. This allows the transformer flux density to staircase beyond the normal operating level. A value of 3800 gauss at the peak current limit of the selected device together with the built-in protection features of InnoSwitch3-TN IC provide sufficient margin to prevent core saturation under start-up or output short-circuit conditions.

Transformer Primary Inductance, L_P

Once the lowest operating input voltage, switching frequency at full load, and required V_{OR} are determined, the transformers primary inductance can be calculated. The PIXIs design spreadsheet can be used to assist in designing the transformer.

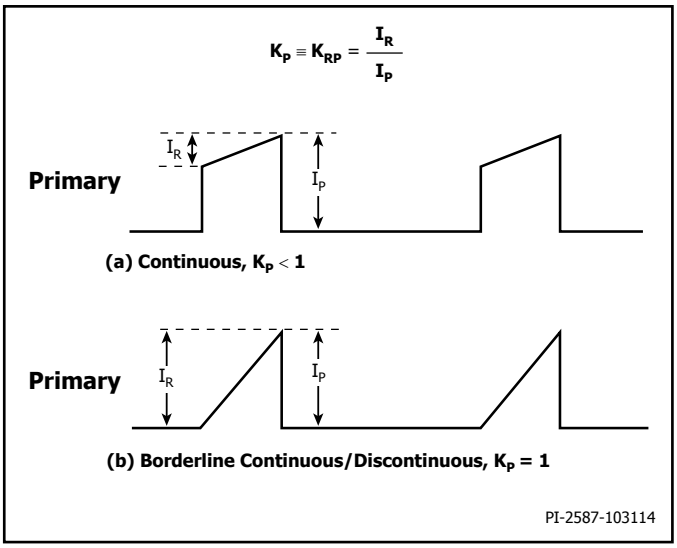


Figure 13. Continuous Conduction Mode Current Waveform, $K_P < 1$.

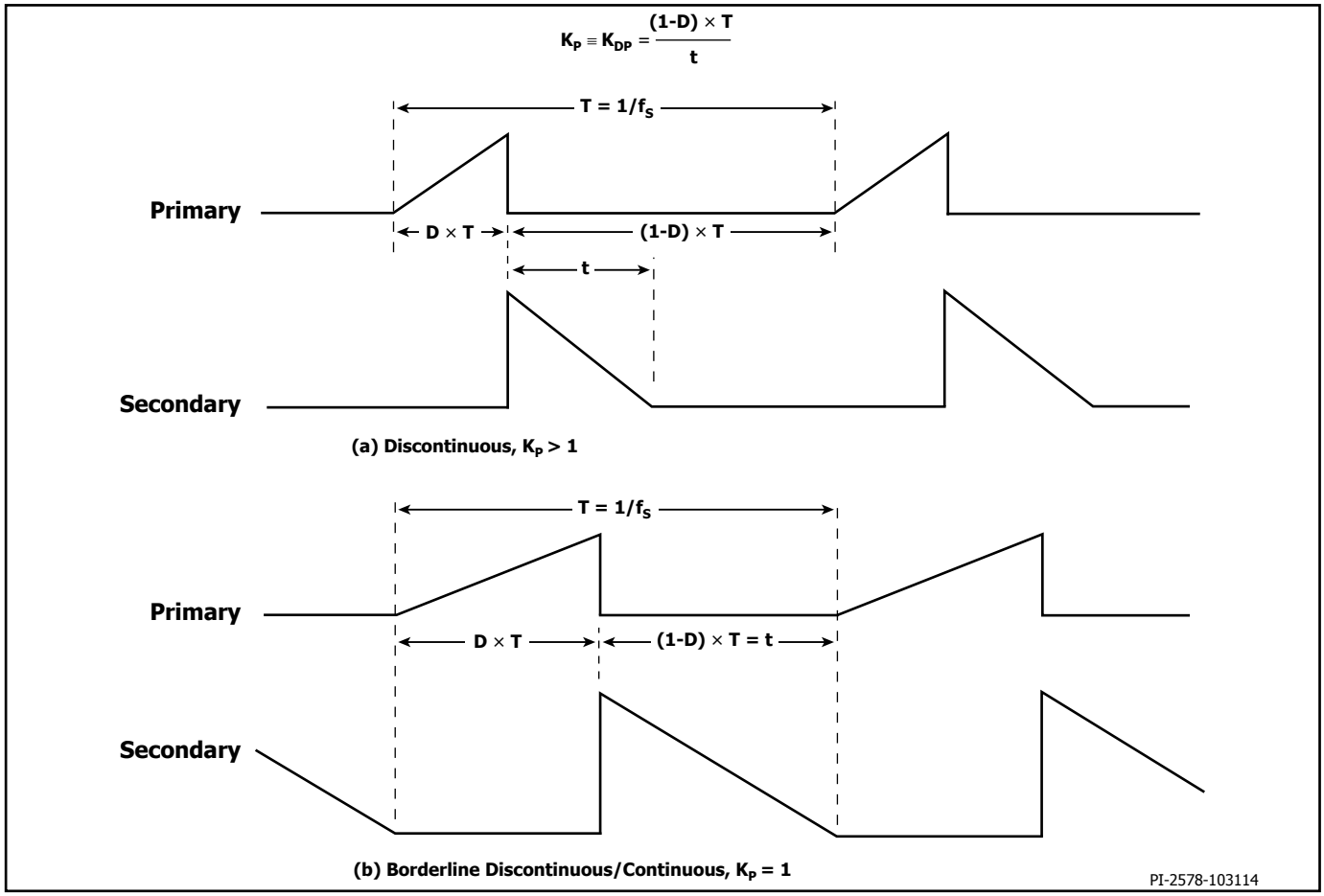


Figure 14. Discontinuous Conduction Mode Current Waveform, $K_P > 1$.

Quick Design Checklist

As with any power supply, the operation of all InnoSwitch3-TN designs should be verified on the bench to make sure that component limits are not exceeded under worst-case conditions.

As a minimum, the following tests are strongly recommended:

1. Maximum Drain Voltage – Verify that V_{DS} of InnoSwitch3-TN and SR FET do not exceed 90% of breakdown voltages at the highest input voltage and peak (overload) output power in normal operation and during start-up.
2. Maximum Drain Current – At maximum ambient temperature, maximum input voltage and peak output (overload) power verify drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start up. Repeat under steady-state conditions and verify that the leading edge current spike is below $I_{LIMIT(MIN)}$ at the end of $t_{LEB(MIN)}$. Under all conditions, the maximum drain current should be below the specified absolute maximum ratings.
3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that temperature specification limits for InnoSwitch3-TN IC, transformer, output SR FET, and output capacitors are not exceeded. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of the InnoSwitch3-TN IC as specified in the data sheet.

Under low-line maximum power, a maximum InnoSwitch3-TN SOURCE pin temperature of 110 ºC is recommended to allow for these variations.

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage	725 V
DRAIN Pin Peak Current: INN3072M	1.6 A
INN3073M	2.24 A
INN3074M	3.26 A
BPP/BPS Pin Voltage	-0.3 to 6 V
BPP/BPS Pin Current	100 mA
FWD Pin Voltage	-1.5 to 150 V
COMP Pin Voltage	-0.3 V to 6 V
SR Pin Voltage	-0.3 V to 6 V
VOUT Pin Voltage	-0.3 V to 16 V
Storage Temperature	-65 to 150 °C
Operating Junction Temperature[3]	-40 to 150 °C
Ambient Temperature	-40 to 105 °C
Lead Temperature[4]	260 °C

Notes:
1. All voltages referenced to SOURCE and Secondary GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Normally limited by internal circuitry.
4. 1/16" from case for 5 seconds.

Thermal Resistance

Thermal Resistance: MinSOP-16A	
(θ_{JA})	87 °C/W[1], 82 °C/W[2]
(θ_{JC})	31 °C/W[3]

Notes:
1. Soldered to 0.36 sq. inch (232 mm^2) 2 oz. (610 g/m^2) copper clad.
2. Soldered to 1 sq. inch (645 mm^2), 2 oz. (610 g/m^2) copper clad.
3. The case temperature is measured on the top of the package.

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Jitter Frequency	f_M	T_J = 25 °C, f_{SW} = 100 kHz			1.1		kHz
Maximum On-Time	$t_{ON(MAX)}$	T_J = 25 °C			15	18	µs
BPP Supply Current	I_{S1}	V_{BPP} = V_{BPP} + 0.1 V (Switch not Switching) T_J = 25 °C			170	280	µA
	I_{S2}	V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at f_{SREQ}) T_J = 25 °C	INN3072M		378		µA
			INN3073M		443		
			INN3074M		521		
BPP Pin Charge Current	I_{CH1}	V_{BPP} = 0 V, T_J = 25 °C			-1.3		mA
	I_{CH2}	V_{BPP} = 4 V, T_J = 25 °C			-4.4		
BPP Pin Voltage	V_{BPP}	T_J = 25 °C		4.65	4.9	5.15	V
BPP Pin Voltage Hysteresis	$V_{BPP(H)}$	T_J = 25 °C			0.4		V
BPP Shunt Voltage	V_{SHUNT}	I_{BPP} = 2 mA T_J = 25 °C		5.05	5.33	5.74	V
BPP Power-Up Reset Threshold Voltage	$V_{BPP(RESET)}$	T_J = 25 °C		2.4	3.15	3.6	V
Circuit Protection							
Standard Current Limit	I_{LIMIT}	di/dt = 138 mA/µs T_J = 25 °C	INN3072M	510	550	590	mA
		di/dt = 163 mA/µs T_J = 25 °C	INN3073M	600	650	700	
		di/dt = 188 mA/µs T_J = 25 °C	INN3074M	690	750	810	
BYPASS Pin Latching Shutdown Threshold Current	I_{SD}	T_J = 25 °C			7.4	10.0	mA
Auto-Restart On-Time	t_{AR}	T_J = 25 °C			90		ms
Auto-Restart Trigger Skip Time	$t_{AR(SK)}$	T_J = 25 °C See Note A			1.5		sec
Auto-Restart Off-Time	$t_{AR(OFF)}$	T_J = 25 °C			2.3		sec
Short Auto-Restart Off-Time	$t_{AR(OFF)SH}$	T_J = 25 °C See Note A			0.3		sec

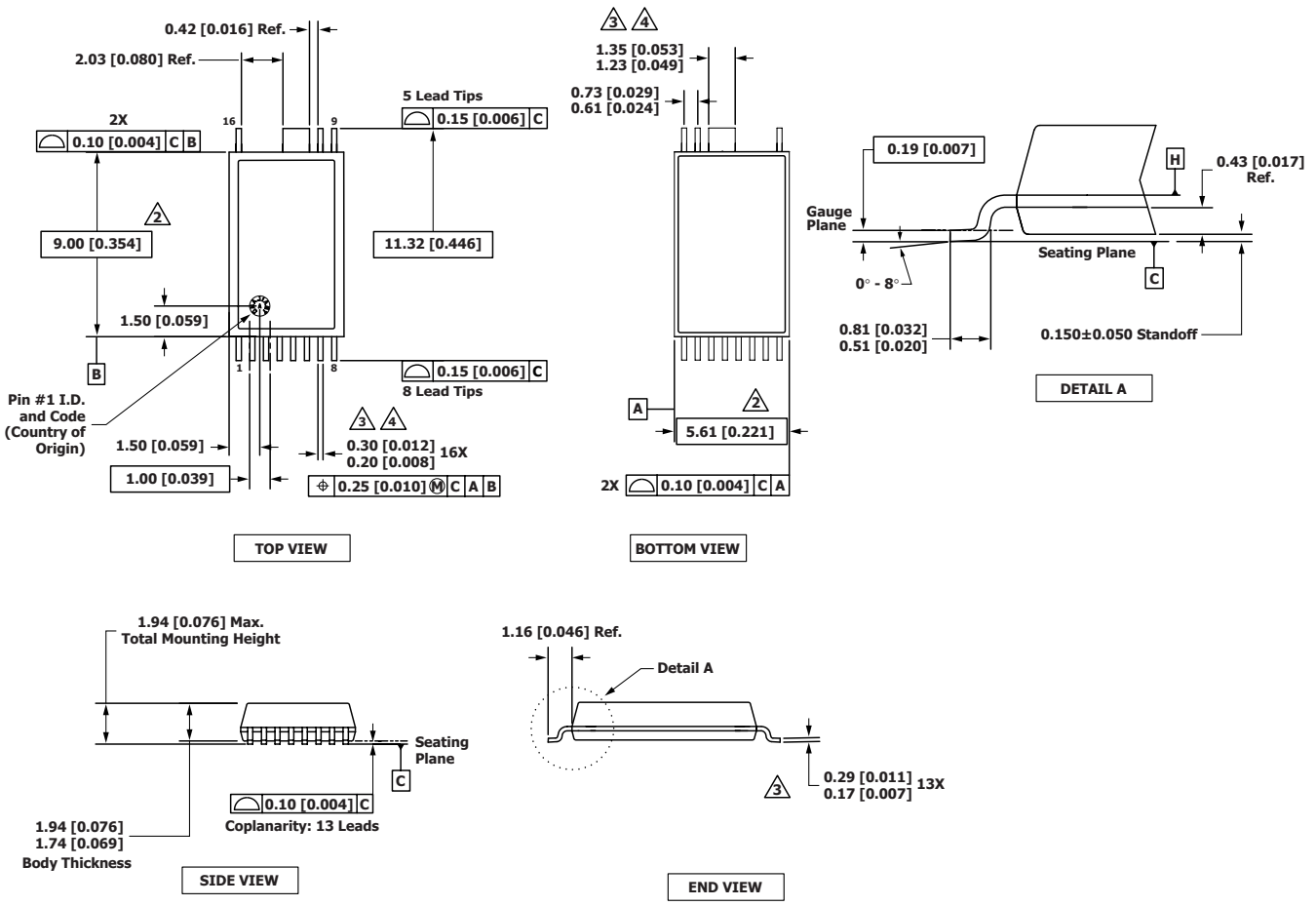
Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	INN3072M $I_D = I_{LIMIT}$	T_J = 25 °C		6.30	7.25	Ω
			T_J = 100 °C		9.77	11.24	
		INN3073M $I_D = I_{LIMIT}$	T_J = 25 °C		4.42	5.08	
			T_J = 100 °C		6.85	7.88	
		INN3074M $I_D = I_{LIMIT}$	T_J = 25 °C		3.22	3.70	
			T_J = 100 °C		4.99	5.74	
OFF-State Drain Leakage Current	I_{DSS1}	$V_{BPP} = V_{BPP}$ + 0.1 V V_{DS} = 80% Peak Drain Voltage T_J = 125 °C				200	µA
	I_{DSS2}	$V_{BPP} = V_{BPP}$ + 0.1 V V_{DS} = 325 V T_J = 25 °C			15		µA
Breakdown Voltage	BV_{DSS}	$V_{BPP} = V_{BPP}$ + 0.1 V T_J = 25 °C		725			V
Drain Supply Voltage				50			V
Thermal Shutdown	T_{SD}	See Note A		132	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note A			70		°C

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Secondary							
Output Voltage	V_{OUT}	End of board at no-load T_J = 25 °C		4.85	5.00	5.15	V
VOUT Pin Auto-Restart Threshold	$V_{OUT(AR)}$				0.630 × V_{OUT}		V
VOUT Pin Auto-Restart Timer	$t_{VOUT(AR)}$	T_J = 25 °C			50		ms
BPS Pin Current at No-Load	I_{SNL}	T_J = 25 °C			260		µA
BPS Pin Voltage	V_{BPS}	T_J = 25 °C		4.12	4.4	4.7	V
BPS Pin Undervoltage Threshold	$V_{BPS(UVLO)(TH)}$	T_J = 25 °C			3.80	4.04	V
BPS Pin Undervoltage Hysteresis	$V_{BPS(UVLO)(H)}$	T_J = 25 °C			0.65		V
Maximum Switching Frequency	f_{SREQ}				132		kHz
Constant Current Regulation Threshold	I_{CC}	T_J = 25 °C	INN3072M	1.5	1.7	1.9	A
			INN3073M	2.0	2.2	2.4	
			INN3074M	2.4	2.6	2.8	
Minimum Off-Time	$t_{OFF(MIN)}$	T_J = 25 °C			3.4	4.0	µs
Soft-Start Frequency Ramp Time	$t_{SS(RAMP)}$	T_J = 25 °C			11		ms

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Synchronous Rectifier @ T_J = 25 °C							
SR Pin Drive Voltage	V_{SR}				4.4		V
SR Pin Threshold	$V_{SR(TH)}$	T_J = 25 °C			-2.5	0	mV
Rise Time	t_R	T_J = 25 °C C_{LOAD} = 2 nF	0-100%		81		ns
			10-90%		55		
Fall Time	t_F	T_J = 25 °C C_{LOAD} = 2 nF	0-100%		142		ns
			10-90%		95		
Output Pull-Up Resistance	R_{PU}	T_J = 25 °C V_{BPS} = 4.4 V I_{SR} = 30 mA			8.9		Ω
Output Pull-Down Resistance	R_{PD}	T_J = 25 °C V_{BPS} = 4.4 V I_{SR} = 30 mA			12.3		Ω

NOTES:
A. This parameter is derived from characterization.

MinSOP-16A (M Package)



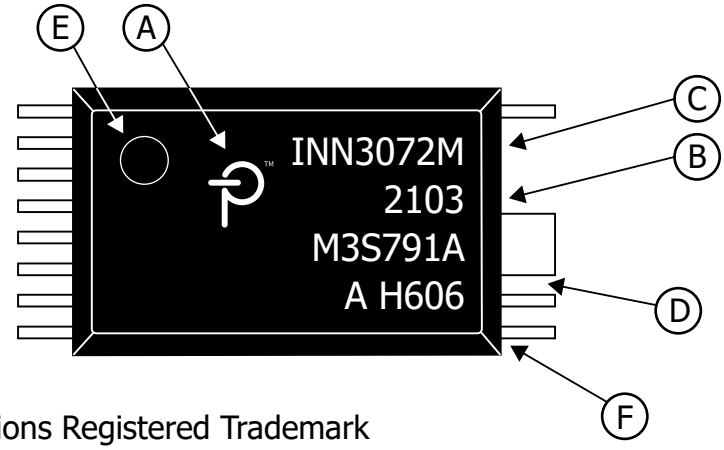
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and inter-lead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 [0.007] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters [Inches].
6. Datums A and B to be determined in Datum H.

PI-8833-091021
POD-MinSOP-16A Rev C

PACKAGE MARKING

MinSOP-16A



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Pin 1 Indicator
F. Test Lot Information

PI-9220b-070921

Parameter	Conditions	Rating	Units
Ratings for UL1577			
Primary-Side Current Rating	Current from pin (11-13) to pin 16	1.3	A
Primary-Side Power Rating	T_{AMB} = 25 °C (device mounted in socket resulting in T_{CASE} = 120 °C)	1.35	W
Secondary-Side Power Rating	T_{AMB} = 25 °C (device mounted in socket)	0.125	W
Secondary-Side Power Rating	Current from pin 1 to pin 2	3.5	A

Parameter	Symbol	Conditions	Rating	Units
Package Characteristics				
Clearance	CLR		9.48	mm (min)
Creepage	CPG		9.48	mm (min)
Distance Through Insulation	DTI		>0.4	mm
Comparative Tracking Index	CTI		>600	V
Isolation Resistance, Input to Output	R_{IO}	V_{IO} = 500 V, T_J = 25 °C (See Note 1)	10^{12}	Ω (min)
		V_{IO} = 500 V, 100 °C ≤ T_J ≤ 125 °C (See Note 1)	10^{11}	
Isolation Capacitance, Input to Output	C_{IO}	(See Note 1)	1	pF
Package Insulation Characteristics (See Note 2)				
Maximum RMS Working Isolation Voltage	$V_{IORM(RMS)}$		512	V_{RMS} (max)
Maximum Repetitive Peak Isolation Voltage	$V_{IORM(PK)}$		725	V_{PK} (max)
Maximum Transient Peak Isolation Voltage	V_{IOTM}	Test Voltage = V_{IOTM}, t = 60 s (qualification)	6.6	kV_{PK} (max)
		t = 1 s (100% production)	8	
Maximum Surge Isolation Voltage	V_{IOSM}	Surge Test 1.2/50 usec Table 2 IEC 60747-17	10.4	kV_{PK} (max)
Input to Output Test Peak Voltage	V_{PD}	Method A, After Environmental Tests Subgroup 1, V_{PD} = 1.6 × V_{IORM}, t = 10 s (qualification) Partial Discharge < 5 pC	1160	V_{PEAK} (min)
		Method A, After Input / Output Safety Test Subgroup 2/3, V_{PD} = 1.2 × V_{IORM}, t = 10 s, (qualification) Partial Discharge < 5 pC	870	
		Method B1, 100% Production Test, V_{PD} = 1.875 × V_{IORM}, t = 1 s Partial Discharge < 5 pC	1360	
Insulation Resistance	R_S	V_{IO} = 500 V at T_J = 150 °C	$>10^9$	Ω
Climatic Category			40/125/21	

Parameter	Conditions	Specifications
IEC 60664-1 Rating Table		
Basic Isolation Group	Material Group	I
Insulation Classification	Rated Mains RMS voltage ≤ 150 V	I - IV
	Rated Mains RMS voltage ≤ 300 V	I - IV
	Rated Mains RMS voltage ≤ 600 V	I - IV
	Rated Mains RMS voltage ≤ 1000 V	I - III

Note 1: All pins on each side of the barrier tied together creating a two-terminal device
Note 2: VDE 0884-17 (IEC/EN 60747-17) Only applies to devices with the following H-codes: H156, H157, H158, H159, H160

Feature Code Table

Features	Specifications
FeedBack Resistors	Internal V_{OUT} = 5.0 V
IS Sense Resistor	Internal CC
ILIM Selectable	No
Primary Fault Response	Auto-Restart
Secondary Fault Response	Auto-Restart
Auto-Restart	63% V_{OUT}
Over-Temperature Protection	Hysteretic

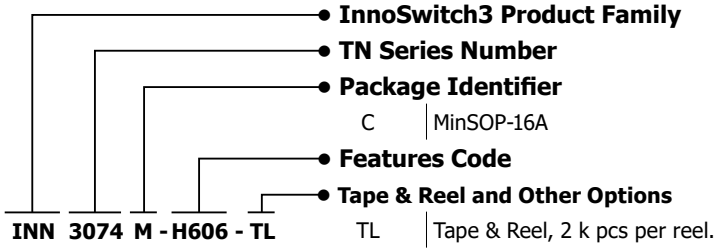
MSL Table

Part Number	MSL Rating
INN3072M	3
INN3073M	3
INN3074M	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78E	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2017	> ±2000 V on all pins
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2018	> ±500 V on all pins

Part Ordering Information



Revision	Notes	Date
C	Code A release.	11/21
D	Updated VOUT pin voltage in Abs Max Ratings table.	05/22
E	Updated isolation voltage on page 1. Updated V_{IOTM} and deleted V_{ISO} on page 21.	11/22
F	Updated Internal Output Voltage Feedback Circuit section on page 8.	02/23

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