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APPLICATION NOTE 4735

Quick Reference Guide for Programming the DS1873 SFP+ Controller

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Abstract: The DS1873 enhanced small form factor pluggable (SFP+) controller with digital laser diode driver (LDD) interface allows various programming options to configure the alarms, warnings, lookup tables (LUTs), and other functions. This programmability necessitates a large register memory map. The application note provides an alternate view of the register map, which is convenient when programming the device.

Introduction

The DS1873 controls and monitors all functions for small form factor (SFF), small form factor pluggable (SFP), and SFP+ modules including all SFF-8472 functionality. Six ADC channels monitor V_{CC}, temperature, and four external monitor inputs (MON1–MON4) can be used to meet all monitoring requirements. Two digital-to-analog (DAC) outputs with temperature-indexed lookup tables (LUTs) are available for additional monitoring and control functionality. To monitor these many functions, the DS1873 controller needs a large register memory map. This application note presents an alternate view of that register map.

Memory Map of the DS1873

The DS1873 features nine separate memory tables that are internally organized into eight byte rows.

The **Lower Memory** is addressed from 00h to 7Fh. It contains alarm and warning thresholds, flags, masks, several control registers, password entry area (PWE), and the Table Select byte.

Table 01h primarily contains user EEPROM (with PW1 level access), as well as alarm and warning enable bytes.

Table 02h is a multifunction space that contains configuration registers, scaling and offset values, passwords, interrupt registers, and other miscellaneous control bytes.

Table 04h contains a temperature-indexed LUT for controlling the modulation voltage. The modulation LUT can be programmed in 2°C increments over the -40°C to +102°C range.

Table 05h is empty by default. It can be configured to contain the alarm and warning enable bytes from

Table 01h, Registers F8h–FFh, with the MASK bit enabled (Table 02h, Register 89h). In this case, Table 01h will be empty.

Table 06h contains a temperature-indexed LUT that allows the automatic power control (APC) set point to change as a function of temperature to compensate for Tracking Error (TE). The APC LUT has 36 entries that determine the APC setting in 4°C windows between -40°C to +100°C.

Table 07h contains a temperature-indexed LUT for controlling DAC1. The LUT has 72 entries that determine the DAC setting in 4°C windows between -40°C to +100°C.

Table 08h contains a temperature-indexed LUT for controlling DAC2. The LUT has 36 entries that determine the DAC setting in 4°C windows between -40°C to +100°C.

Auxiliary memory (device A0h) contains 256 bytes of EEPROM accessible from address 00h–FFh. The auxiliary memory is selected with the device address of A0h.

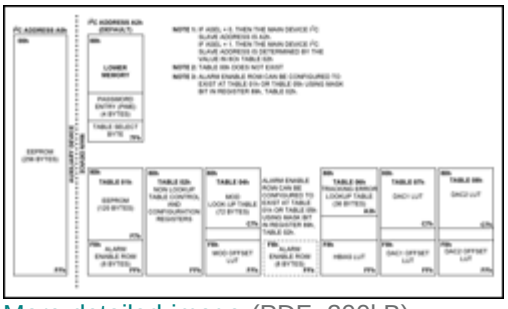
Refer to the tables below for more complete details of each byte's function and for read/write permissions for each byte.

Shadowed EEPROM

Many nonvolatile memory locations (see the **Register reference** section below) are actually shadowed EEPROM and are controlled by the SEEB bit in Table 02h, Register 80h.

The DS1873 incorporates shadowed EEPROM memory locations for key memory addresses that can be written many times. By default, the shadowed EEPROM bit, SEEB, is not set and these locations act as ordinary EEPROM. By setting SEEB these locations function like SRAM cells, which allow an infinite number of write cycles without concern for wearing out the EEPROM. Using the SEEB bit also eliminates the requirement for the EEPROM write time, t_{WR}. Because changes made with SEEB enabled do not affect the EEPROM, these changes are not retained through power cycles. The power-on value is the last value written with SEEB disabled. The SEEB function can be used to limit the number of EEPROM writes during calibration, or to change the monitor thresholds periodically during normal operation. This helps reduce the number of times that EEPROM is written. The Memory Map description below indicates which locations are shadowed EEPROM.

DS1873 Memory Map



More detailed image (PDF, 200kB)

Register Reference

The following tables provide an easy reference to the Lower Memory, and Tables 01h and 02h. For

description of the functionality for each bit, please refer to the corresponding register in the data sheet. Tables 04h through 08h are LUTs that do not require a separate reference and, hence, are not included here. Please refer to the data sheet for detailed information about these tables.

Note: RSVD is used as an acronym for "reserved."

Lower Memory

Register Name	Address (h)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
TEMP ALARM HI	00, 04	S	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
TEMP WARN HI	01, 05	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
TEMP ALARM LO	02, 06	S	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
TEMP WARN LO	03, 07	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
V_{CC} ALARM HI	08, 0C, 10, 14, 18, 1C, 20, 24, 28, 2C	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
V_{CC} WARN HI MON1–4 ALARM HI MON1–4 WARN HI	09, 0D, 11, 15, 19, 1D, 21, 25, 29, 2D	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
V_{CC} ALARM LO	0A, 0E, 12, 16, 1A, 1E, 22, 26, 2A, 2E	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
V_{CC} WARN LO MON1–4 ALARM LO MON1–4 WARN LO	0B, 0F, 13, 17, 1B, 1F, 23, 27, 2B, 2F	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
PW2 EE	30–5F	EE	EE	EE	EE	EE	EE	EE	EE
TEMP VALUE	60	S	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	61	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
V_{CC} VALUE	62, 64, 66, 68, 6A	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
MON1–4 VALUE	63, 65, 67, 69, 6B	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
RESERVED	6C, 6D	0	0	0	0	0	0	0	0
STATUS	6E	TXDS	TXDC	IN1S	RSELS	RSELC	TXF	RXL	RDYB
UPDATE	6F	TEMP RDY	V_{CC} RDY	MON1 RDY	MON2 RDY	MON3 RDY	MON4 RDY	RSVD	RSSIR
$ALARM_3$	70	TEMP HI	TEMP LO	V_{CC} HI	V_{CC} LO	MON1 HI	MON1 LO	MON2 HI	MON2 LO
$ALARM_2$	71	MON3 HI	MON3 LO	MON4 HI	MON4 LO	RSVD	RSVD	RSVD	TXFINT
$ALARM_1$	72	RSVD	RSVD	RSVD	RSVD	HBAL	RSVD	TXP	TXP

								HI	LO
$ALARM_0$	73	LOS HI	LOS LO	RSVD	RSVD	BIAS MAX	RSVD	RSVD	RSVD
$WARN_3$	74	TEMP HI	TEMP LO	V_{CC} HI	V_{CC} LO	MON1 HI	MON1 LO	MON2 HI	MON2 LO
$WARN_2$	75	MON3 HI	MON3 LO	MON4 HI	MON4 LO	RSVD	RSVD	RSVD	RSVD
RESERVED	76–7A	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
PASSWORD ENTRY	7B	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
	7C	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
	7D	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
	7E	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
TABLE SELECT	7F	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Table 01h

Register Name	Address (h)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
EEPROM	80-BF	EE	EE	EE	EE	EE	EE	EE	EE
EEPROM	C0-F7	EE	EE	EE	EE	EE	EE	EE	EE
ALARM EN_3	F8	TEMP HI	TEMP LO	V_{CC} HI	V_{CC} LO	MON1 HI	MON1 LO	MON2 HI	MON2 LO
ALARM EN_2	F9	MON3 HI	MON3 LO	MON4 HI	MON4 LO	RSVD	RSVD	RSVD	RSVD
ALARM EN_1	FA	RSVD	RSVD	RSVD	RSVD	HBAL	RSVD	TXP HI	TXP LO
ALARM EN_0	FB	LOS HI	LOS LO	RSVD	RSVD	BIAS MAX	RSVD	RSVD	RSVD
WARN EN_3	FC	TEMP HI	TEMP LO	V_{CC} HI	V_{CC} LO	MON1 HI	MON1 LO	MON2 HI	MON2 LO
WARN EN_2	FD	MON3 HI	MON3 LO	MON4 HI	MON4 LO	RSVD	RSVD	RSVD	RSVD
RESERVED	FE-FF	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Table 02h

Register Name	Address (h)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MODE	80	SEEB	RSVD	DAC1 EN	DAC2 EN	AEN	MOD EN	APC EN	BIAS EN
T INDEX	81	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
MOD DAC VALUE	82	0	0	0	0	0	0	0	2^8
	83	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
DAC1 VALUE	84	0	0	0	0	0	0	0	2^8
	85	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
									8

DAC2 VALUE	86	0	0	0	0	0	0	0	2
	87	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
UPDATE RATE	88	SEE	SEE	SEE	SEE	APC_SR_3	APC_SR_2	APC_SR_1	APC_SR^0
CNFGA	89	LOSC	RSVD	INV LOS	ASEL	MASK	INVRSOUT	RSVD	RSVD
CNFGB	8A	IN1C	INVOUT1	RSVD	RSVD	RSVD	ALATCH	QTLATCH	WLATCH
CNFGC	8B	XOVREN	RSVD	TXDM34	TXDFG	TXDFLT	TXDIO	RSSI_FC	RSSI_FF
DEVICE ADDR	8C	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
RIGHT $SHIFT_2$	8D	RSVD	RSVD	RSVD	RSVD	RSVD	$MON3C_2$	$MON3C_1$	$MON3C_0$
RIGHT $SHIFT_1$	8E	RSVD	$MON1_2$	$MON1_1$	$MON1_0$	RSVD	$MON2_2$	$MON2_1$	$MON2_0$
RIGHT $SHIFT_0$	8F	RSVD	$MON3F_2$	$MON3F_1$	$MON3F_0$	RSVD	$MON4_2$	$MON4_1$	$MON4_0$
XOVER COARSE	90	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
	91	2^7	2^6	2^5	2^4	2^3	2^2	2^1	0
V_{CC} SCALE MON1–2 SCALE	92, 94, 96, 98, 9A, 9C	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
MON3 F SCALE MON4 SCALE MON3 C SCALE	93, 95, 97, 99, 9B, 9D	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
RESERVED	9E–9F	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
XOVER FINE	A0	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
	A1	2^7	2^6	2^5	2^4	2^3	2^2	2^1	0
V_{CC} OFFSET MON1–2 OFFSET	A2, A4, A6, A8, AA, AC	S	S	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}
MON3 F OFFSET MON4 OFFSET MON3 C OFFSET	A3, A5, A7, A9, AB, AD	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
INTERNAL TEMP OFFSET	AE	S	2^8	2^7	2^6	2^5	2^4	2^3	2^2
	AF	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-7}
PW1	B0	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
	B1	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
	B2	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
	B3	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

PW2	B4	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
	B5	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
	B6	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
	B7	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
LOS RANGING	B8	RSVD	$HLOS_2$	$HLOS_1$	$HLOS_0$	RSVD	$LLOS_2$	$LLOS_1$	$LLOS_0$
COMP RANGING	B9	RSVD	$HBIAS_2$	$HBIAS_1$	$HBIAS_0$	RSVD	APC_2	APC_1	APC_0
IBIASMAX	BA	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}
ISTEP	BB	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}
HTXP	BC	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
LTXP	BD	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
HLOS	BE	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
LLOS	BF	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
PW_ENA	C0	RWTBL78	RWTBL1C	RWTBL2	RWTBL1A	RWTBL1B	WLOWER	WAUXA	WAUXB
PW_ENB	C1	RWTBL46	RTBL1C	RTBL2	RTBL1A	RTBL1B	WPW1	WAUXAU	WAUXBU
RESERVED	C2–C5	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
POLARITY	C6	RSVD	RSVD	RSVD	RSVD	MODP	BIASP	DAC1P	DAC2P
TBLSELPON	C7	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
MAN BIAS	C8	0	0	0	0	0	0	0	2^{8}
	C9	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
MAN_CNTL	CA	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	MAN_CLK
BIAS DAC	CB	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	2^{9}	2^{8}
	CC	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
RESERVED	CD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
DEVICE ID	CE	0	1	1	1	0	0	1	1
DEVICE VER	CF	DEVICE VERSION							
APC DAC	D0	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
HBIAS DAC	D1	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
RESERVED	D2–D7	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
EMPTY	D8–FF	EMPTY							

Table 04h: Registers 80h–C7h: MODULATION LUT
Table 04h, Registers F8h–FFh: MOD OFFSET LUT

Table 06h: Registers 80h–A3h: APC LUT
Table 06h, Registers F8h–FFh: HBIAS LUT

Table 07h: Registers 80h–C7h: DAC1 LUT
Table 07h, Registers F8h–FFh: DAC1 OFFSET LUT

Table 08h: Registers 80h–A3h: DAC2 LUT

Table 08h, Registers F8h–FFh: DAC2 OFFSET LUT

Related Parts		
DS1873	SFP+ Controller with Analog LDD Interface	Free Samples

More Information
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