


# 75MHZ, 3RD OVERTONE OSCILLATOR W/DUAL LVC MOS/LVTTL OUTPUTS

**ICS83032I**

## GENERAL DESCRIPTION

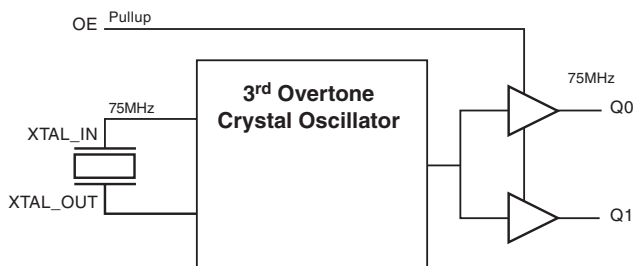


The ICS83032I is a SAS/SATA dual output LVC MOS/LVTTL oscillator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS83032I uses a 3<sup>rd</sup> overtone crystal to provide a reference frequency of 75MHz. The ICS83032I has excellent phase jitter performance, over the 900kHz - 7.5MHz integration range. The ICS83032I is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

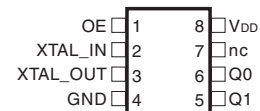
## FEATURES

- One LVC MOS/LVTTL output, 15Ω output impedance
- Crystal oscillator interface designed for 3<sup>rd</sup> overtone 75MHz crystal
- Output frequency range: 53MHz - 80MHz
- RMS phase jitter @ 75MHz (900kHz - 7.5MHz): <125fs (typical)
- 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

## BLOCK DIAGRAM



## PIN ASSIGNMENT


**ICS83032I**
**8-Lead TSSOP**

 4.40mm x 3.0mm x 0.925mm  
 package body  
**G Package**  
 Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	OE	Input	Pullup	Output enable pin. LVCMOS/LVTTL interface levels. See Table 3, Standby Function Table.
2, 3	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
4	GND	Power		Power supply ground.
5, 6	Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
7	nc	Unused		No connect.
8	V <sub>DD</sub>	Power		Power and output supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			100		kΩ
R <sub>OUT</sub>	Output Impedance	V <sub>DD</sub> = 3.6V		15		Ω
		V <sub>DD</sub> = 2.625V		TBD		Ω

TABLE 3. STANDBY FUNCTION TABLE

Control Input	Outputs	Oscillator
<b>OE</b>	<b>Q0, Q1</b>	
High (open)	fo Output Frequency	Normal Operation
Low	High Impedance	Stopped

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	101.7°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.0	3.3	3.6	V
$I_{DD}$	Power Supply Current	OE = $V_{DD}$ (output enabled)		TBD		mA

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current	OE = $V_{DD}$ (output enabled)		TBD		mA

**TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 0.3V$  OR  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{DD} = 3.3V$	-0.3		0.8	V
		$V_{DD} = 2.5V$	-0.3		0.7	V
$I_{IH}$	Input High Current	$V_{DD} = V_{IN} = 3.6V$ or $2.625V$			5	$\mu\text{A}$
$I_{IL}$	Input Low Current	$V_{DD} = 3.6V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu\text{A}$
$V_{OH}$	Output High Voltage; NOTE 1	$V_{DD} = 3.6V$	2.6			V
		$V_{DD} = 2.625V$	1.8			V
$V_{OL}$	Output Low Voltage; NOTE 1	$V_{DD} = 3.6V$ or $2.625V$			0.5	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DD}/2$ . See Parameter Measurement Information Section, "Output Load Test Circuit" diagrams.

TABLE 5. CRYSTAL CHARACTERISTICS (NOTE 1)

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		3 <sup>rd</sup> Overtone			
Frequency		53	75	80	MHz
Equivalent Series Resistance (ESR)			60		$\Omega$
Frequency Tolerance			$\pm 30$		ppm
Frequency Stability Over Operating Temperature Range			$\pm 30$		ppm
Load Capacitance ( $C_L$ ); NOTE 2			18		pF
Shunt Capacitance ( $C_O$ )				7	pF
Aging for 5 Years			$\pm 15$		ppm
Drive Level				1	mW

NOTE 1: Using an HC49/US SMD package, the parameters shown above target  $\pm 100$ ppm accuracy.

NOTE 2: See *Crystal Input Interface* in the Application Information Section.

TABLE 6A. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		53	75	80	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter, Random; NOTE 1	$f_{OUT} = 75MHz$ , (Integration Range: 900kHz-7.5MHz)		<125		fs
$t_{DJ}$	Deterministic Jitter; NOTE 2			0.2		ps
$t_{RJ}$	Random Jitter; NOTE 2			3		ps
$t_{RMS}$	RMS of Total Distribution ( $\sigma$ ); NOTE 2			3		ps
$t_{P-P}$	Peak-to-Peak Jitter; NOTE 2			25		ps
$t_{acc}$	Accumulated Jitter ( $\sigma$ ); NOTE 2	$n = 2$ to 50000 cycles		4		ps
$tsk(o)$	Output Skew; NOTE 3, 4			5		ps
$\Delta f/f_O$	Frequency Stability; NOTE 5			$\pm 10$		ppm
$t_{OSC}$	Oscillation Start Up Time				10	ms
$t_R / t_F$	Output Rise/Fall Time	20% to 80%		350		ps
odc	Output Duty Cycle			50		%

NOTE 1: Measured using Aeroflex PN9500.

NOTE 2: Measured using Wavecrest SIA-3000.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DD}/2$ .

NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

NOTE 5: This is the frequency error contributed by the oscillator and must be added to the frequency timing error from the crystal to obtain the total frequency stability. See *Frequency Stability* in the Application Information Section.

TABLE 6B. AC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		53	75	80	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter, Random; NOTE 1	$f_{OUT} = 75MHz$ , (Integration Range: 900kHz-7.5MHz)		TBD		fs
$t_{DJ}$	Deterministic Jitter; NOTE 2			0.2		ps
$t_{RJ}$	Random Jitter; NOTE 2			3		ps
$t_{RMS}$	RMS of Total Distribution ( $\sigma$ ); NOTE 2			3		ps
$t_{p-p}$	Peak-to-Peak Jitter; NOTE 2			25		ps
$t_{acc}$	Accumulated Jitter ( $\sigma$ ); NOTE 2	$n = 2$ to 50000 cycles		4		ps
tsk(o)	Output Skew; NOTE 3, 4			TBD		ps
$\Delta f/f_O$	Frequency Stability; NOTE 5			$\pm 10$		ppm
$t_{OSC}$	Oscillation Start Up Time				TBD	ms
$t_R / t_F$	Output Rise/Fall Time	20% to 80%		400		ps
odc	Output Duty Cycle			50		%

NOTE 1: Measured using Aeroflex PN9500.

NOTE 2: Measured using Wavecrest SIA-3000.

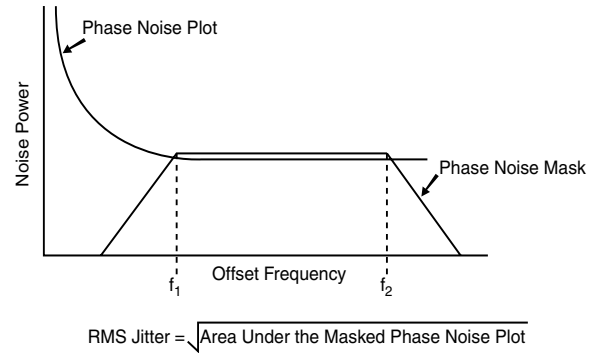
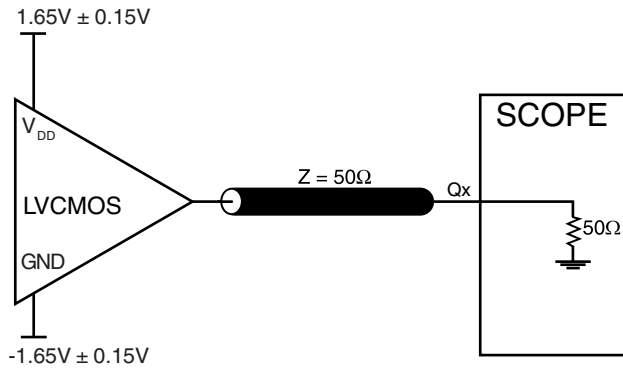
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at  $V_{DD}/2$ .

NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

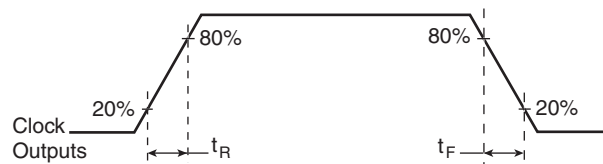
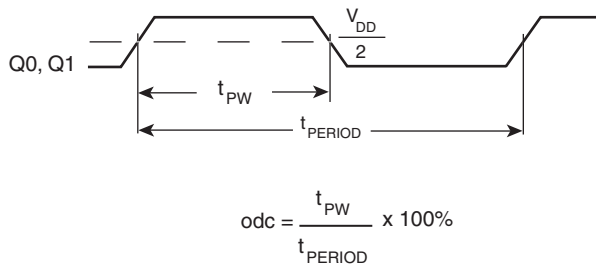
NOTE 5: This is the frequency error contributed by the oscillator and must be added to the frequency timing error from the crystal to obtain the total frequency stability. See *Frequency Stability* in the Application Information Section.

## PARAMETER MEASUREMENT INFORMATION



**3.3V OUTPUT LOAD AC TEST CIRCUIT**

**RMS PHASE JITTER**



**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**

**OUTPUT RISE/FALL TIME**

## APPLICATION INFORMATION

### FREQUENCY STABILITY

The table shown below provides a basic guideline in selecting the proper quartz crystal that meets a timing budget of  $\pm 100$ ppm. For more information on selecting the proper

crystal, see the application note, *Crystal Timing Budget and Accuracy for FemtoClock™*.

Parameter	Typical	Units
Frequency Tolerance	$\pm 30$	ppm
Frequency Stability	$\pm 30$	ppm
Aging for 5 Years	$\pm 15$	ppm
Accuracy of 3 <sup>rd</sup> Overtone Oscillator	$\pm 10$	ppm
Load Capacitance Accuracy	$\pm 3$	ppm
<b>Total Overall Timing Error</b>	<b><math>\pm 88</math></b>	<b>ppm</b>

### RECOMMENDATIONS FOR UNUSED OUTPUT PINS

#### OUTPUTS:

##### LVCMOS OUTPUT:

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 8 LEAD TSSOP

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

### TRANSISTOR COUNT

The transistor count for ICS83032I is: 83



## PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

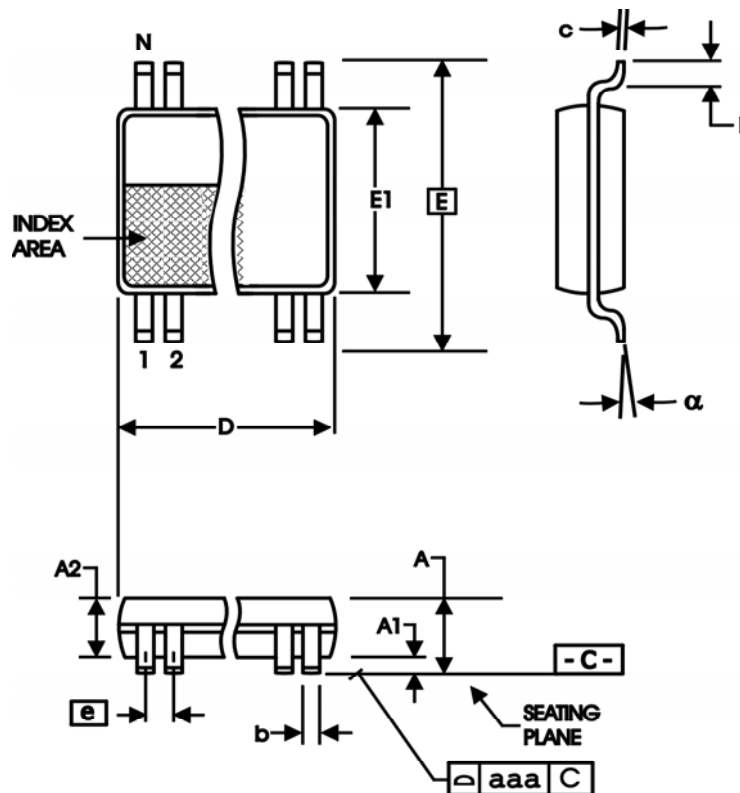


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
$\alpha$	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS83032AGI	303AI	8 lead TSSOP	tube	-40°C to 85°C
ICS83032AGIT	303AI	8 lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS83032AGILF	03AIL	8 lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS83032AGILFT	03AIL	8 lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

The aforementioned trademark, HiPerClockS is a trademark of Integrated Circuit Systems, Inc. or its subsidiaries in the United States and/or other countries.

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial and industrial applications. Any other applications such as those requiring high reliability or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.

Innovate with IDT and accelerate your future networks. Contact:

**www.IDT.com**

**For Sales**

800-345-7015  
408-284-8200  
Fax: 408-284-2775

**For Tech Support**

clockhelp@idt.com  
408-284-8200

---

**Corporate Headquarters**

Integrated Device Technology, Inc.  
6024 Silver Creek Valley Road  
San Jose, CA 95138  
United States  
800 345 7015  
+408 284 8200 (outside U.S.)

**Asia Pacific and Japan**

Integrated Device Technology  
Singapore (1997) Pte. Ltd.  
Reg. No. 199707558G  
435 Orchard Road  
#20-03 Wisma Atria  
Singapore 238877  
+65 6 887 5505

**Europe**

IDT Europe, Limited  
Prime House  
Barnett Wood Lane  
Leatherhead, Surrey  
United Kingdom KT22 7DE  
+44 1372 363 339