

## 1. General description

Planar passivated four quadrant triac in a SOT78 (TO-220AB) plastic package intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants. This very sensitive gate "series D" triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

## 2. Features and benefits

- Direct triggering from low power drivers and logic ICs
- High blocking voltage capability
- Low holding current for low current loads and lowest EMI at commutation
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate for easy logic level triggering

## 3. Applications

- General purpose motor controls
- General purpose switching

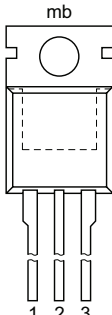
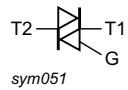
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 110\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	4	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	35	A
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	-	5	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	-	5	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	-	5	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G+; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	-	10	mA

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		 sym051
2	T2	main terminal 2		
3	G	gate		
mb	T2	mounting base; main terminal 2		

## 6. Ordering information

Table 3. Ordering information

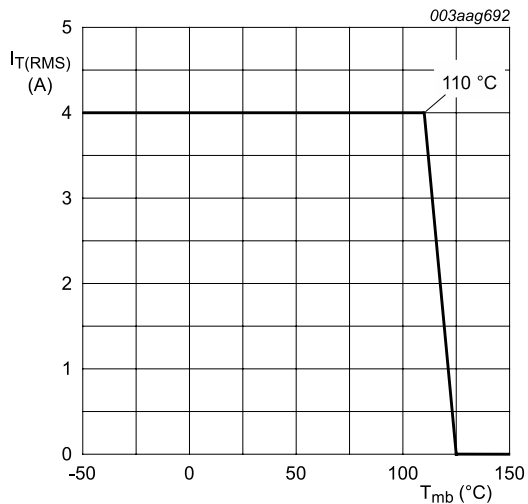
Type number	Package		
	Name	Description	Version
BTA234-800D	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

## 7. Limiting values

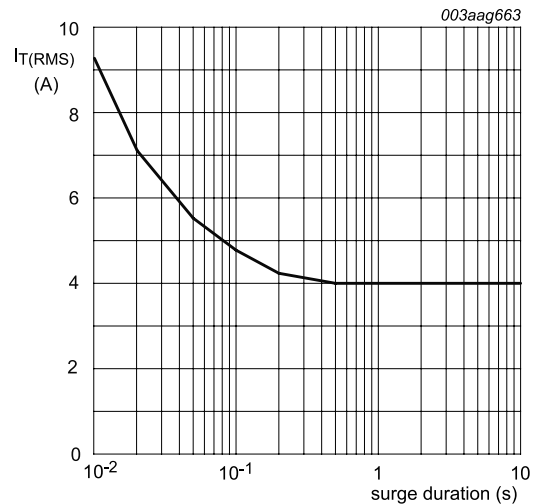
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 110\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	4	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig 4</a> ; <a href="#">Fig 5</a>	-	35	A
		full sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 16.7\text{ ms}$	-	38.5	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; sine-wave pulse	-	6.1	$A^2s$
$di_T/dt$	rate of rise of on-state current	$I_G = 10\text{ mA}$ ; T2+ G+	-	50	$A/\mu s$
		$I_G = 10\text{ mA}$ ; T2+ G-		50	$A/\mu s$
		$I_G = 10\text{ mA}$ ; T2- G-		50	$A/\mu s$
		$I_G = 20\text{ mA}$ ; T2- G+		10	$A/\mu s$
$I_{GM}$	peak gate current		-	2	A
$P_{GM}$	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
$T_{stg}$	storage temperature		-40	150	$^{\circ}C$
$T_j$	junction temperature		-	125	$^{\circ}C$



**Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values**



$f = 50\text{ Hz}$ ;  $T_{mb} = 110\text{ °C}$

**Fig. 2. RMS on-state current as a function of surge duration; maximum values**

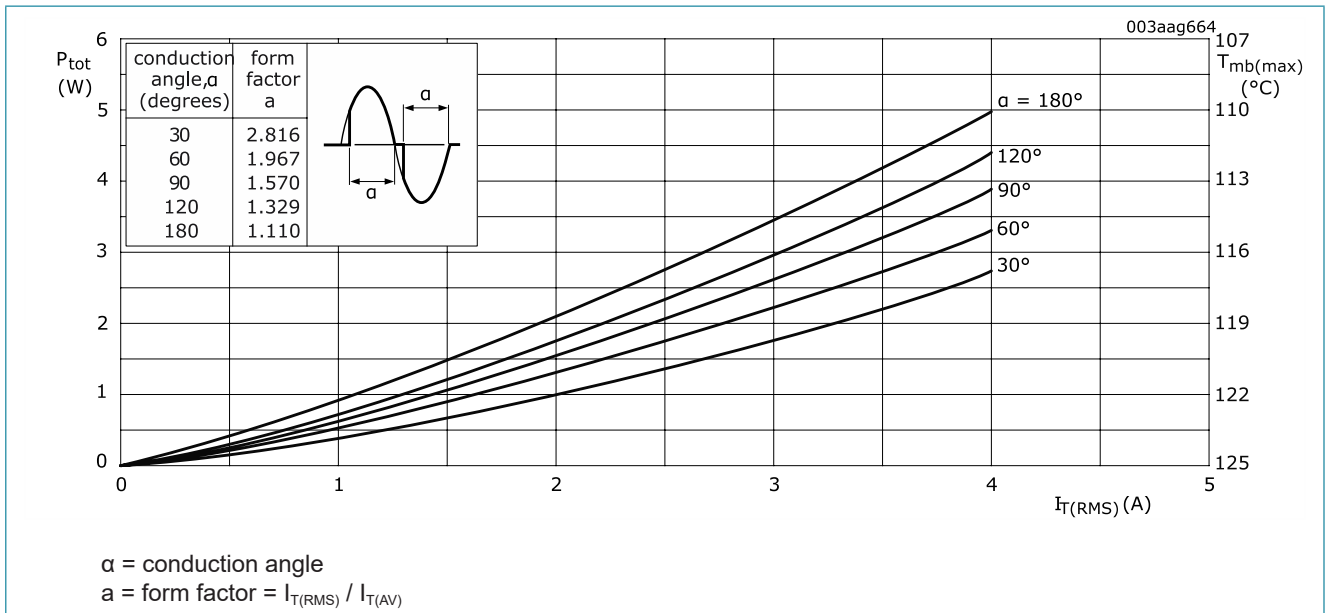


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

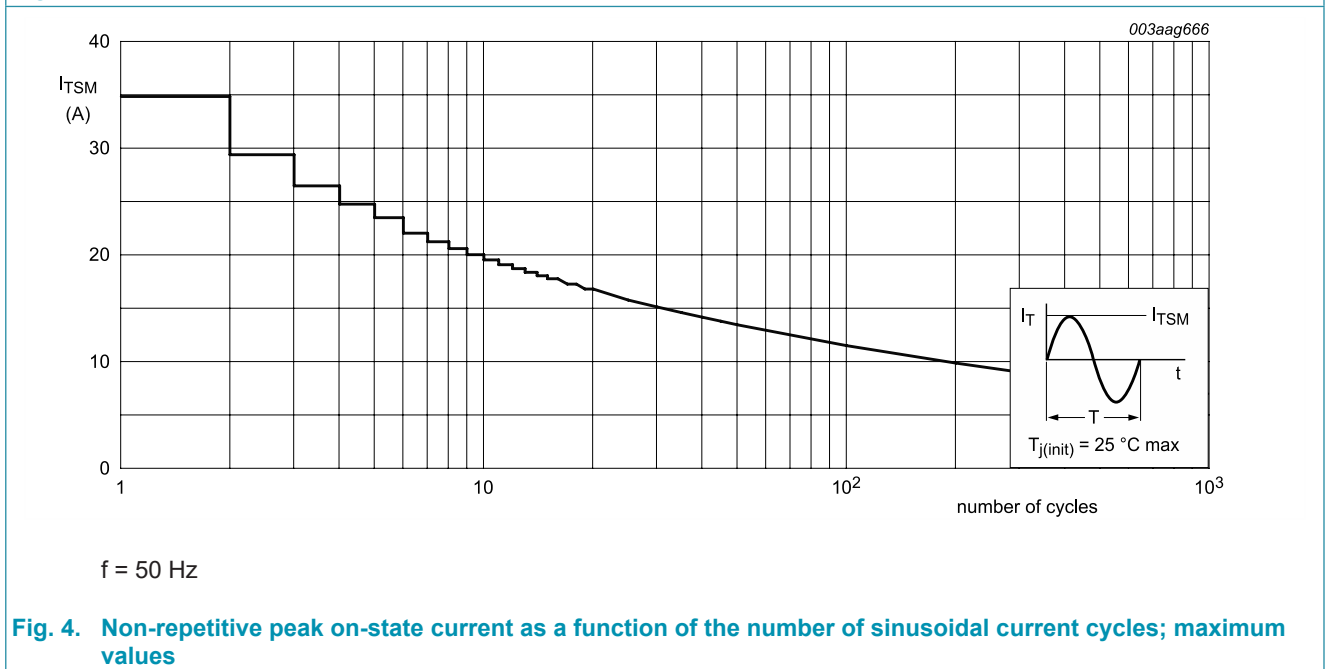


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

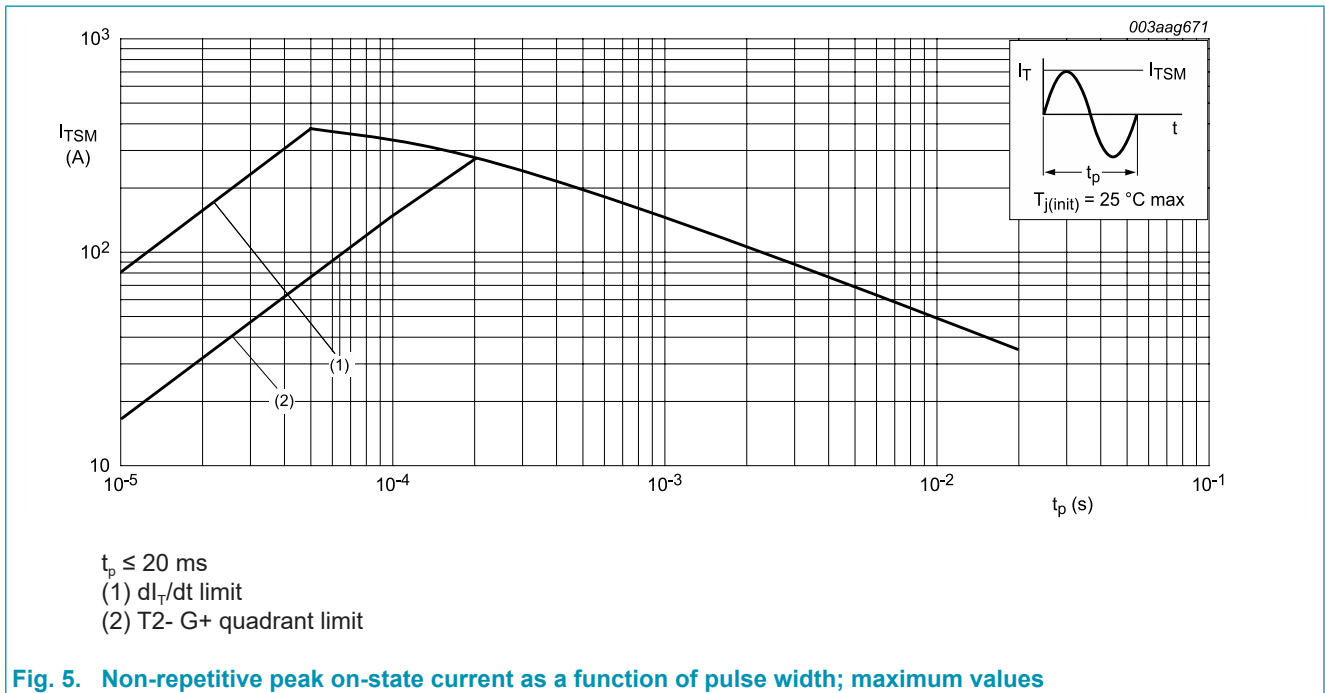


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

## 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; <a href="#">Fig. 6</a>	-	-	3.7	K/W
		half cycle; <a href="#">Fig. 6</a>	-	-	3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	60	-	K/W

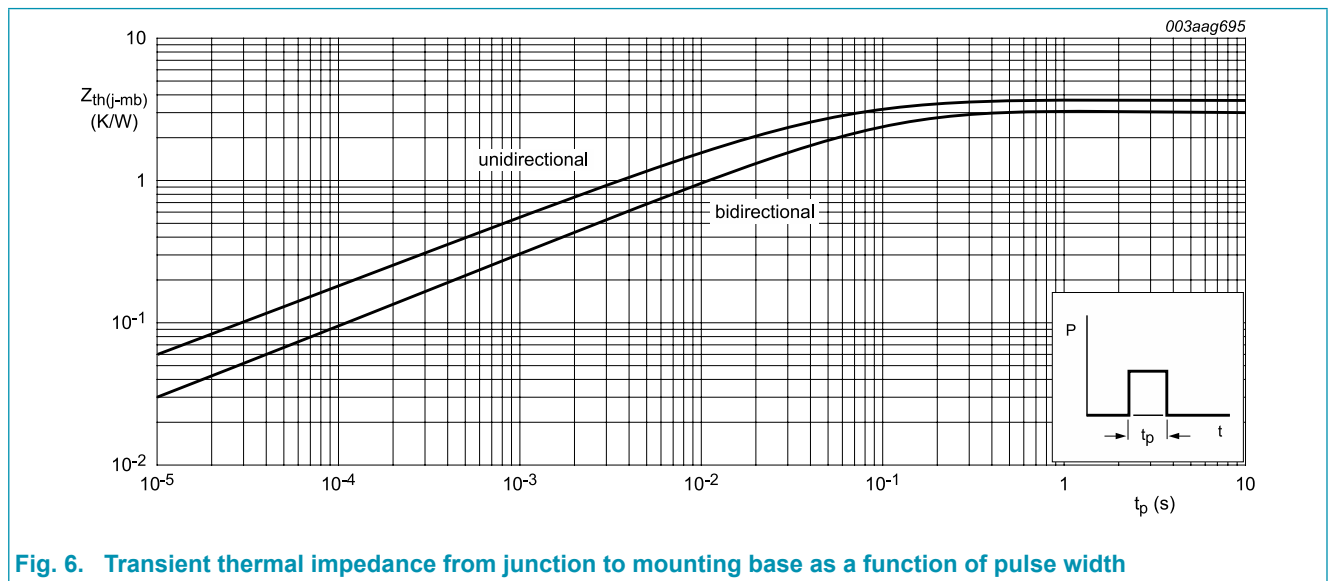
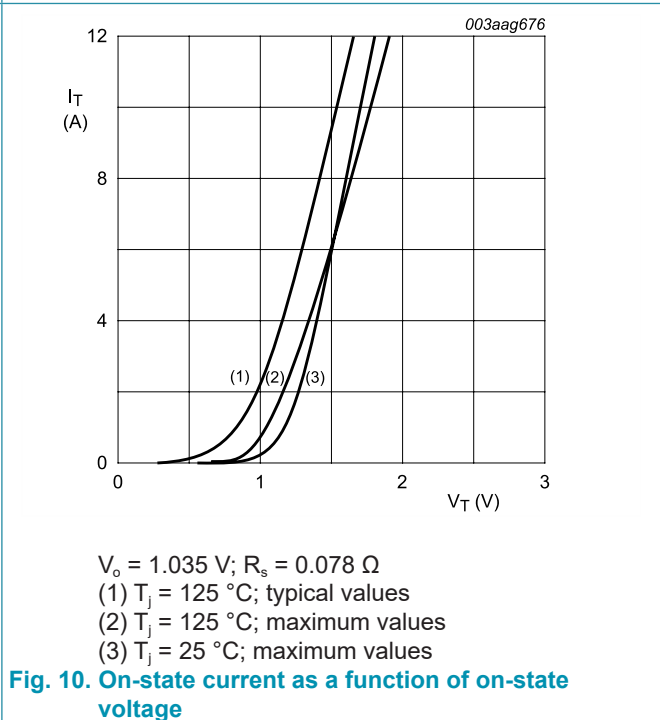
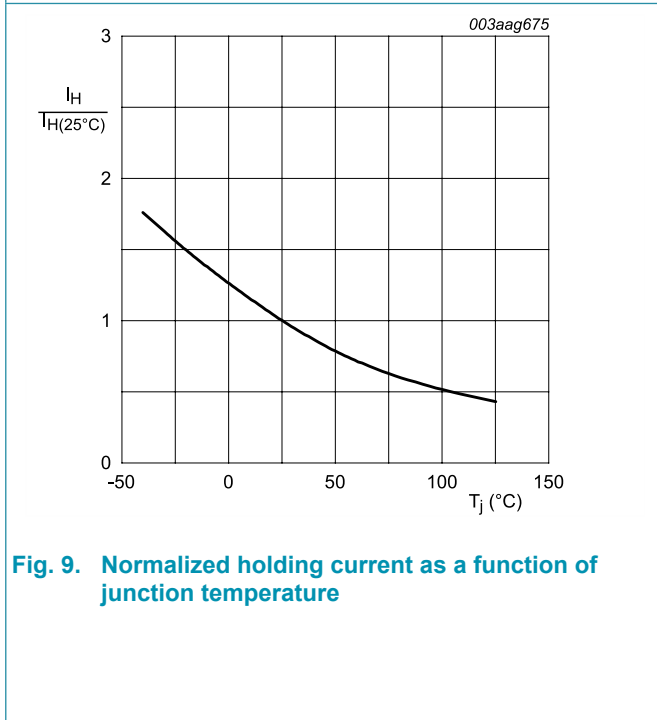
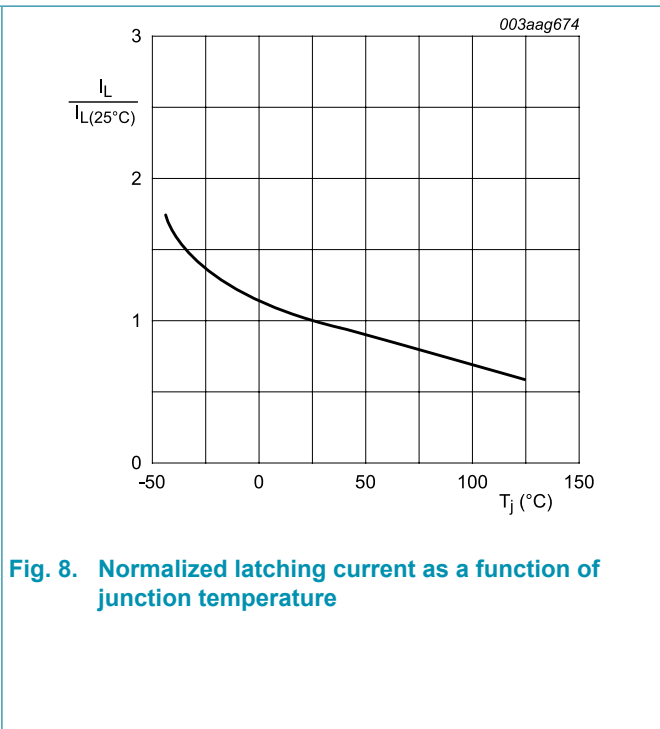
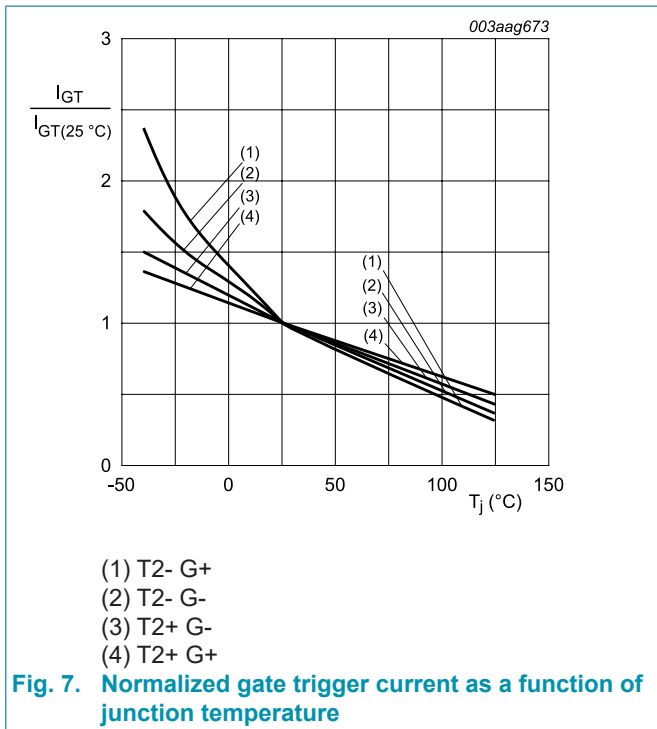


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2+ G+;$ $T_J = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>	-	-	5	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2+ G-;$ $T_J = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>	-	-	5	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2- G-;$ $T_J = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>	-	-	5	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2- G+;$ $T_J = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>	-	-	10	mA
$I_L$	latching current	$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_2+ G+;$ $T_J = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 8</a>	-	-	10	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_2+ G-;$ $T_J = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 8</a>	-	-	15	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_2- G-;$ $T_J = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 8</a>	-	-	10	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_2- G+;$ $T_J = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 8</a>	-	-	10	mA
$I_H$	holding current	$V_D = 12\text{ V}; T_J = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 9</a>	-	-	6	mA
$V_T$	on-state voltage	$I_T = 6\text{ A}; T_J = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	-	1.3	1.5	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_J = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	-	0.7	1	V
		$V_D = 800\text{ V}; I_T = 0.1\text{ A}; T_J = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	0.25	0.4	-	V
$I_D$	off-state current	$V_D = 800\text{ V}; T_J = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}; T_J = 125\text{ }^\circ\text{C}; (V_{DM} = 67\%$ of $V_{DRM});$ exponential waveform; gate open circuit	-	50	-	V/ $\mu$ s
$dI_{com}/dt$	rate of change of commutating current	$V_D = 400\text{ V}; T_J = 125\text{ }^\circ\text{C}; I_{T(RMS)} = 4\text{ A};$ $dV_{com}/dt = 20\text{ V}/\mu\text{s};$ (snubberless condition); gate open circuit	-	1.2	-	A/ms
$t_{gt}$	gate-controlled turn-on time	$I_{TM} = 6\text{ A}; V_D = 800\text{ V}; I_G = 0.1\text{ A};$ $dI_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	$\mu$ s





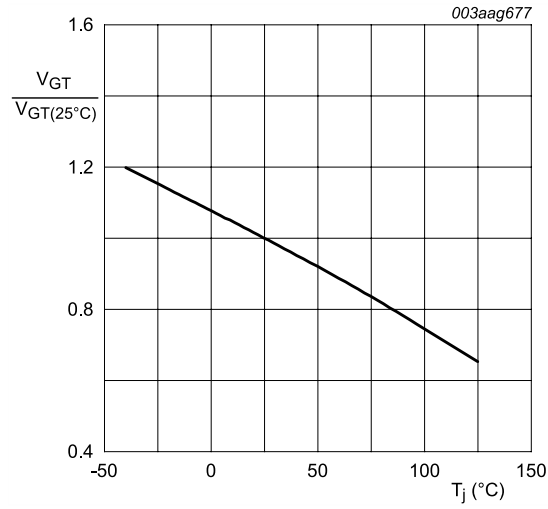
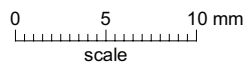


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

### 10. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



**DIMENSIONS** (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub> ( <sup>2</sup> )	b <sub>2</sub> ( <sup>2</sup> )	c	D	D <sub>1</sub>	E	e	L	L <sub>1</sub> ( <sup>1</sup> )	L <sub>2</sub> ( <sup>1</sup> ) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

**Notes**

- Lead shoulder designs may vary.
- Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT78		3-lead TO-220AB	SC-46		08-04-23 08-06-13

## 11. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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