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Keywords: HSTL, PECL, high speed, interface standards, differential HSTL, high speed transceiver logic, Jedec standard, Jedec std, differential

APPLICATION NOTE 1752

Applying HSTL Signals to PECL Input Devices

Feb 18, 2003

Abstract: This application note discusses the conditions for interfacing differential HSTL (High-Speed Transceiver Logic) outputs to PECL (Positive Emitter Coupled Logic) inputs.

PECL and HSTL are two of the high-speed interface standards in common use. PECL (positive supply referred ECL) is an older standard than HSTL and was developed as a higher speed alternative to the TTL logic standards. HSTL was defined as an interface standard for digital integrated circuits. The two standards are not directly compatible. Some PECL devices can receive differential HSTL signals but careful examination of the HSTL output specifications and PECL input specifications is needed in order to guarantee operation. Typically, such PECL devices can only receive HSTL signals that have been transmitted over a short distance. This application note describes the specification criteria required for direct connection of ICs with HSTL compliant outputs to devices with PECL inputs.

What is HSTL?

High-Speed Transceiver Logic (HSTL) is a 1.5V output buffer supply referenced interface standard for digital integrated circuits. HSTL can be implemented in both single ended and differential forms and is intended to be a technology independent standard, suitable for use with CMOS and Bipolar ICs. Jedec Standard EIA/JESD8-6 describes the functional and parametric constraints required for HSTL compliance.

EIA/JESD8-6 describes a nominal 1.5V output buffer supply voltage (V_{ddq}) based interface in which V_{ddq} is independent of the main IC supply voltage. The HSTL input reference voltage (V_{ref}) is nominally half of V_{ddq} . Single-ended HSTL input and output levels are then defined in relation to V_{ref} and V_{ddq} . Further, EIA/JESD8-6 defines both DC and AC input and output levels as a means of guaranteeing performance under AC conditions. **Figure 1** shows the HSTL I/O levels in diagrammatic form. Table 1 tabulates some key HSTL input and output specifications.

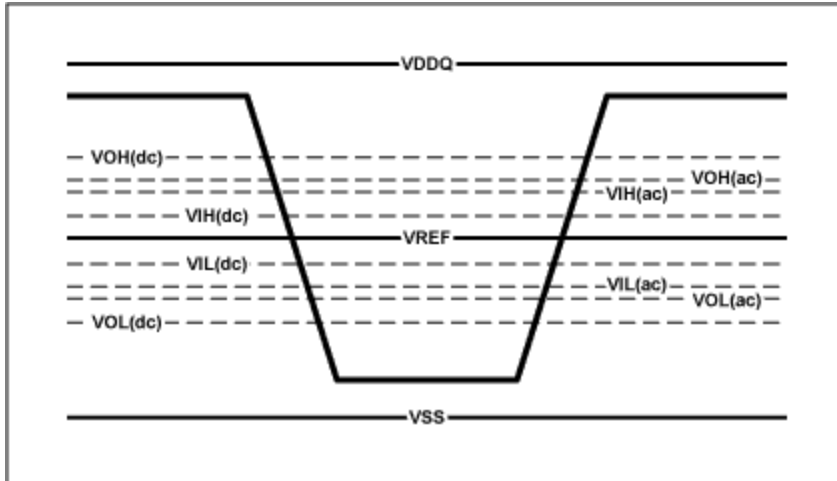


Figure 1. HSTL I/O levels.

Table 1. Key HSTL input and output specifications.

Symbol	Parameter	Min	Typ	Max	Units	Comments
V _{DD}	Device supply voltage	N/A		N/A	V	Not specified/not restricted.
V _{DDQ}	Output supply voltage	1.4	1.5	1.6	V	
V _{REF}	Input reference voltage	0.68	0.75	0.90	V	
V _{IH} (DC)	DC input logic high	V _{REF} +0.10		V _{DDQ} +0.3	V	
V _{IL} (DC)	DC input logic low	-0.30		V _{REF} - 0.10	V	
V _{IH} (AC)	AC input logic high	V _{REF} +0.20			V	
V _{IL} (AC)	AC input logic low			V _{REF} -0.20	V	
V _{DIF} (DC)	DC differential input	0.20		V _{DDQ} +0.60	V	
V _{DIF} (AC)	AC differential input	0.40		V _{DDQ} +0.60	V	
V _{OH} (DC)	DC output logic high	V _{DDQ} -0.4			V	Note 1
V _{OL} (DC)	DC output logic low			0.4	V	Note 1
V _{OH} (AC)	AC output logic high	V _{DDQ} -0.5			V	Note 1
V _{OL} (AC)	AC output logic low			0.5	V	Note 1

*Note 1. Output voltage load condition depends on output configuration and load type. Four configurations are covered by the JESD8-6 standard with minimum load currents in the range 8mA to 24mA.

What is PECL?

Positive Emitter Coupled Logic (PECL) is a positive supply rail referred high-speed transmission standard that has been optimized for use in bipolar IC technology. PECL is essentially the same standard as Emitter Coupled Logic (ECL). The power supplies for ECL systems are ground and a negative supply voltage (V_{EE}). ECL inputs and outputs are ground referred. PECL systems operate from a positive supply (V_{CC}) and ground. PECL inputs and outputs are V_{CC} referred. In most cases PECL and ECL devices are interchangeable.

Figure 2 illustrates a simplified PECL input stage comprising a differential pair (Q1, Q2) and a tail current source (I). The input transistors will switch depending on the relative voltages at the inputs IN+ and IN-. If IN+ is at a more positive voltage than IN-, Q1 will turn on and Q2 will turn off. The converse is true if IN- is more positive than IN+. A differential signal of only a few milli-volts is typically required to switch the input transistors although a larger voltage than this is required to guarantee the device output levels quoted in a datasheet. Most PECL datasheets specify a differential input voltage (V_{ID}) of at least 100mV to guarantee the specified output levels. Figure 4 shows example data sheet values for a PECL input stage with a V_{ID} range of 100mV to 3V.

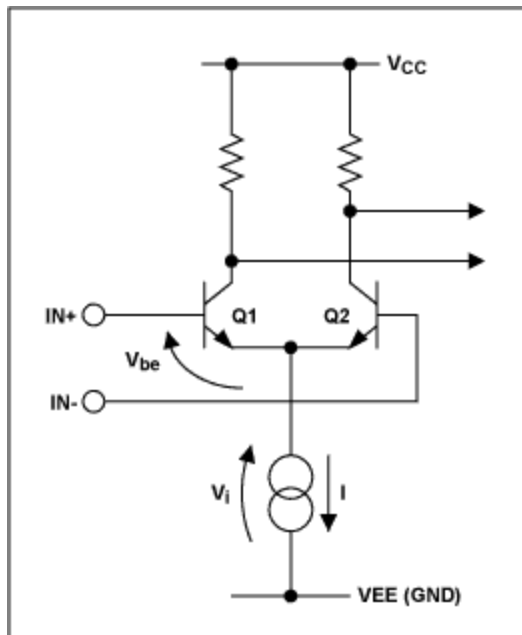


Figure 2. Simplified PECL input stage.

There are additional restrictions placed on the absolute voltages applied at inputs IN+ and IN-. These are the differential input high and low voltage ranges. On older PECL devices the input voltage ranges were limited to the requirements of the various PECL specifications. Many newer devices have extended input ranges allowing some flexibility in the input signal specification. The differential input low voltage (V_{ILD}) range on Maxim PECL parts often includes the negative supply voltage. Referring to Table 2, transistor Q2 is turned off in the case when IN- is low with respect to IN+. Decreasing the voltage on IN- further does not change this situation, nor does it degrade the input stage response characteristics in a properly designed circuit. A suitable input circuit will therefore accept V_{ILD} values which include V_{EE} .

The turned on transistor, Q1 in this case, is not so fortunate. In order for Q1 to remain on there must be sufficient voltage at IN+ both to supply Q1's base emitter voltage drop (V_{be}) and the minimum operating voltage across the current source (V_i). This places a limit on the differential input high voltage (V_{IHD}). The datasheet example shown in Table 2 specifies a minimum V_{IHD} of $V_{EE} + 1.2V$, which is the minimum voltage required to maintain Q1 and the tail current source within normal operating parameters.

A further consideration is the input stage behavior during switching. For an ideal input signal the value of V_{IHD} drops to the input signal crossing (differential zero) point and rises again to the V_{OH} level as the input signal changes state. The precise input stage behavior under these circumstances is complex and is dependent on the input edge rate and various internal time constants within the PECL device. For edge rates below approximately 1ns ($V_{IHD} < V_{IHD}(\min)$ for less than 1ns) there should be no noticeable effect on the PECL device response. For edge rates much greater than 1ns a pulse skew effect should

be observed at the PECL device outputs (pulse skew is the effect seen when one output of a differential pair starts to transition before the other).

Table 2. Example PECL data sheet input specification.

Parameter	Symbol	40°C		25°C		+85°C		Units
		Min	Max	Min	Max	Min	Max	
Differential Input High Voltage	V _{IHD}	V _{EE} +1.2	V _{CC}	V _{EE} +1.2	V _{CC}	V _{EE} +1.2	V _{CC}	V
Differential Input Low Voltage	V _{ILD}	V _{EE}	V _{CC} - 0.100	V _{EE}	V _{CC} - 0.100	V _{EE}	V _{CC} - 0.100	V
Differential Input Voltage	V _{ID}	0.100	3.0	0.100	3.0	0.100	3.0	V
Input Current	I _{IH} , I _{IL}	-100	100	-100	100	-100	100	μA

Conditions for Compatibility Between Differential HSTL Outputs and PECL Inputs

Three basic criteria determine the compatibility of a particular differential HSTL output and PECL input. These are the differential voltage (V_{OH}-V_L/V_{ID}), differential voltage low level (V_L/V_{ILD}) and differential voltage high level (V_{OH}/V_{IHD}). In each case the condition for compatibility is that the minimum value of the HSTL output parameter must be greater than the minimum value of the corresponding PECL input parameter.

Expressed as inequality statements the three criteria are:

- (V_{OH}-V_L) min (HSTL) >= V_{ID} min (PECL)
- V_L min (HSTL) >= V_{ILD} min (PECL)
- V_{OH} min (HSTL) >= V_{IHD} min (PECL)

Figure 3 illustrates these conditions for compatibility in the form of a signal trace.

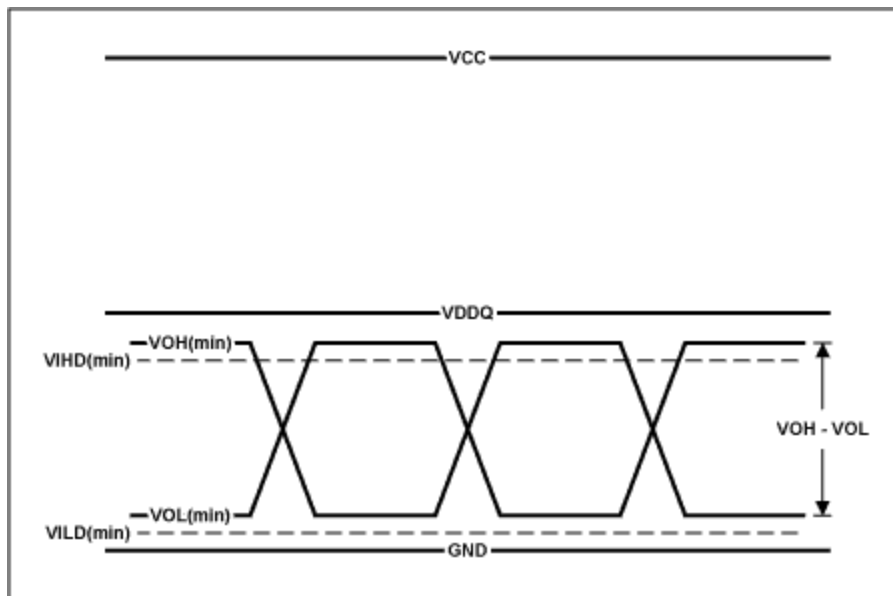


Figure 3. Conditions for compatibility between differential HSTL output and PECL input.

Of the three conditions indicated above the limiting factor is usually the relationship between the $V_{IHD}(\min)$ and $V_{OH}(\min)$ specifications for the PECL input and HSTL output respectively. This is because of the limitations imposed on $V_{IHD}(\min)$ by the structure of the PECL input stage. PECL device datasheets that indicate input compatibility with differential HSTL signals generally do so on the basis of having specified values for $V_{ILD}(\min)$ of V_{EE} (GND) and $V_{IHD}(\min)$ of no more than $V_{EE} + 1.2V$ (1.2V). Careful examination of the transmitter's HSTL output specification is still required as some devices may not be suitable for driving the specified PECL V_{IHD} levels.

Conditions for Compatibility Between Single-ended HSTL Outputs and PECL Inputs

Single-ended HSTL signals typically swing about a reference voltage of approximately 0.75V. An ideal single ended receiver would switch as the HSTL signal transitions through the 0.75V reference point. A differential input would be configured as an ideal receiver by connecting the single ended signal to one input, and applying a 0.75V reference to the other. The input stage shown in Figure 3 would be configured as a non-inverting single ended receiver by connecting the incoming signal to $IN+$ and applying the reference to $IN-$. In this situation the (differential) input stage sees a high level equal to V_{OH} when the input is high and V_{REF} when the input is low. For a PECL input stage to perform as an ideal single ended receiver the specified value for $V_{IHD}(\min)$ would have to be less than or equal to the reference voltage V_{REF} . This situation is illustrated in Figure 4. Limitations on the differential voltage and differential voltage low level specifications apply as with the differential signaling case except that the differential voltage is given by the relationship between the signal high and low levels and V_{REF} .

The resulting criteria are:

- $(V_{OH} - V_{REF}) \min (\text{HSTL}) \geq V_{ID} \min (\text{PECL})$
- $(V_{REF} - V_{OL}) \min (\text{HSTL}) \geq V_{ID} \min (\text{PECL})$
- $V_{OL} \min (\text{HSTL}) \geq V_{ILD} \min (\text{PECL})$
- $V_{REF} \min \geq V_{IHD} \min (\text{PECL})$

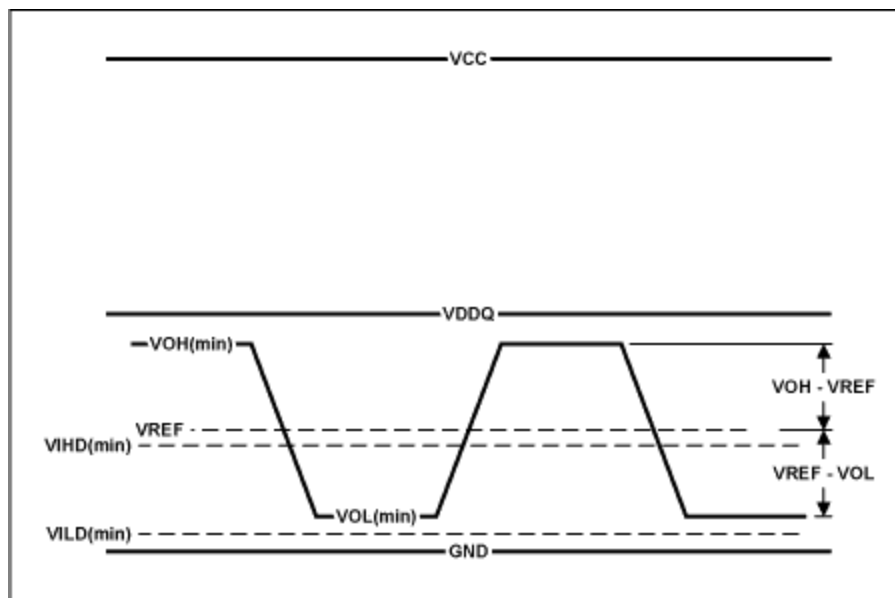


Figure 4. Conditions for compatibility between single ended HSTL output and PECL input.

PECL input devices generally cannot receive single-ended HSTL compliant signals. In some cases it may be possible to configure the PECL input with a reference voltage somewhat higher would be required for ideal receiver behavior. This would result in some pulse width distortion depending on the

transition time and frequency of the HSTL signal. In most cases a resistive level shift network which biases the signal towards Vcc would be required to guarantee operation.

Conclusion

The HSTL and PECL interface standards are not directly compatible. Some PECL devices can receive differential HSTL signals but generally cannot receive single ended HSTL signals. The PECL input specification parameters that determine a device's suitability to receive HSTL are the differential input voltage (VID), the differential input low voltage (VILD) and the differential input high voltage (VIHD). The corresponding HSTL output specification parameters are the differential output voltage (VOH-VOL), the output low voltage (VOL) and the output high voltage (VOH). Careful examination of the device data sheets is generally needed in order to assure compatibility between the HSTL output and the PECL input.

Related Parts		
MAX9310	1:5 Clock Driver with Selectable LVPECL Inputs and LVDS Outputs	
MAX9311	1:10 Differential LVPECL/LVECL/HSTL Clock and Data Drivers	Free Samples
MAX9312	Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers	
MAX9313	1:10 Differential LVPECL/LVECL/HSTL Clock and Data Drivers	Free Samples
MAX9314	Dual 1:5 Differential LVPECL/LVECL/HSTL Clock and Data Drivers	
MAX9315	1:5 Differential LVPECL/LVECL/HSTL Clock and Data Driver	Free Samples
MAX9316	1:5 Differential LVPECL/LVECL/HSTL Clock and Data Driver	
MAX9317	Dual 1:5 Differential Clock Drivers with LVPECL Inputs and LVDS Outputs	
MAX9320	1:2 Differential LVPECL/LVECL/HSTL Clock and Data Drivers	Free Samples
MAX9321	Differential LVPECL/LVECL/HSTL Receiver/Drivers	
MAX9322	LVECL/LVPECL 1:15 Differential Divide-by-1/Divide-by-2 Clock Driver	
MAX9325	2:8 Differential LVPECL/LVECL/HSTL Clock and Data Driver	Free Samples
MAX9326	1:9 Differential LVPECL/LVECL/HSTL Clock and Data Driver	

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APPLICATION NOTE 1752, AN1752, AN 1752, APP1752, Appnote1752, Appnote 1752

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