

1

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A

A

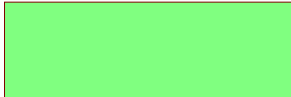
U_FPGA
FPGA.SchDoc



U_SODIMM
SODIMM.SchDoc



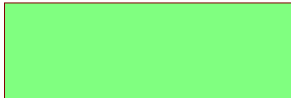
U_CLOCK
CLOCK.SchDoc



U_POWER
POWER.SchDoc



U_CONN
CONN.SchDoc



U_CPLD
CPLD.SchDoc



B

B

C

C

PM1

PM2

PM3



FIDU-DOT - small

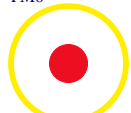
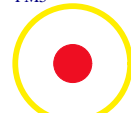
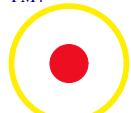
FIDU-DOT - small

FIDU-DOT - small

PM4

PM5

PM6

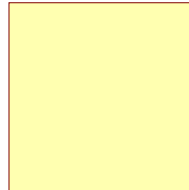


FIDU-DOT - small

FIDU-DOT - small

FIDU-DOT - small

Front Bracket screw head on Top
MECH1



Slotblende Ndigo xTDC4 Lemo

Front Bracket screw head on Bottom
MECH2



TEF1001 PCIe Frontplate

Serial
Serialnumber 6,3 x 6.3mm

LOGO1

TE Logo PRINT Layer

LOGO PRINT



Title: TEF1001 - MAIN		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 1 of 33
Filename: TEF1001.SchDoc		

1

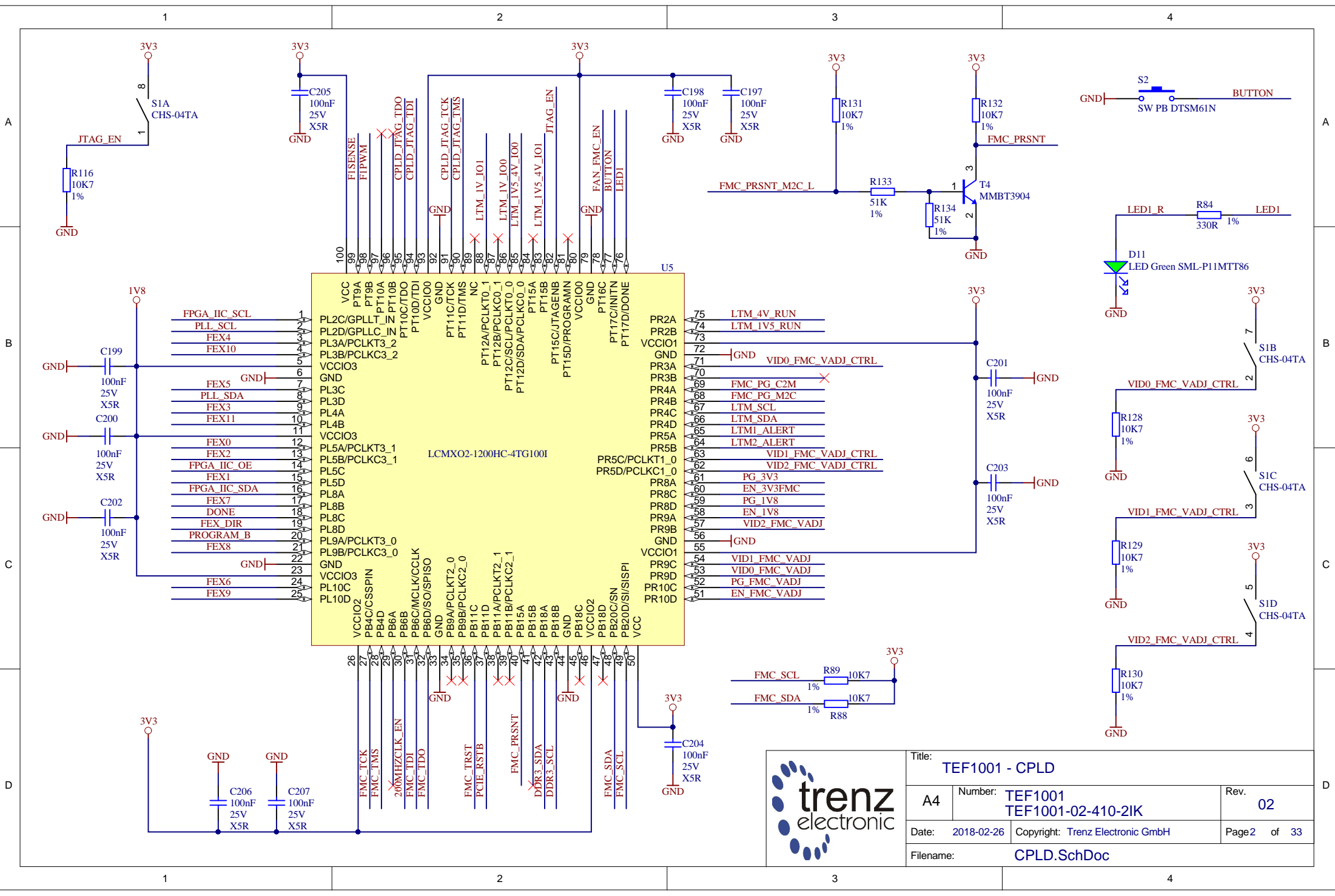
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3

4

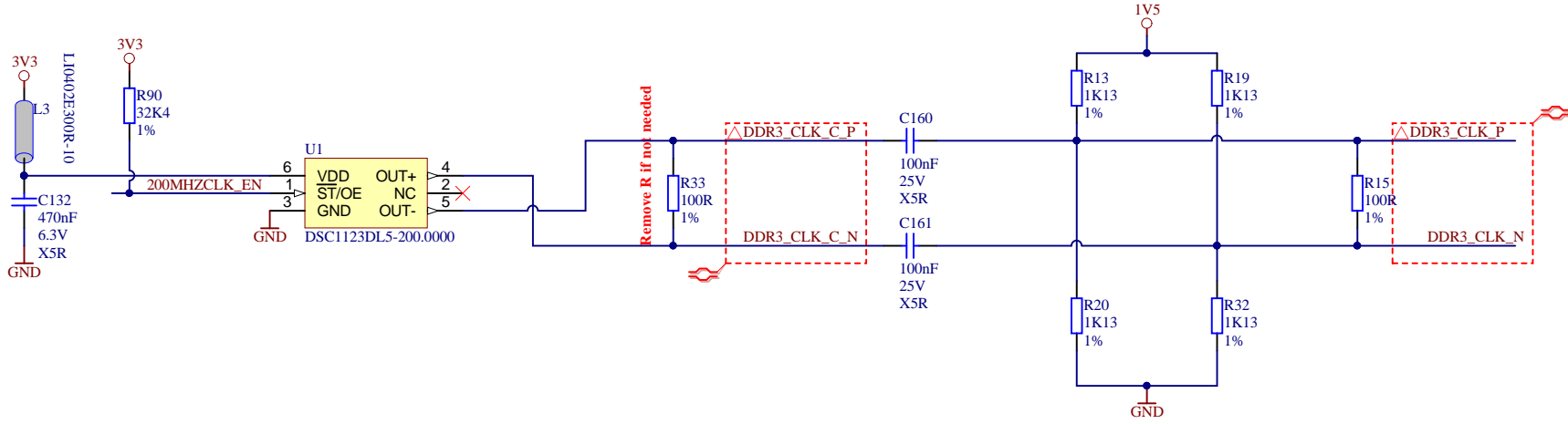
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D

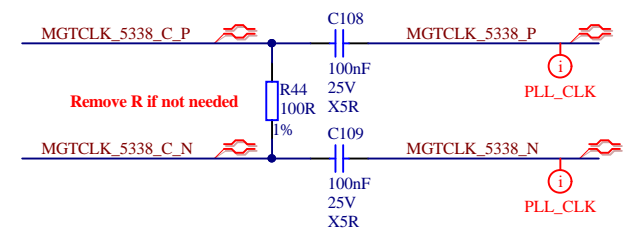
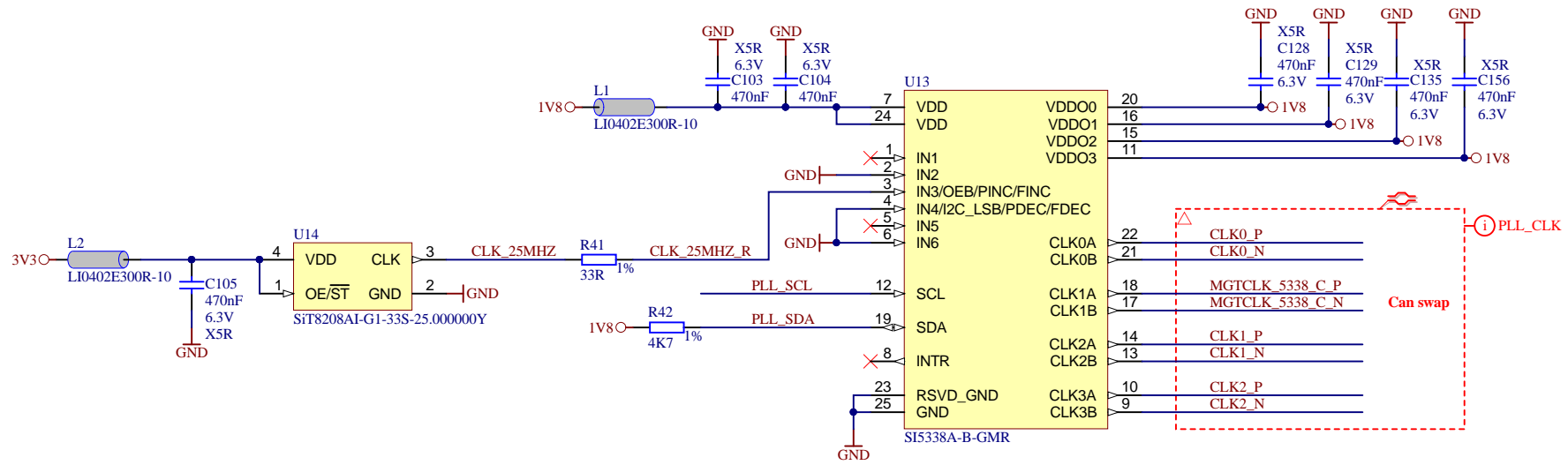


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A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 2 of 33
Filename: CPLD.SchDoc		

U_CLK-SI5338
 CLK-SI5338.SchDoc



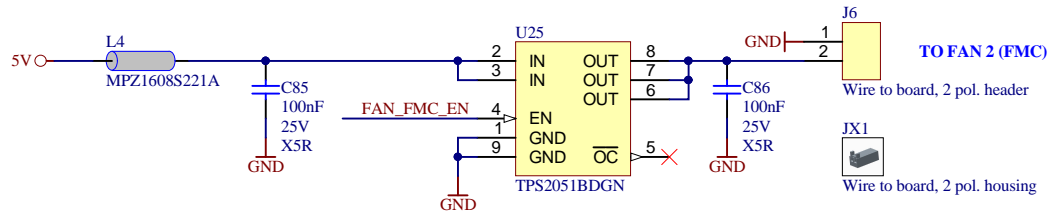
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	A4	Number: TEF1001 TEF1001-02-410-2IK
	Date: 2018-02-26	Rev. 02
	Copyright: Trenz Electronic GmbH	Page 3 of 33
Filename: CLOCK.SchDoc		



Title: TEF1001 - CLK-SI5338		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 4 of 33
Filename: CLK-SI5338.SchDoc		

U_FMC
FMC.SchDoc

U_PCIE_CONN
PCIE_CONN.SchDoc



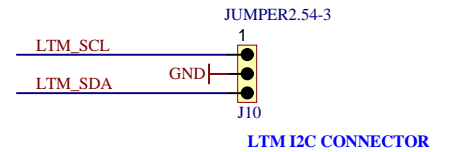
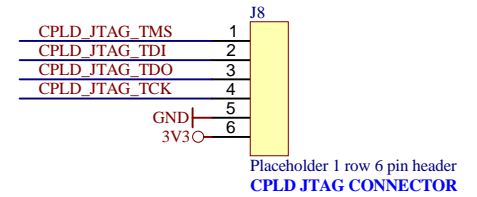
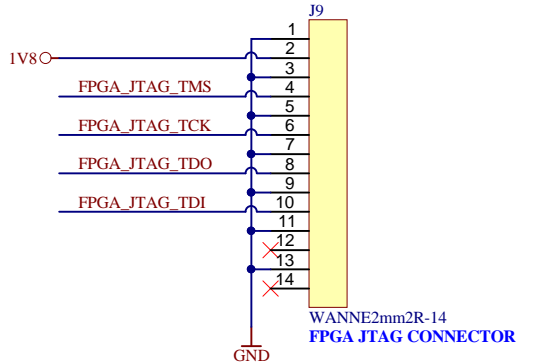
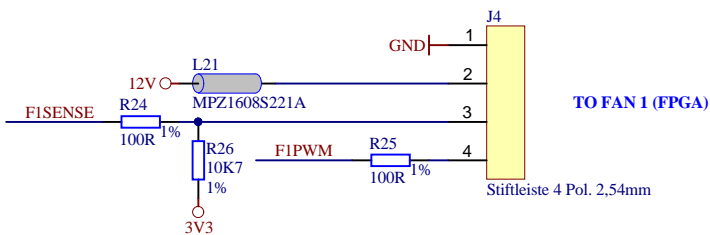
Wire to board, 2 pol. housing



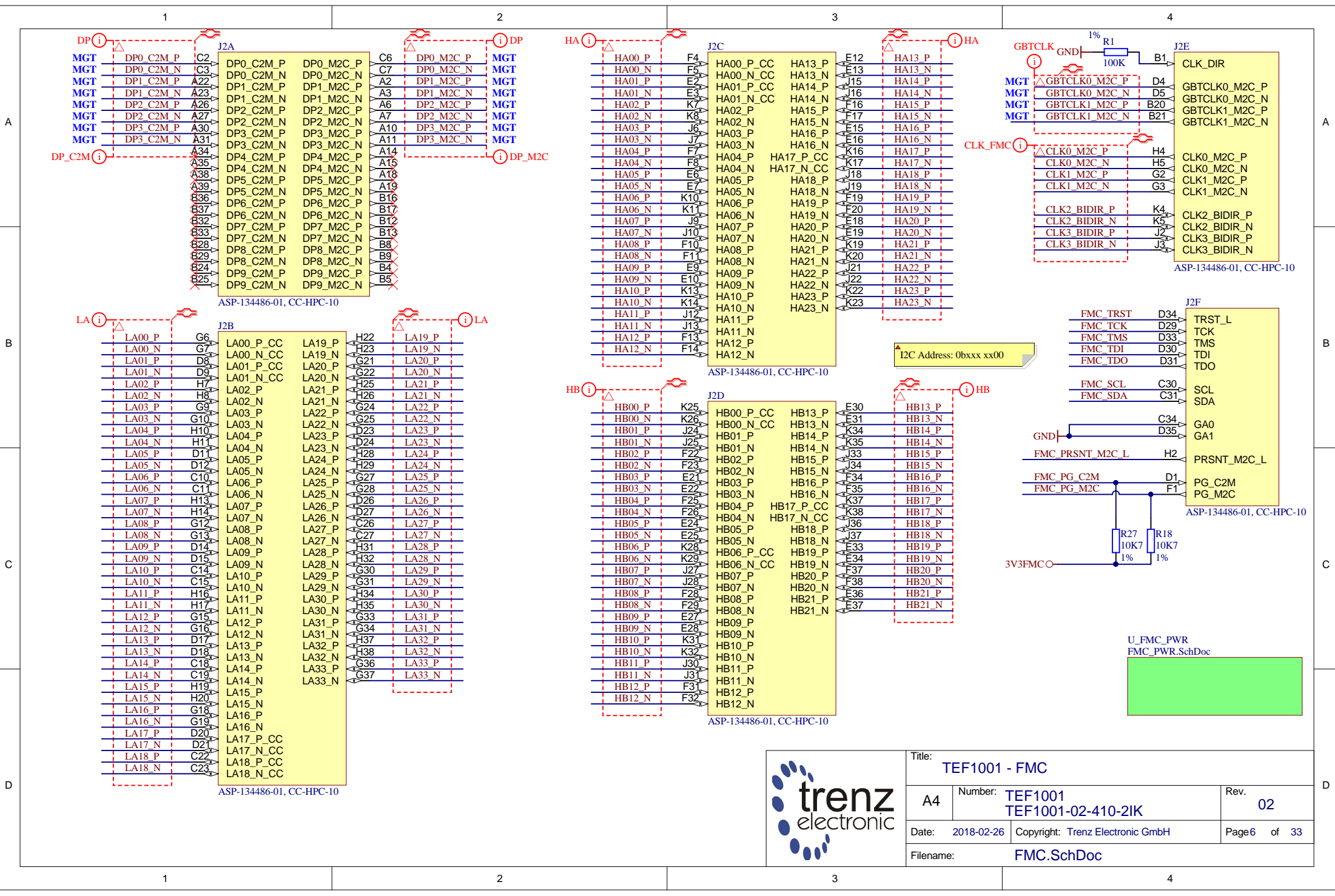
Crimp Terminal 4809, 22-30 AWG




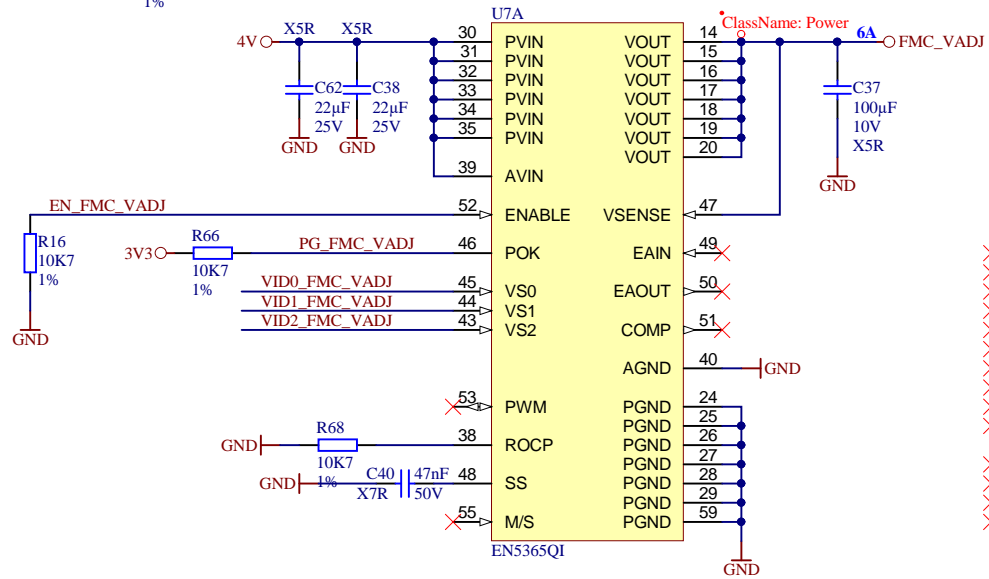
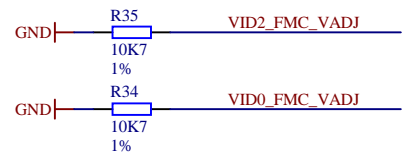
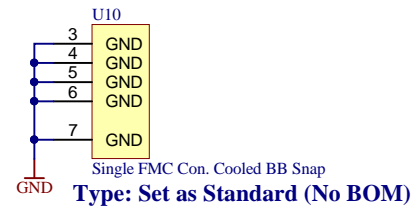
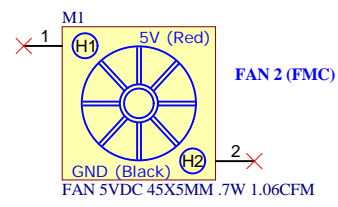
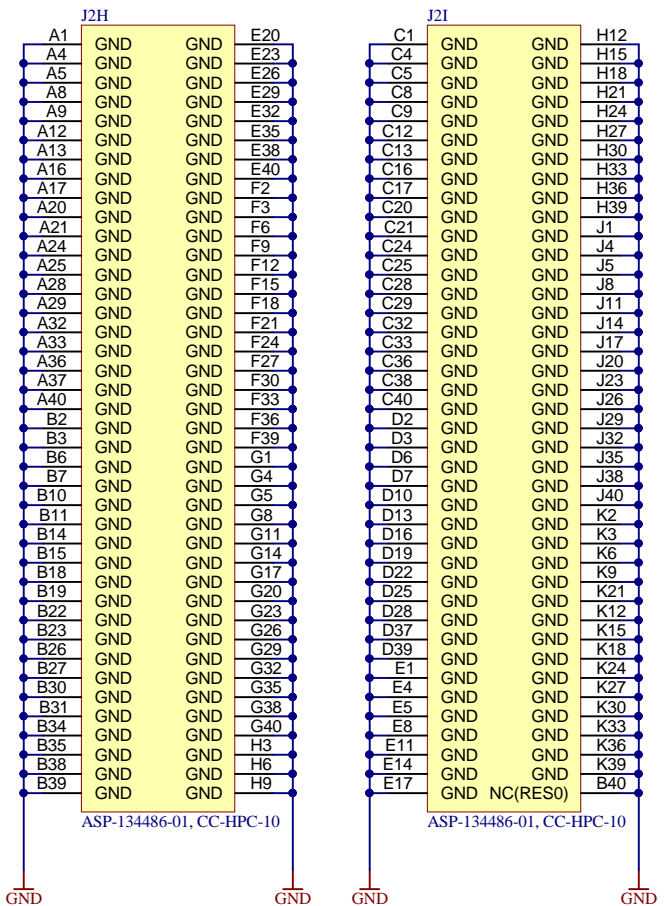
Crimp Terminal 4809, 22-30 AWG



Title: TEF1001 - CONN		
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Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 5 of 33
Filename: CONN.SchDoc		

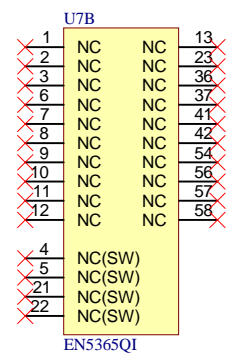
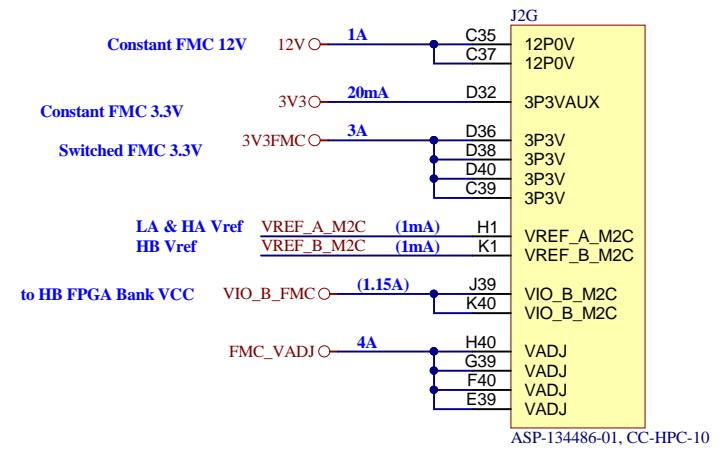


			Title: TEF1001 - FMC	
			A4	Number: TEF1001 TEF1001-02-410-2IK
Date: 2018-02-26		Copyright: Trenz Electronic GmbH		Page 6 of 33
Filename: FMC.SchDoc				

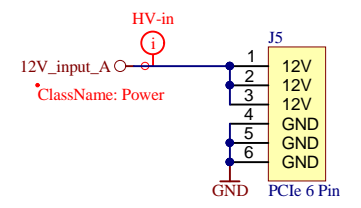
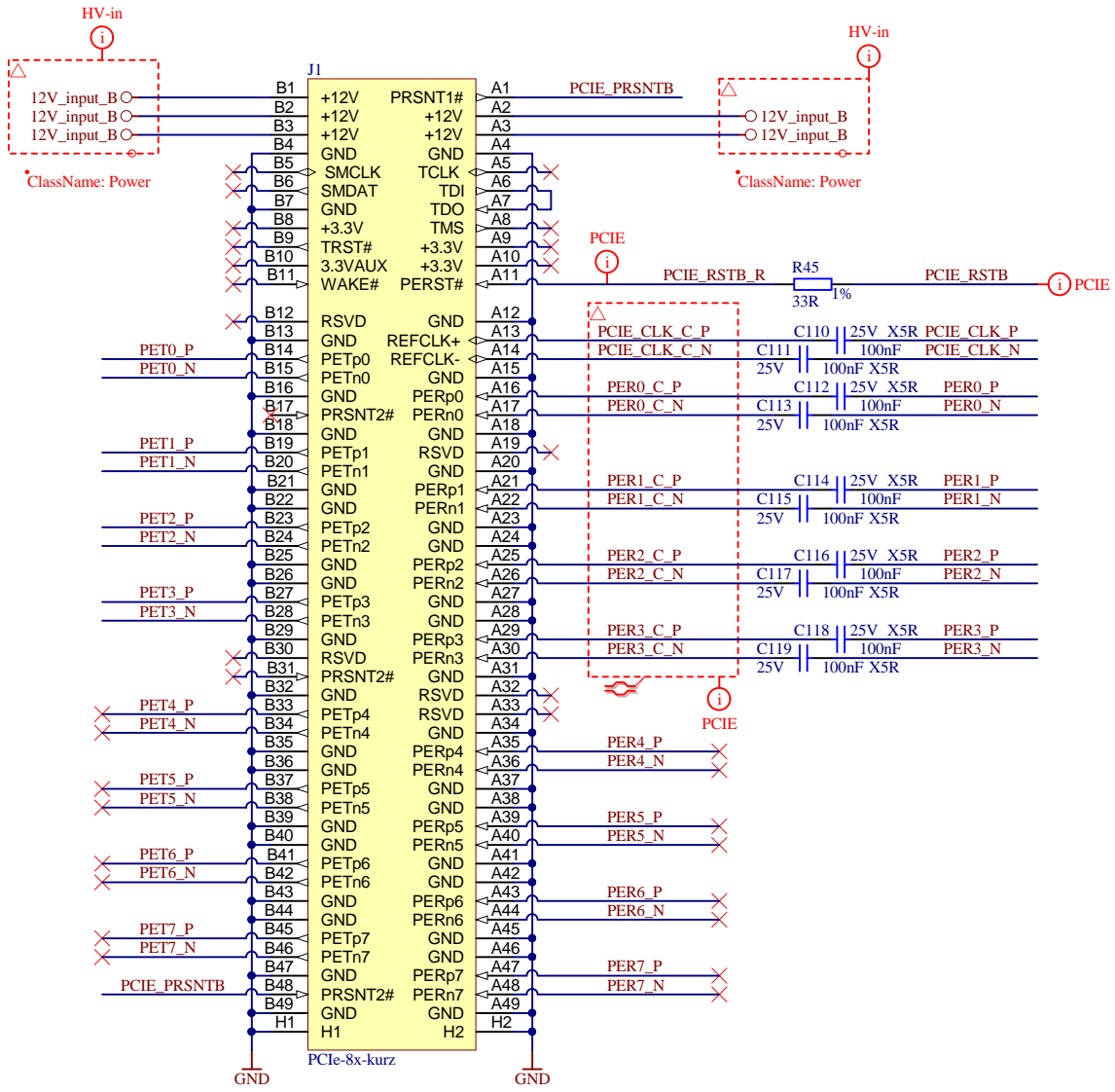


VS2 | VS1 | VS0 | Output Voltage

0	0	0	3.3V
0	0	1	2.5V
0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V



Title: TEF1001 - FMC_PWR		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
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Filename: FMC_PWR.SchDoc		



Title: TEF1001 - PCIe CONNECTOR		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 8 of 33
Filename: PCIe_CONN.SchDoc		

U_FPGA_BANK_12
FPGA_BANK_12.SchDoc

U_FPGA_MGT_BANKS
FPGA_MGT_BANKS.SchDoc

U_FPGA_BANK_13
FPGA_BANK_13.SchDoc

U_FPGA_CFG
FPGA_CFG.SchDoc

U_FPGA_BANK_14
FPGA_BANK_14.SchDoc

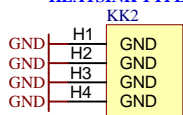
U_DDR_Banks
DDR_Banks.SchDoc

U_FPGA_BANK_15
FPGA_BANK_15.SchDoc

U_FPGA_POWER
FPGA_POWER.SchDoc

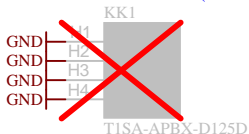
U_FPGA_BANK_16
FPGA_BANK_16.SchDoc

HEATSINK TYPE 2 (FPGA)

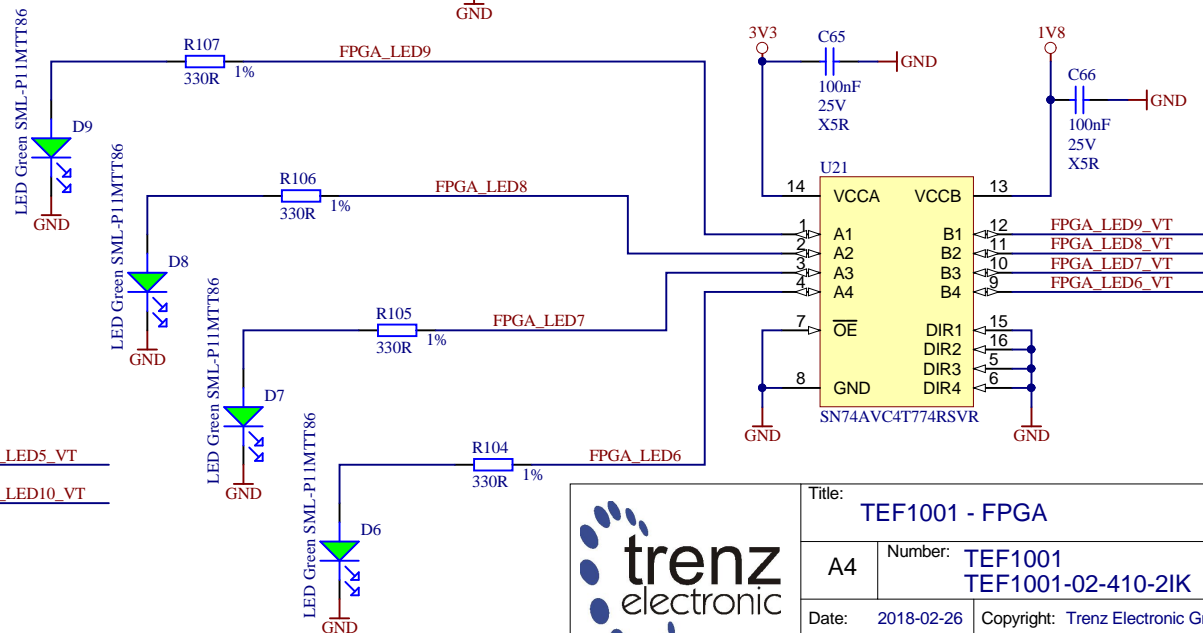
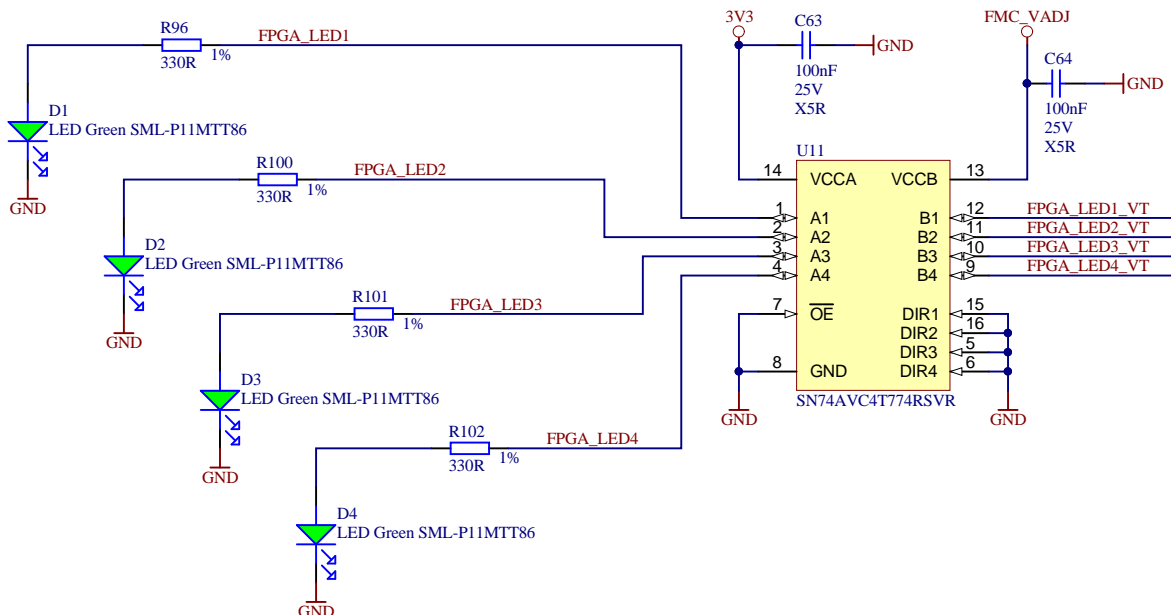
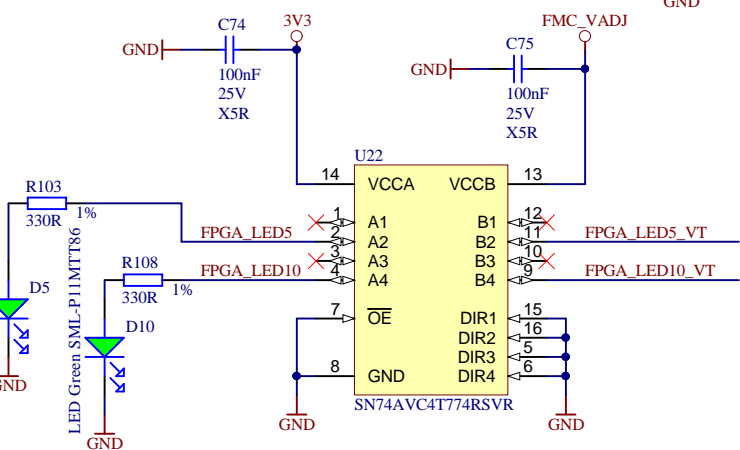


ATS-FPS058061011-40-C2-R0

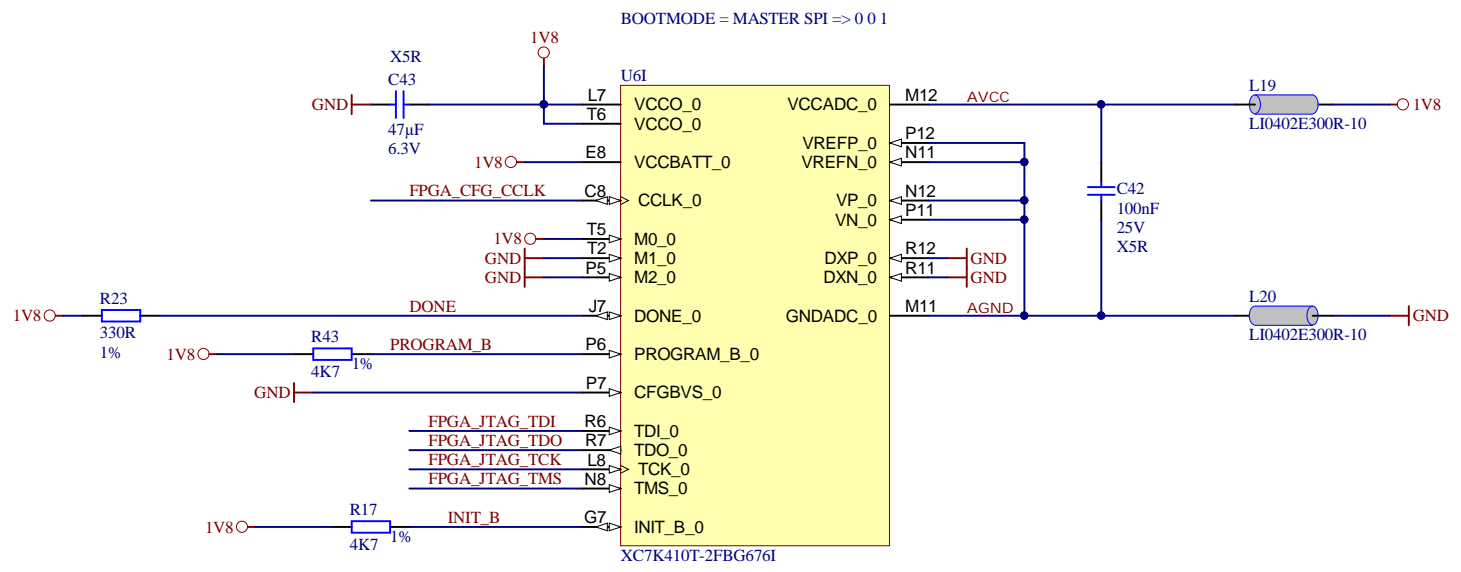
HEATSINK TYPE 1 (FPGA)




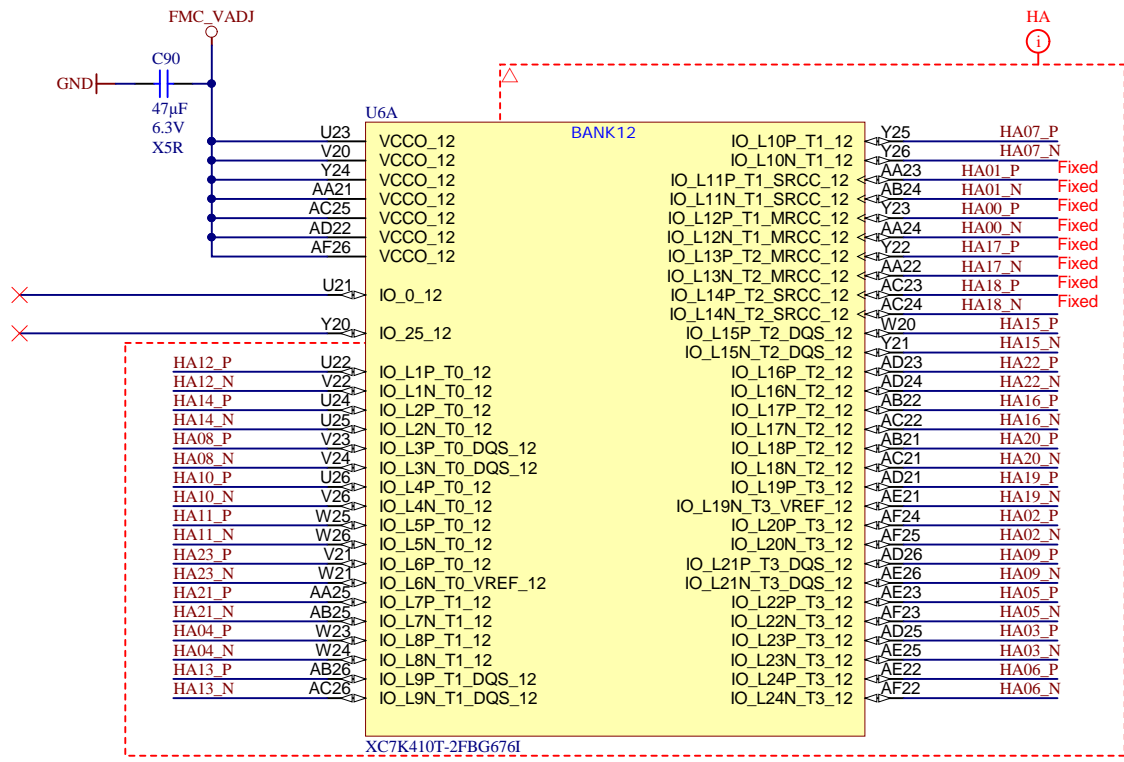
Hardware for HEATSINK TYPE 2 (FPGA)



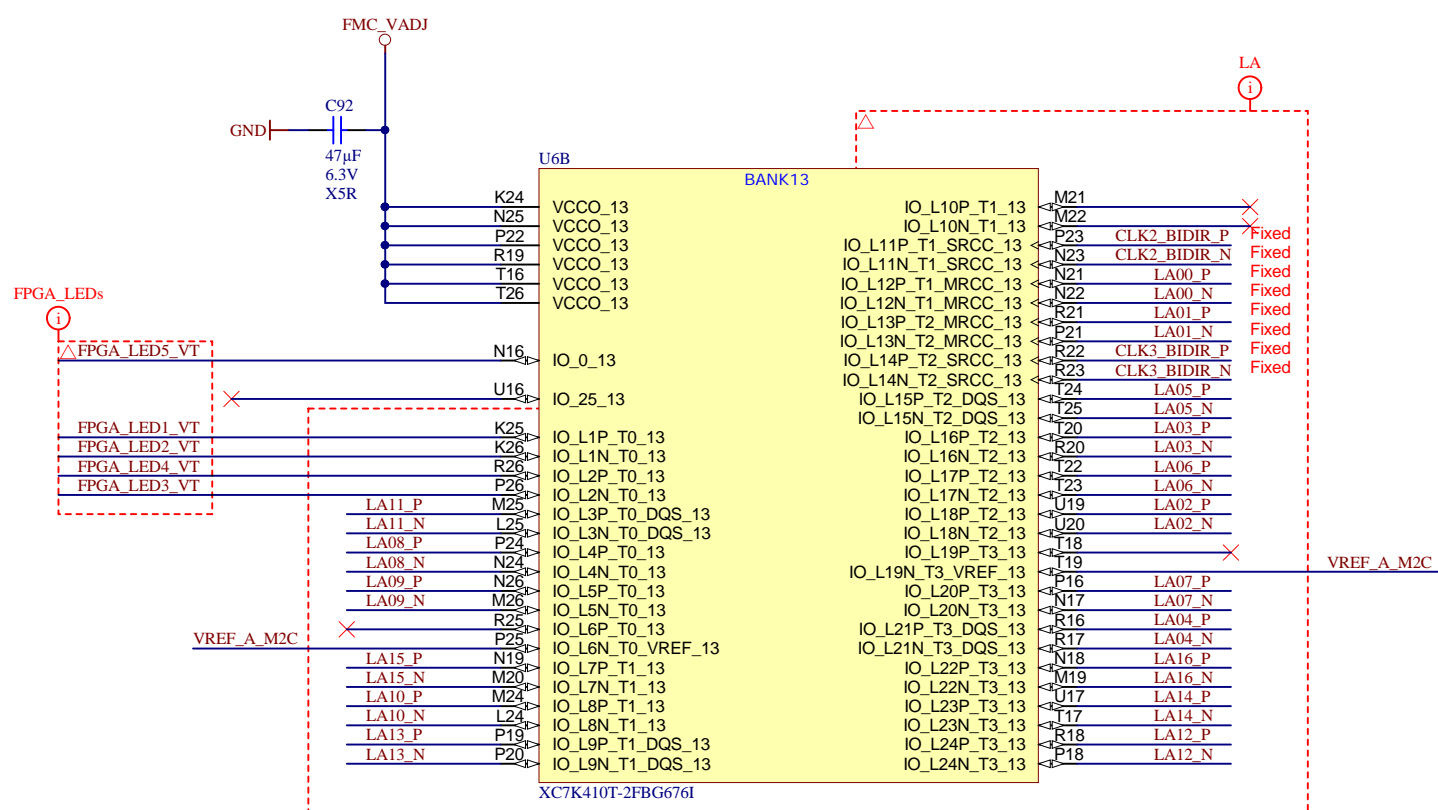
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A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 9 of 33
Filename: FPGA.SchDoc		



	Title: TEF1001 - FPGA_CFG		
	A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 10 of 33
	Filename: FPGA_CFG.SchDoc		



	Title: TEF1001 - FPGA_BANK_12		
	A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 11 of 33
	Filename: FPGA_BANK_12.SchDoc		



Title: TEF1001 - FPGA_BANK_13		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 12 of 33
Filename: FPGA_BANK_13.SchDoc		

A

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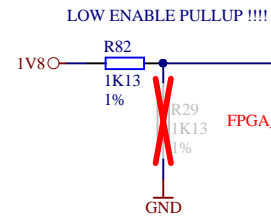
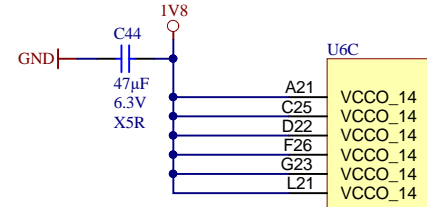
D

A

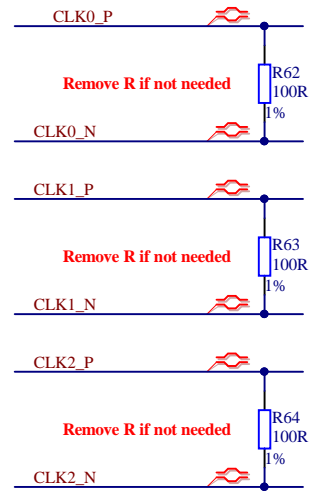
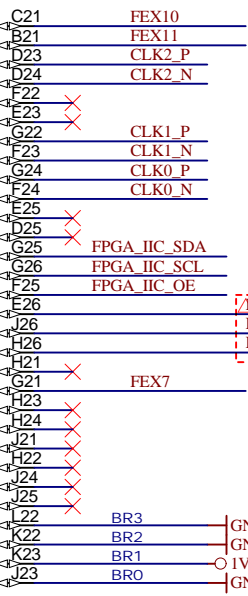
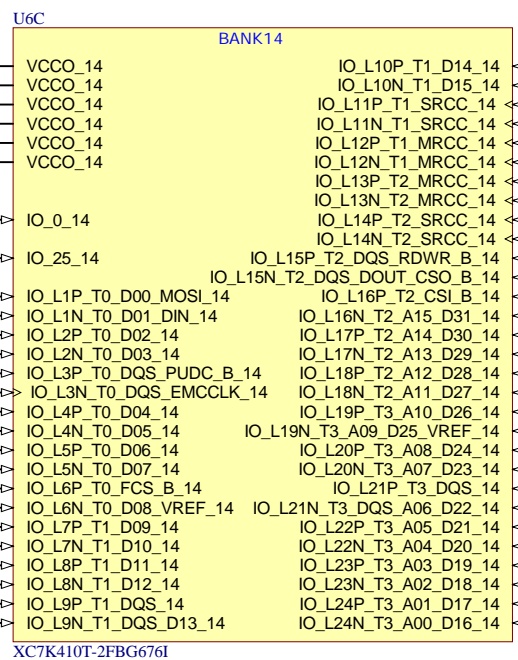
B

C

D

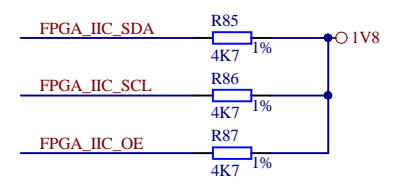
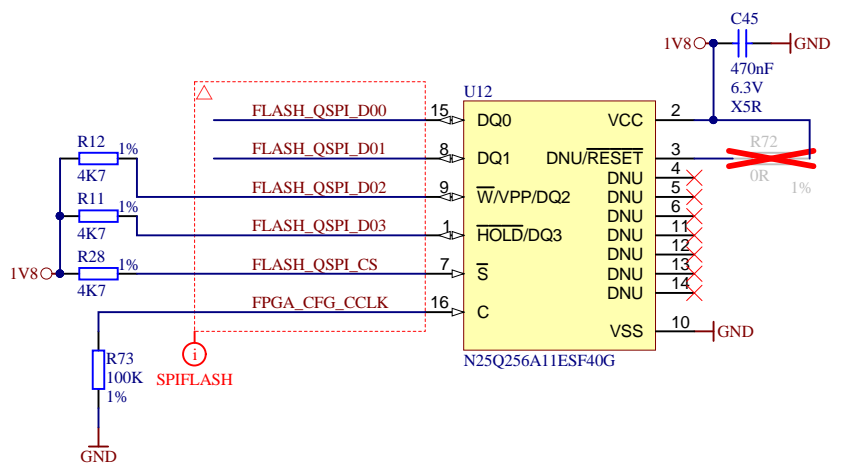


- FLASH_QSPI_D00 B24
- FLASH_QSPI_D01 A25
- FLASH_QSPI_D02 B22
- FLASH_QSPI_D03 A22
- PUDC_B B25
- FEX3 B26
- FEX2 A23
- FPGA_LED9_VT A24
- FEX4 D26
- FEX5 C26
- FLASH_QSPI_CS C23
- FEX_DIR C24
- FEX9 D21
- FEX6 C22
- FEX0 B20
- FEX1 A20
- FEX8 E21

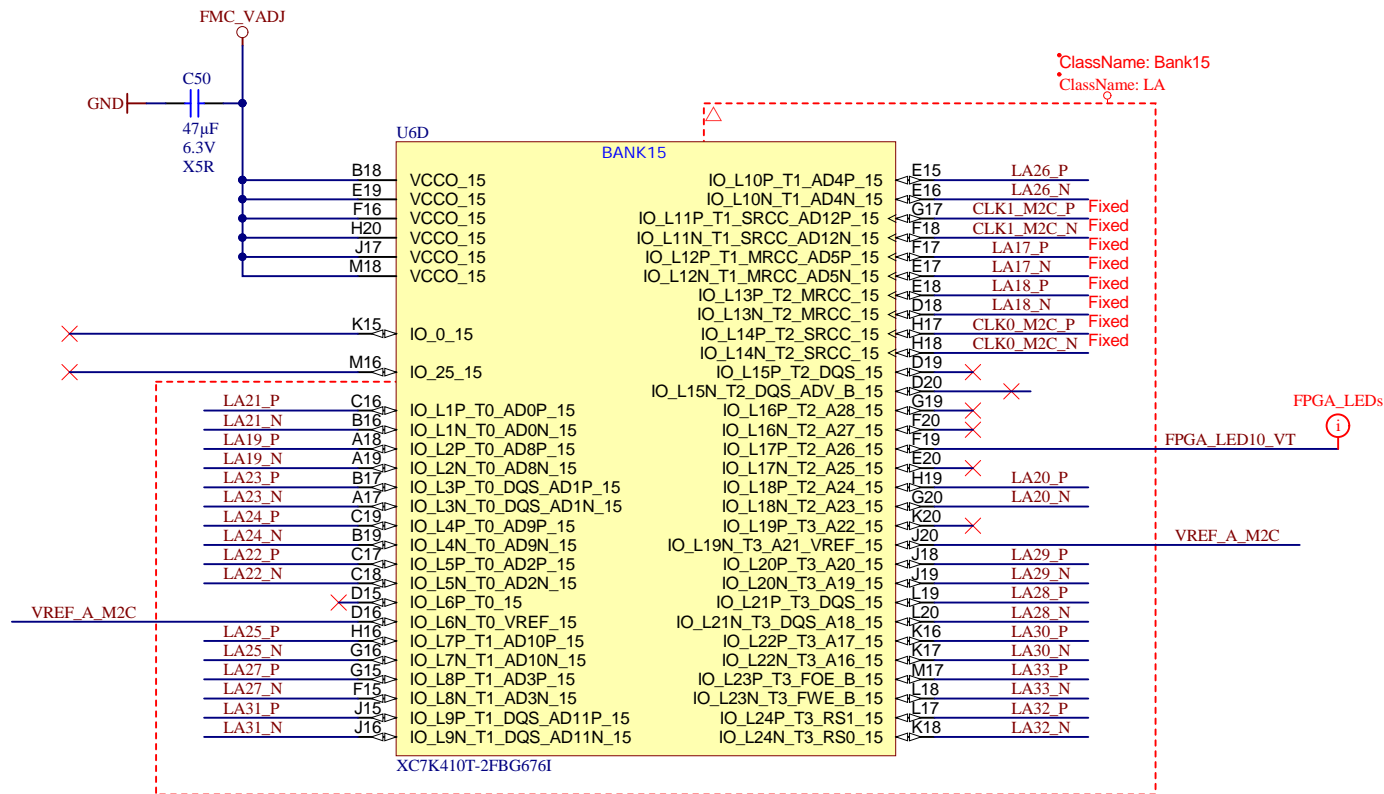


Board Revisions

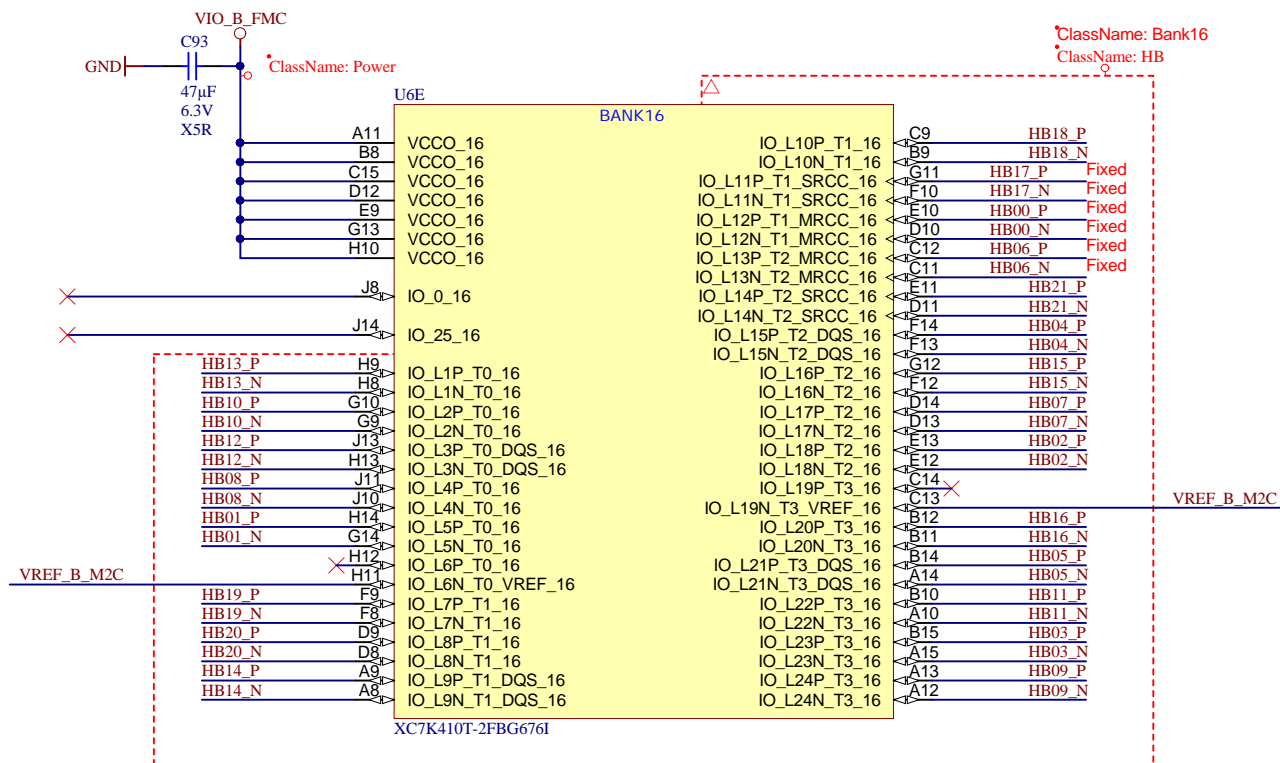
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0	1	0	0	REV02



Title: TEF1001 - FPGA_BANK_14		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 13 of 33
Filename: FPGA_BANK_14.SchDoc		



Title: TEF1001 - FPGA_BANK_15		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 14 of 33
Filename: FPGA_BANK_15.SchDoc		



Title: TEF1001 - FPGA_BANK_16		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 15 of 33
Filename: FPGA_BANK_16.SchDoc		

1

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A

A

U_FPGA_BANK_32
FPGA_BANK_32.SchDoc



U_FPGA_BANK_33
FPGA_BANK_33.SchDoc



U_FPGA_BANK_34
FPGA_BANK_34.SchDoc



B

B

C

C

D


D

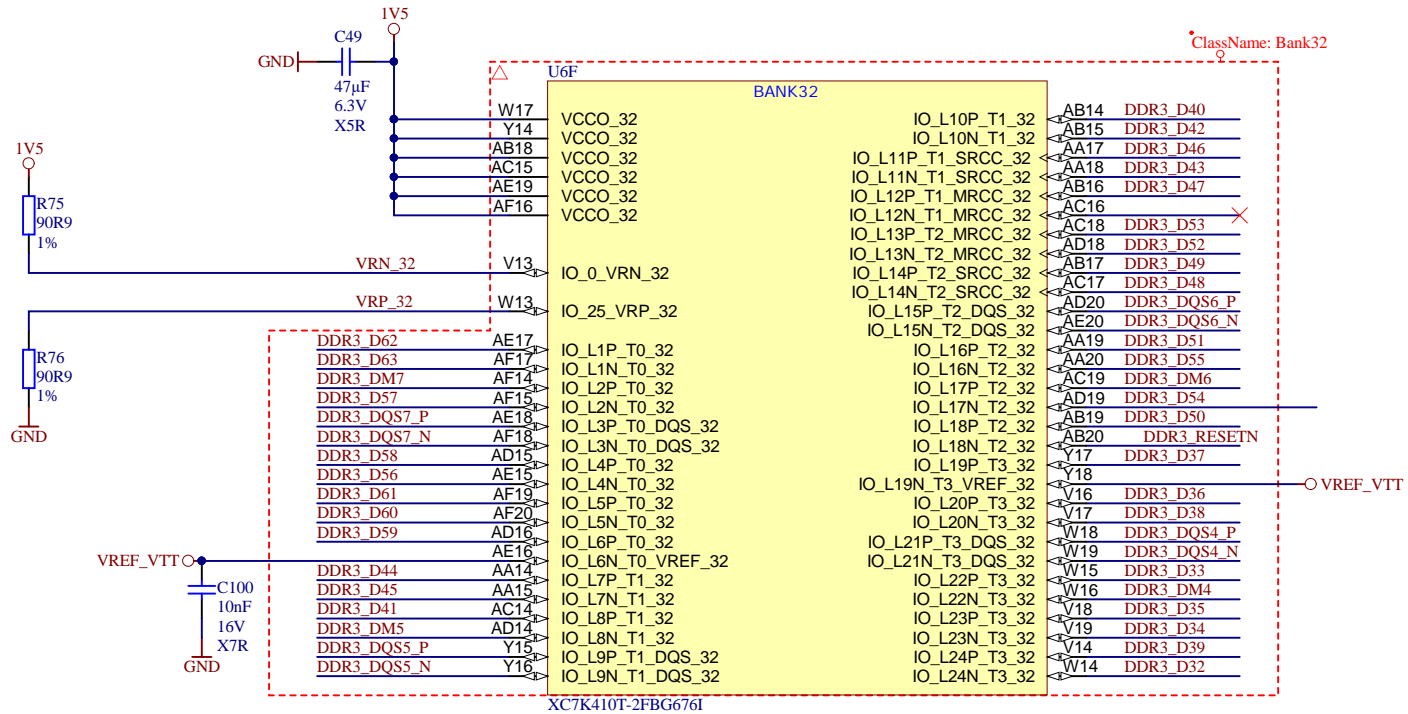
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2

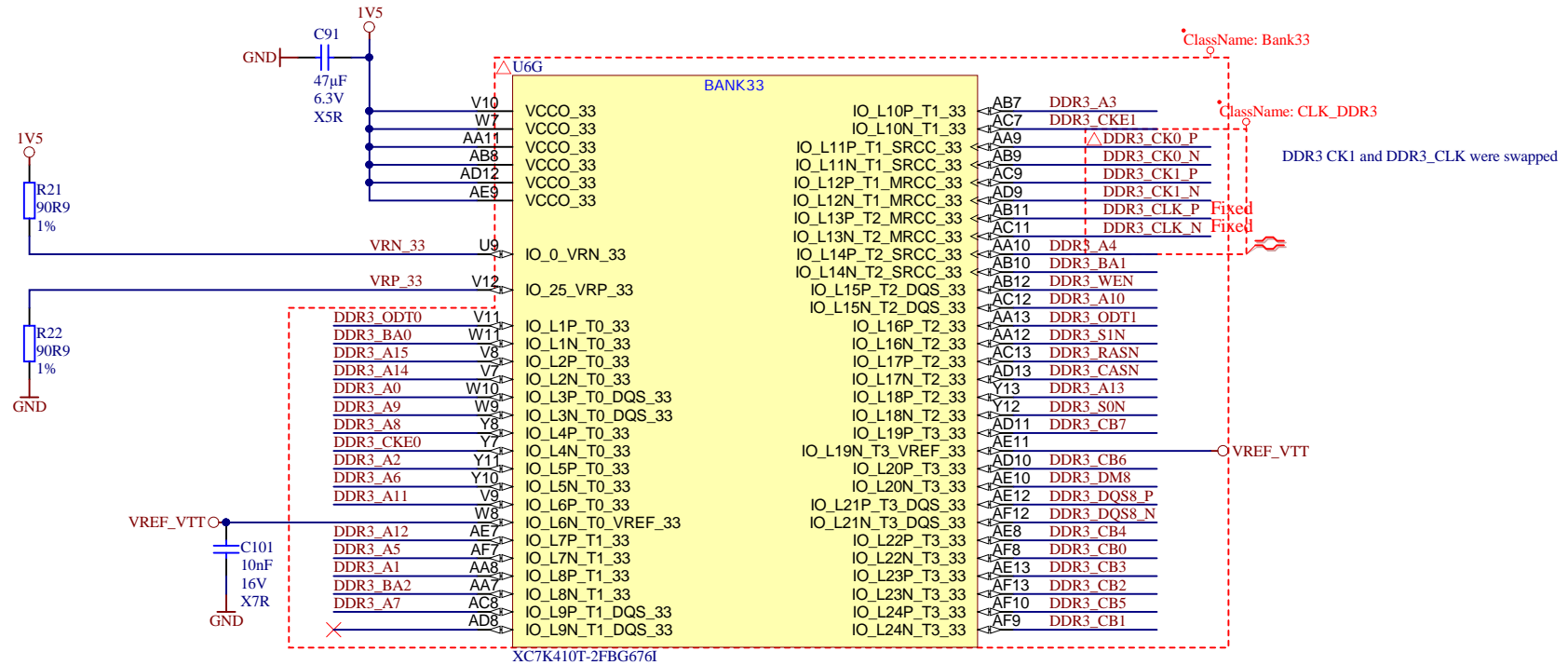
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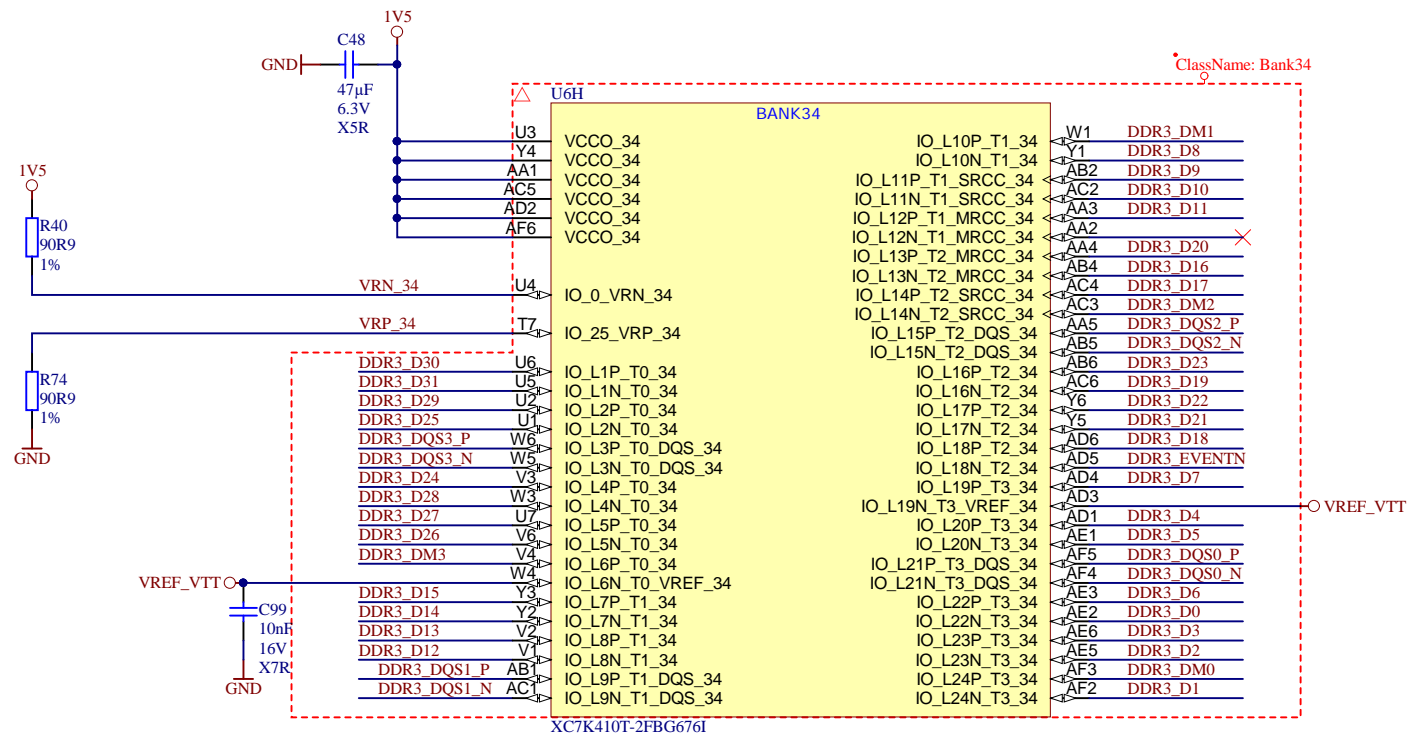
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	A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 16 of 33
	Filename: DDR_Banks.SchDoc		



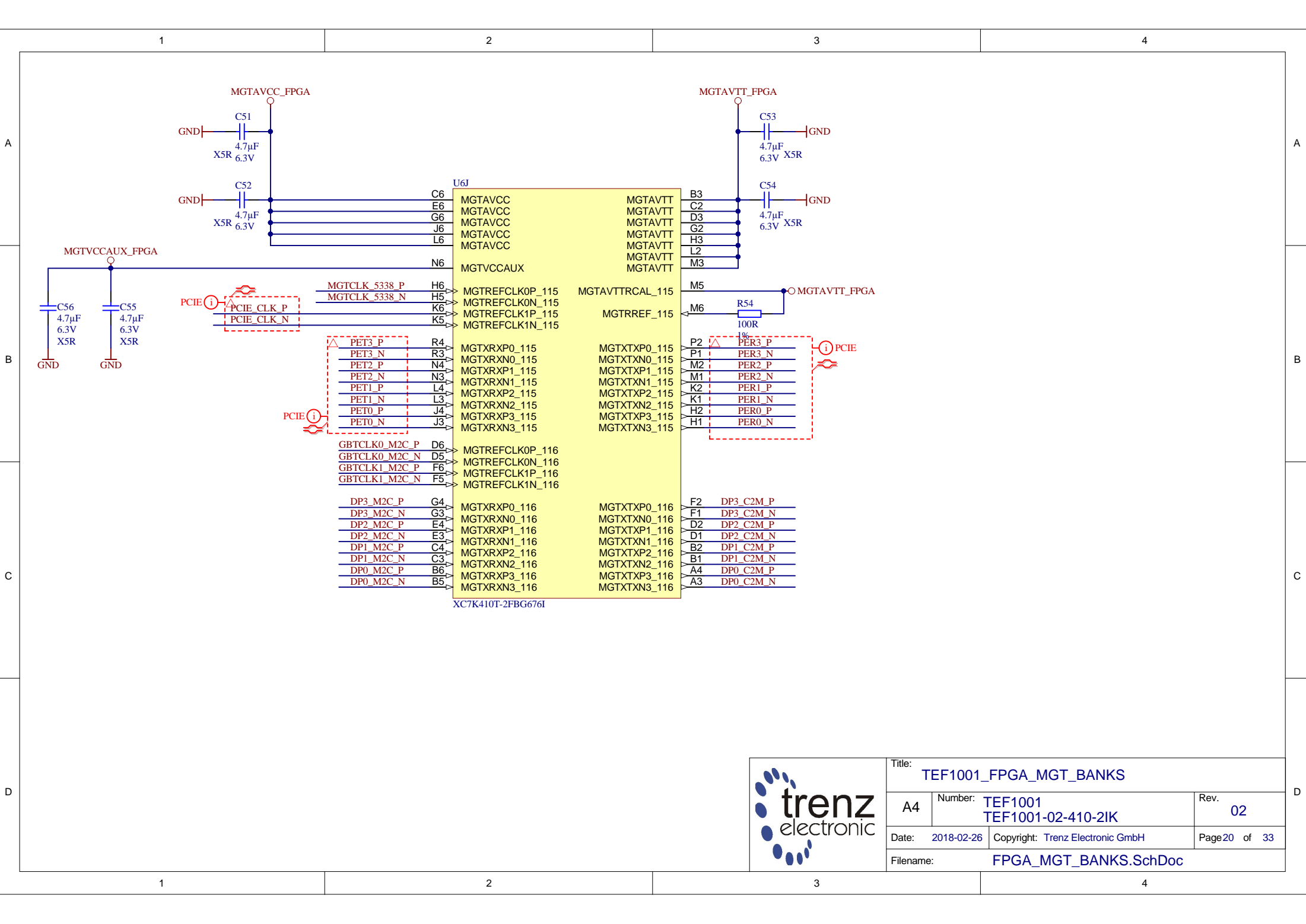
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A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 17 of 33
Filename: FPGA_BANK_32.SchDoc		




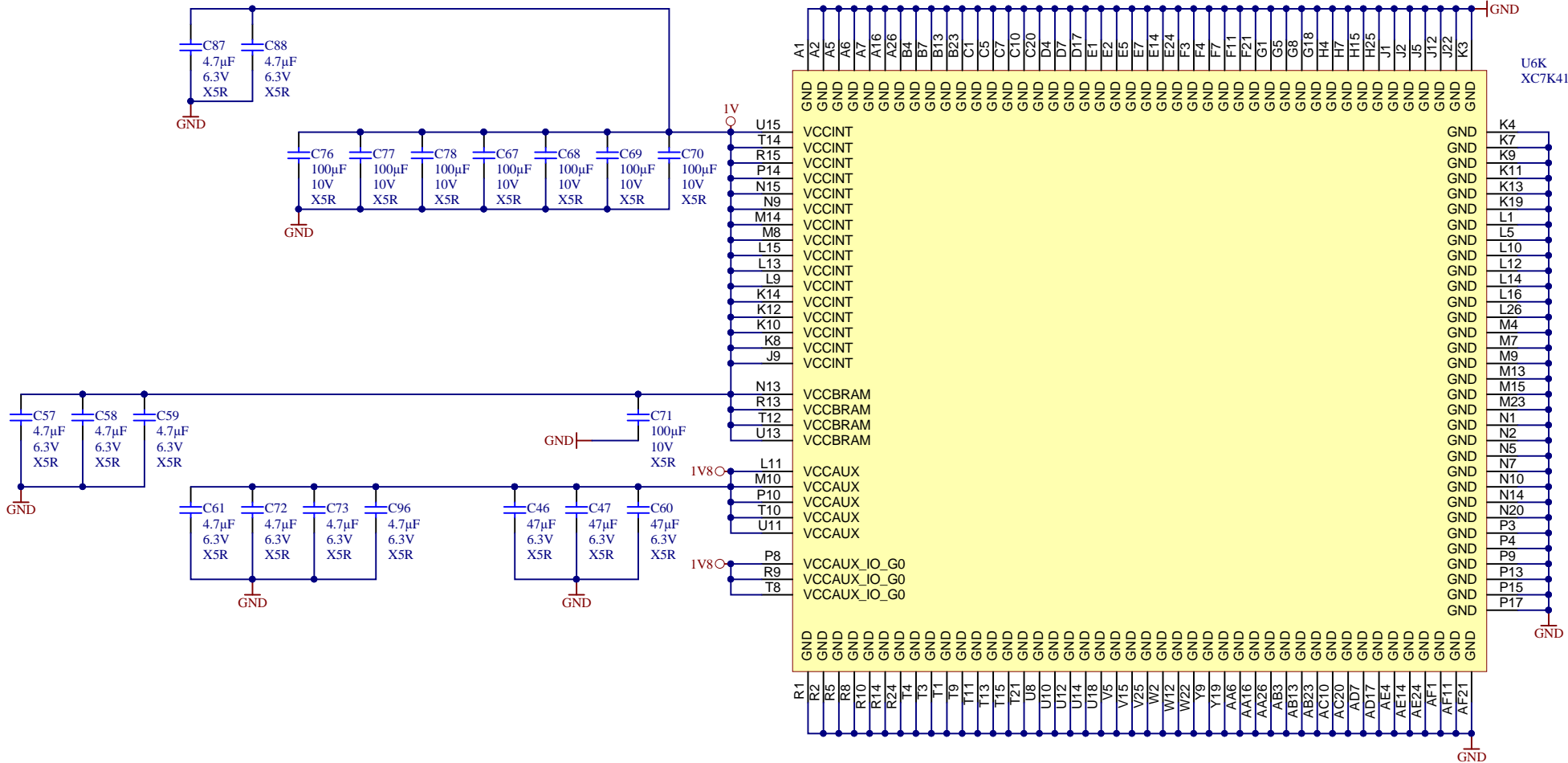
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A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 18 of 33
Filename: FPGA_BANK_33.SchDoc		



Title: TEF1001 - FPGA_BANK_34		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 19 of 33
Filename: FPGA_BANK_34.SchDoc		



	Title: TEF1001_FPGA_MGT_BANKS		
	A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 20 of 33
	Filename: FPGA_MGT_BANKS.SchDoc		



Title: TEF1001 - FPGA_POWER		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 21 of 33
Filename: FPGA_POWER.SchDoc		

A

B

C

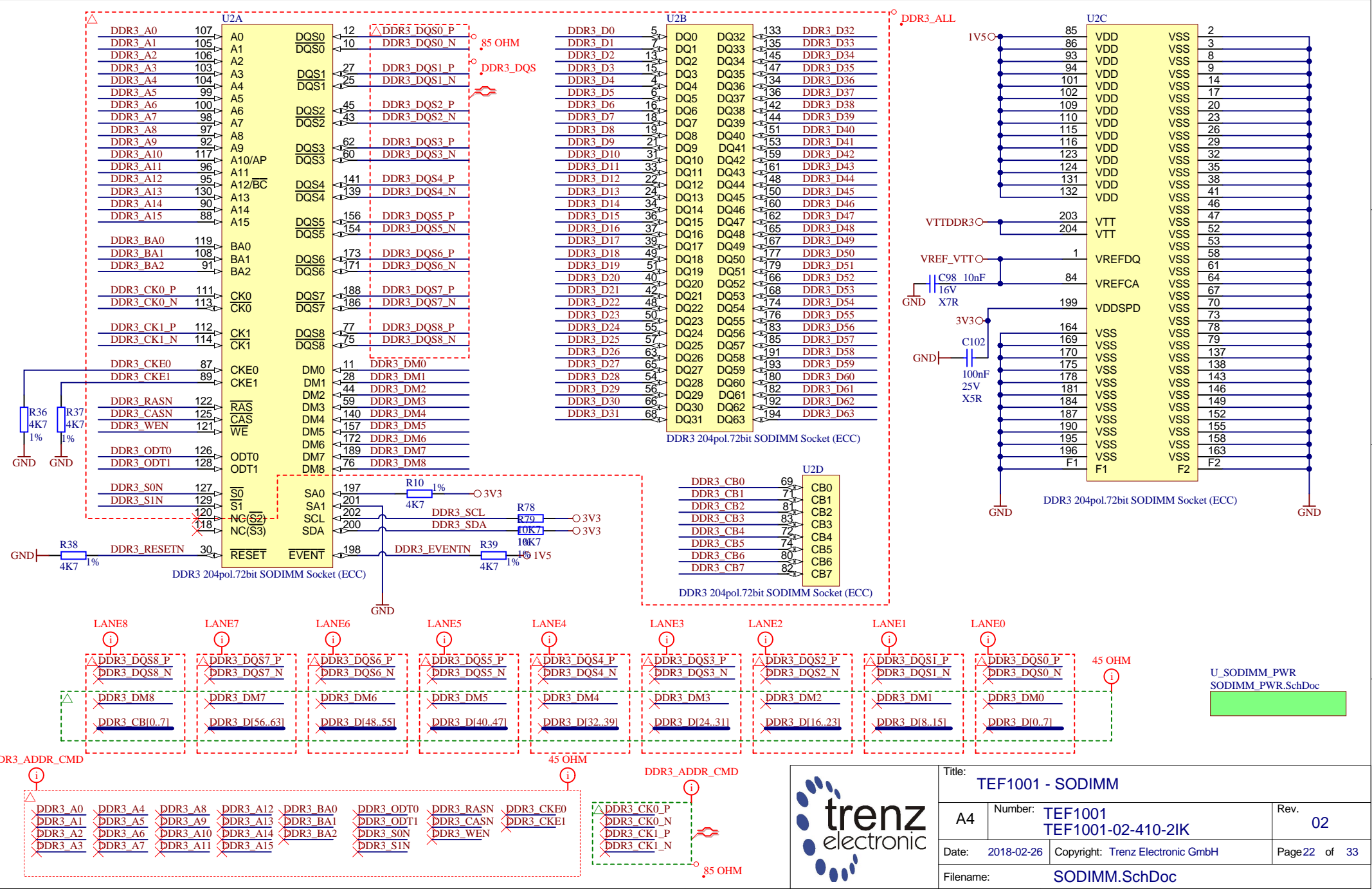
D

A

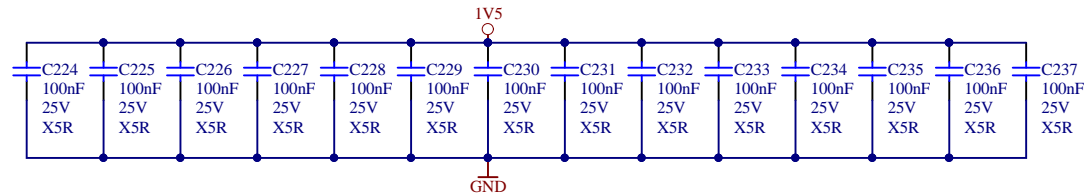
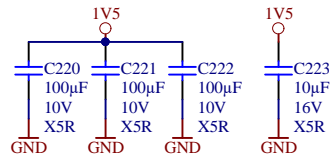
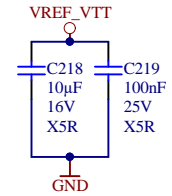
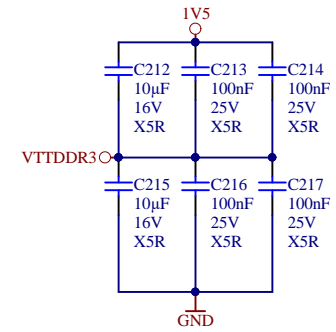
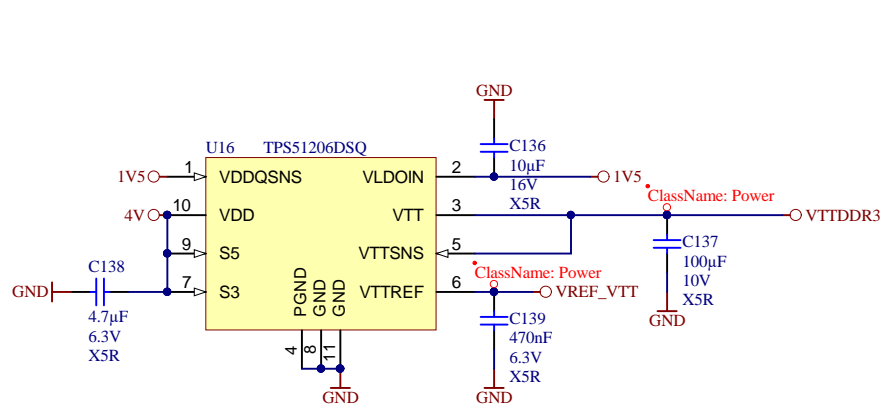
B


C

D



Title: TEF1001 - SODIMM		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 22 of 33
Filename: SODIMM.SchDoc		



	Title: TEF1001 - SODIMM_PWR		
	A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 23 of 33
	Filename: SODIMM_PWR.SchDoc		

U_PWR_4V_1V5
PWR_4V_1V5.SchDoc

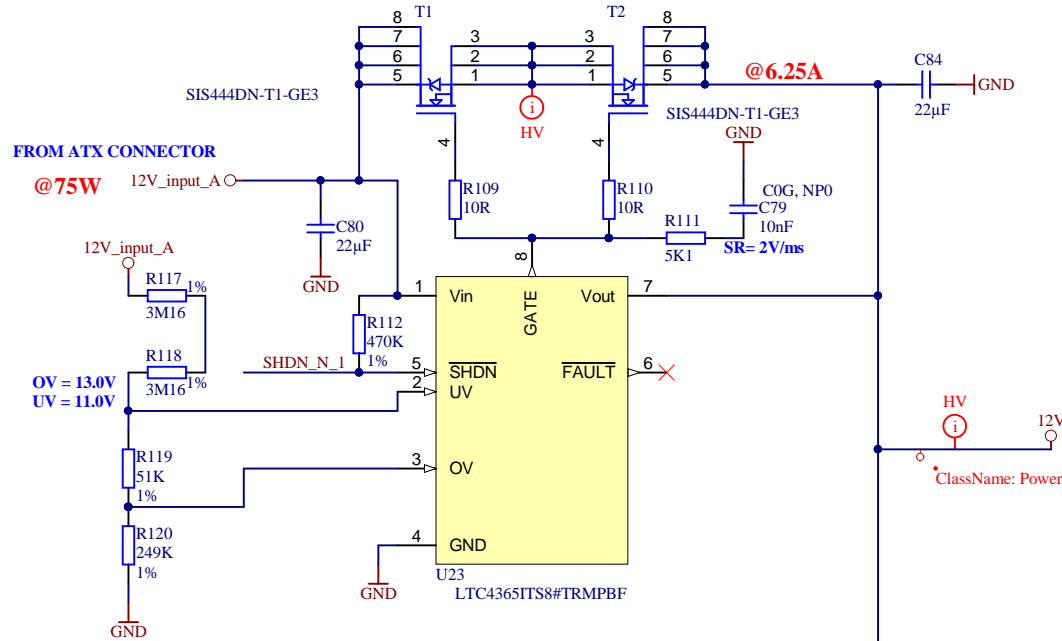
U_PWR_3V3
PWR_3V3.SchDoc

U_PWR_1V
PWR_1V.SchDoc

U_PWR_MGT
PWR_MGT.SchDoc

U_PWR_1V8
PWR_1V8.SchDoc

U_PWR_5V
PWR_5V.SchDoc



FAN FPGA

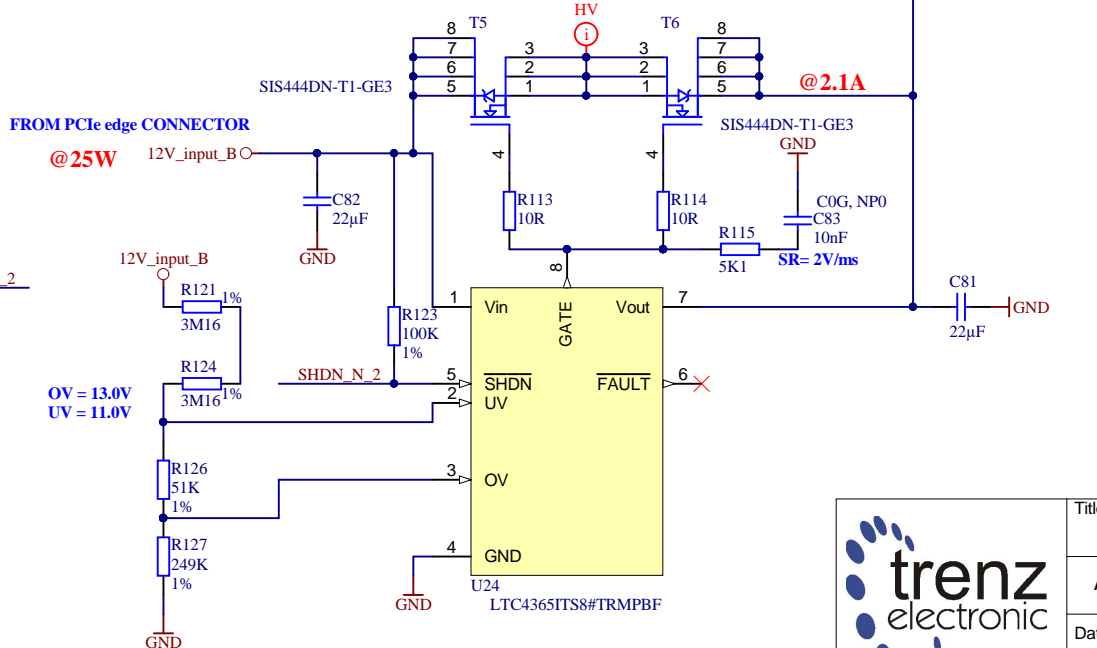
FMC J2 Connector MIN1.4V MAX12.6V (Sec. 5.10. Power Supply Req.)

U4 REGULATOR 1V MIN5.75V MAX26.5V

U3 REGULATOR 4V&1V5 MIN5.75V MAX26.5V

U9 REGULATOR 3V3 MIN4.5V MAX17V

U8 REGULATOR 5V MIN6V MAX17V



Title: TEF1001 - POWER		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 24 of 33
Filename: POWER.SchDoc		

A

A

B

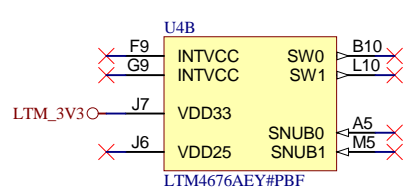
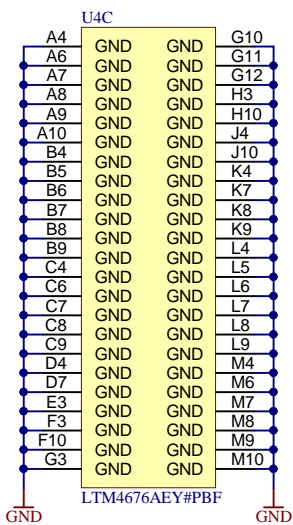
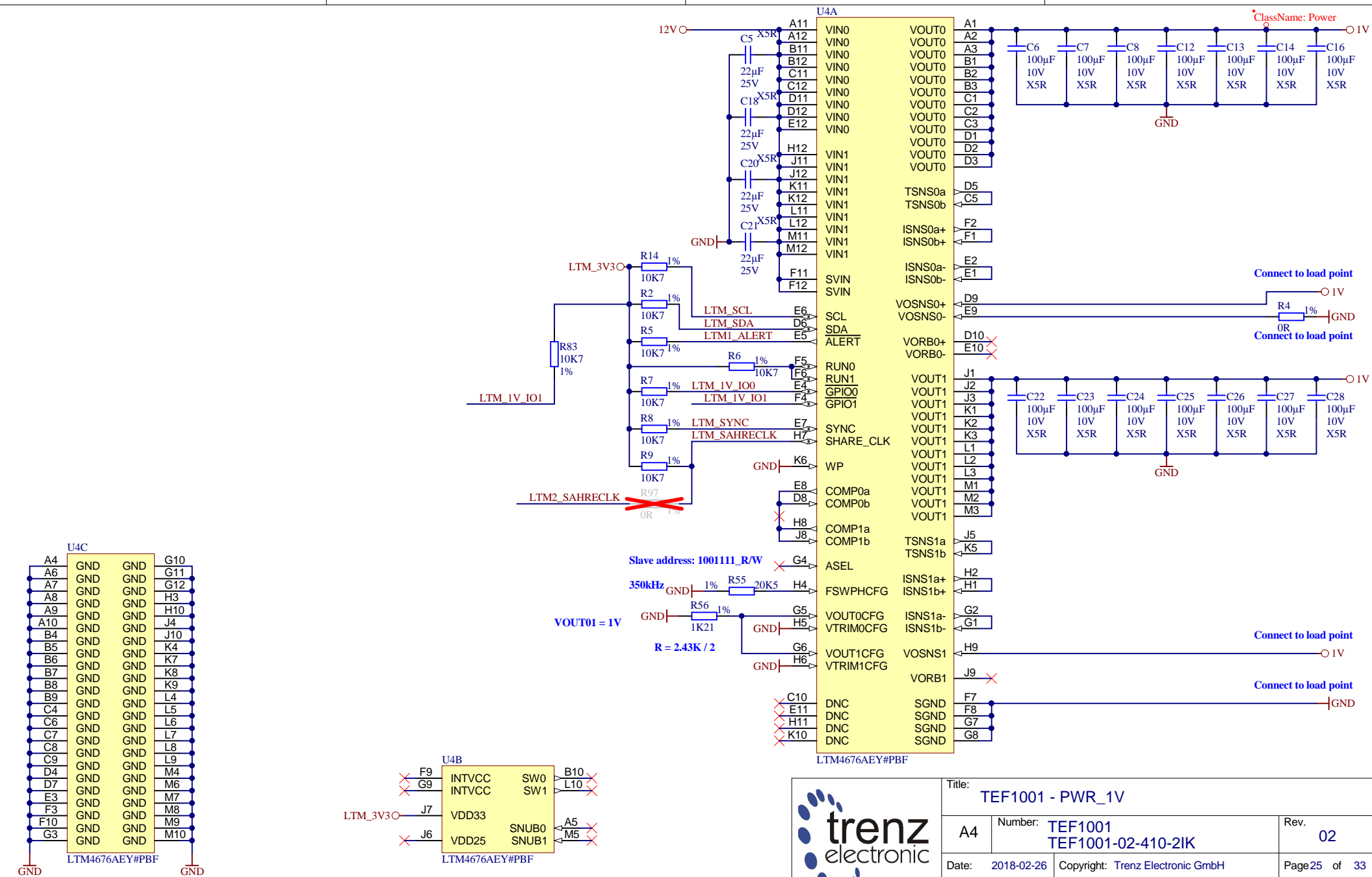
B

C

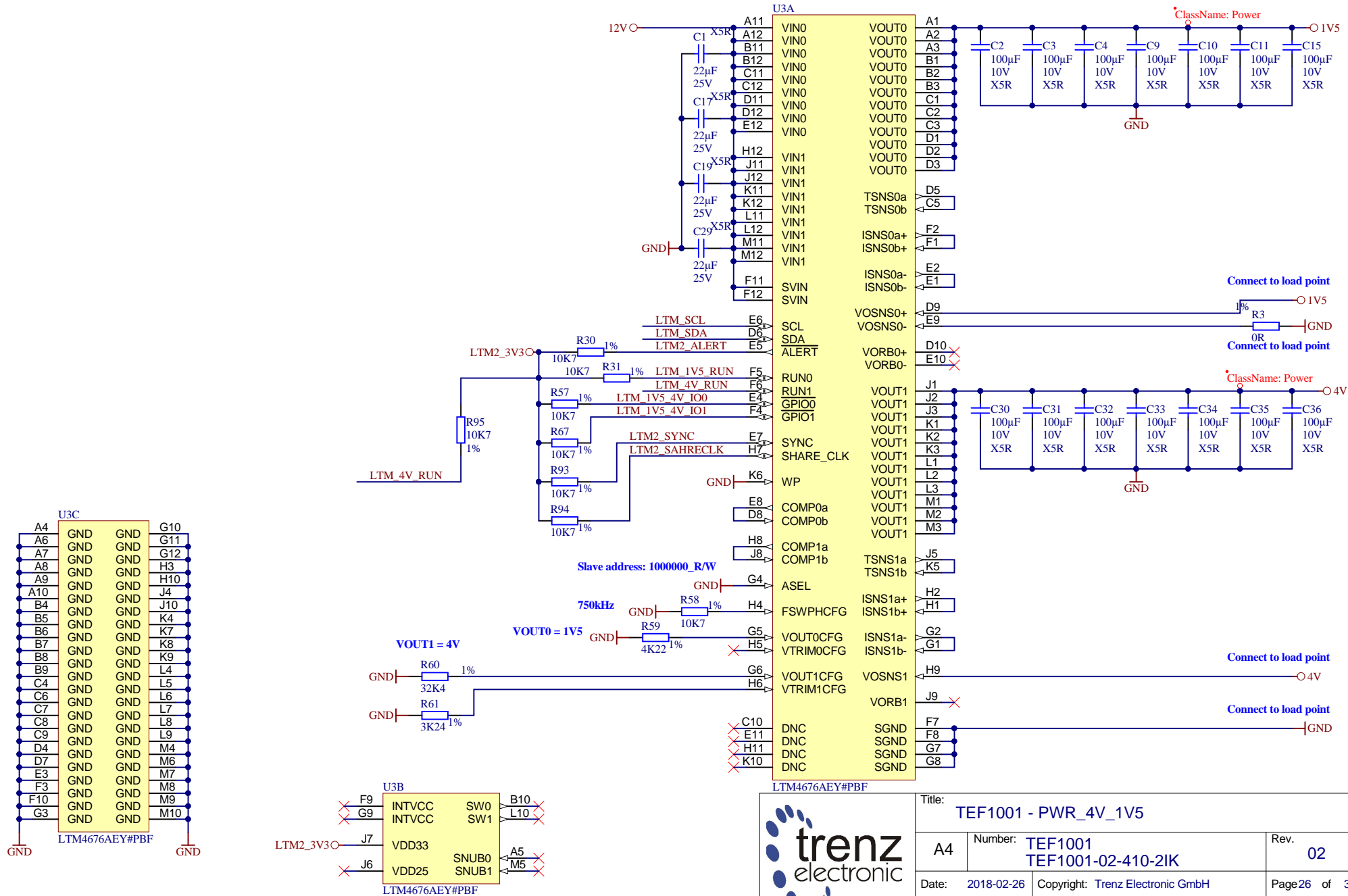
C

D

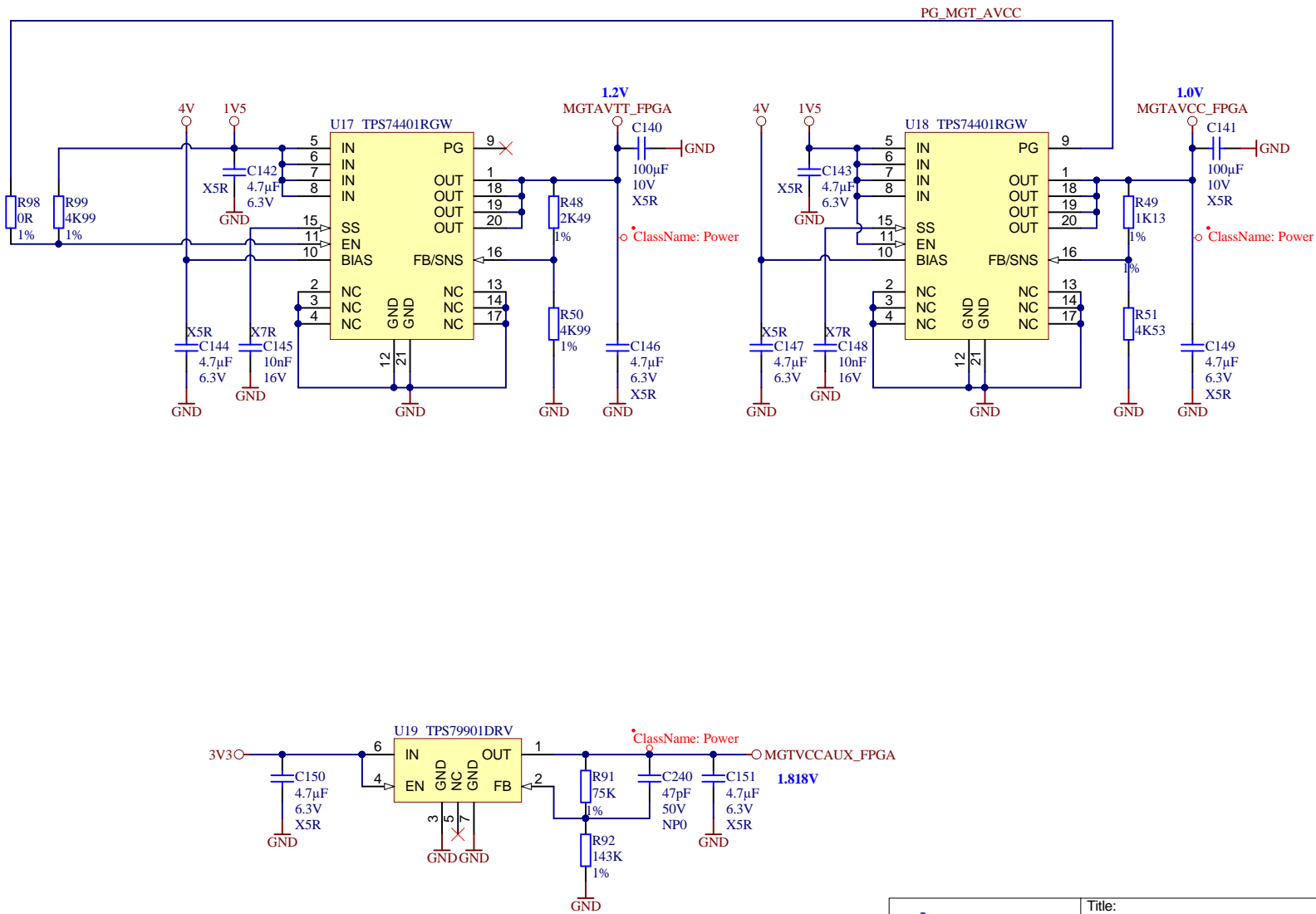
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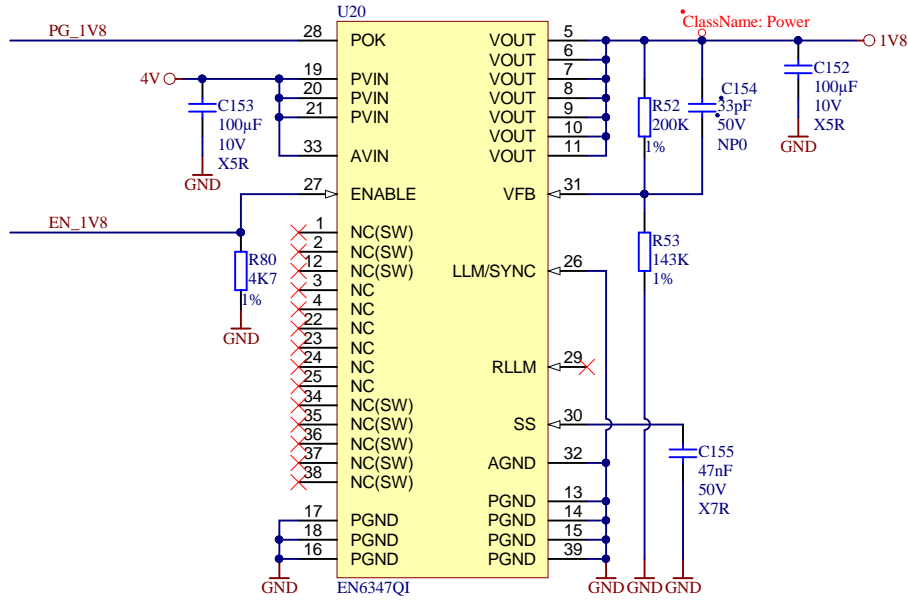
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A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 25 of 33
Filename: PWR_1V.SchDoc		



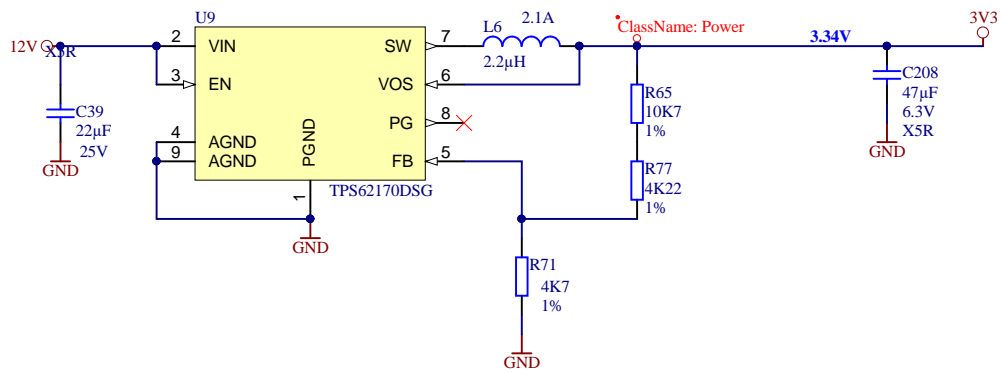
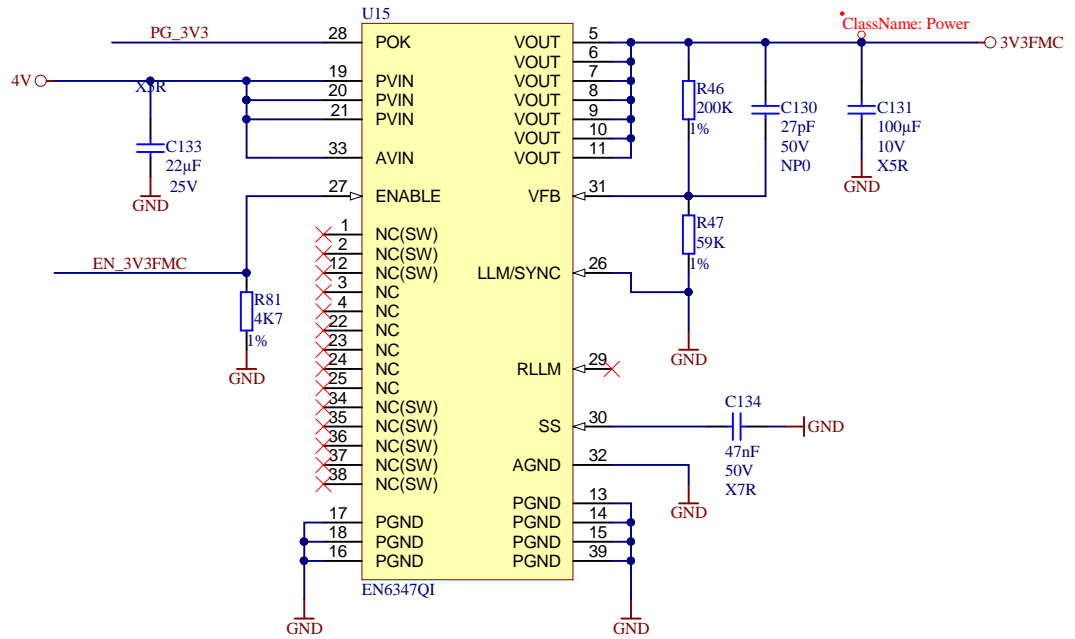
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Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 26 of 33
Filename: PWR_4V_1V5.SchDoc		




Title: TEF1001 - PWR_MGT		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 27 of 33
Filename: PWR_MGT.SchDoc		



Title: TEF1001 - PWR_1V8		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 28 of 33
Filename: PWR_1V8.SchDoc		



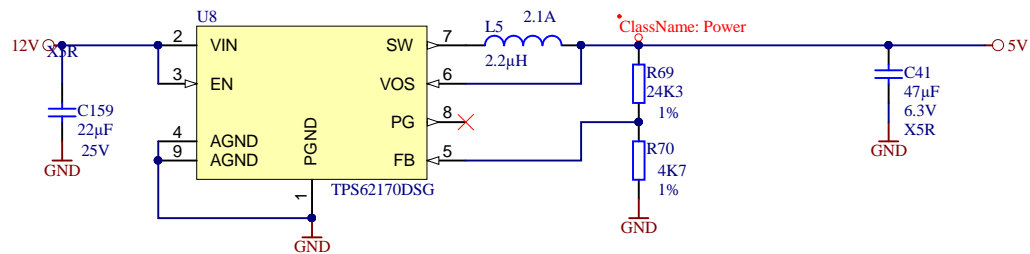
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Date: 2018-02-26		Copyright: Trenz Electronic GmbH		Page 29 of 33
Filename: PWR_3V3.SchDoc				


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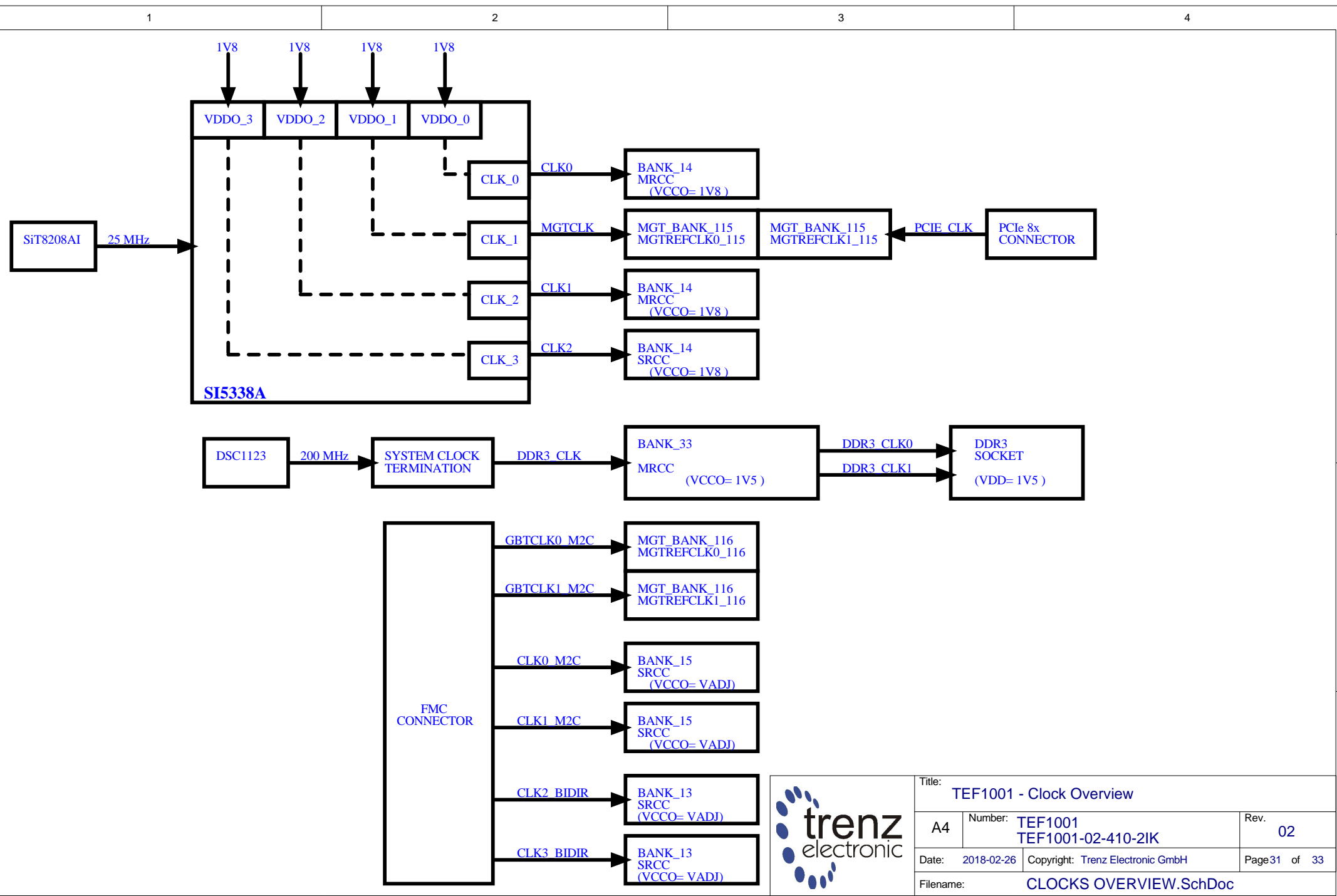
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Date: 2018-02-26		Copyright: Trenz Electronic GmbH	
Filename: PWR_5V.SchDoc		Page 30 of 33	

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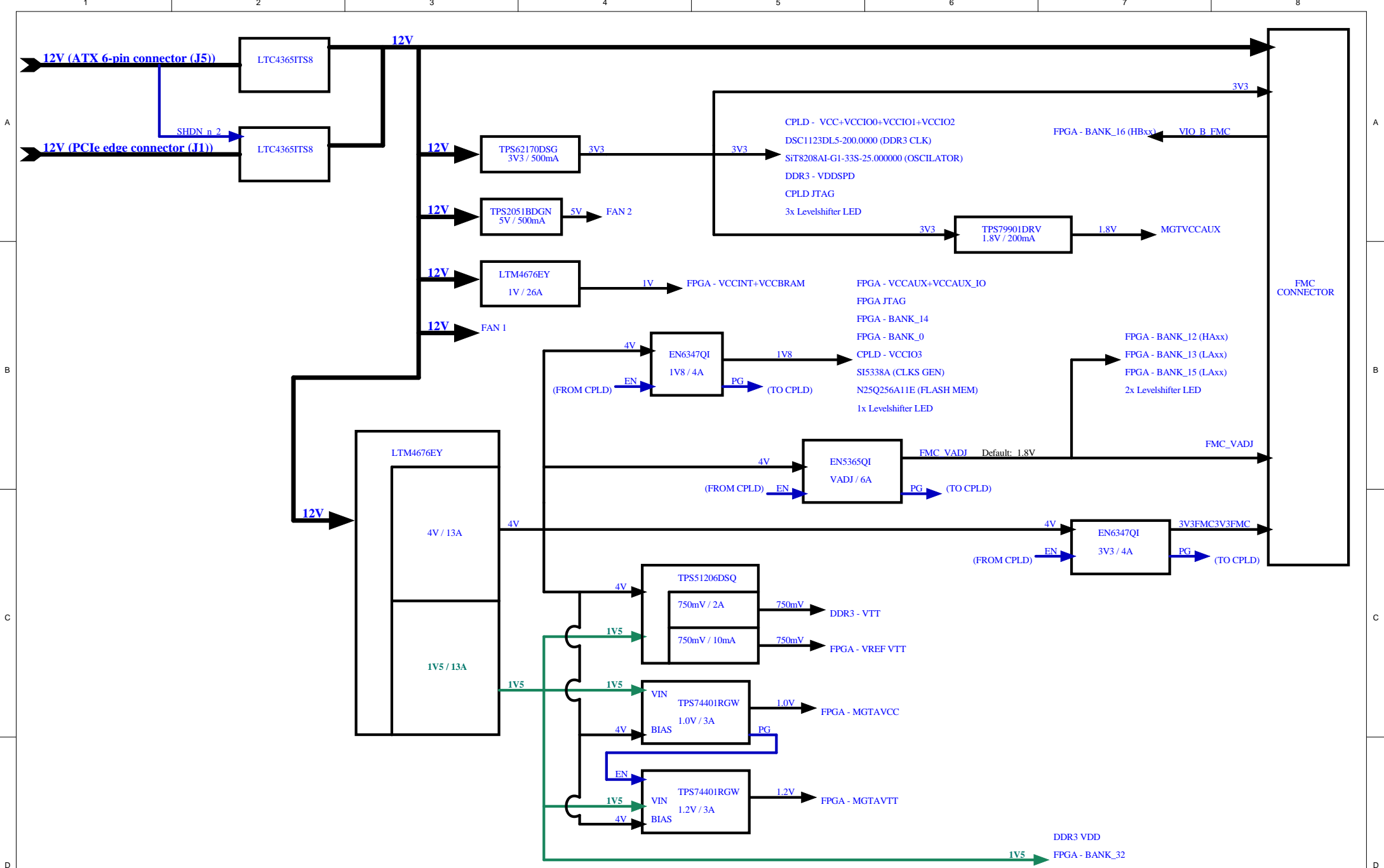
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Title: TEF1001 - Clock Overview		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 31 of 33
Filename: CLOCKS OVERVIEW.SchDoc		



Title: TEF1001 - Power Ens_PGs_COMMs		
A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
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Filename: POWER_ENS_PGs OVERVIEW.SchDoc		

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CHANGES REV01 to REV02:

- 1) added C87, C88 4.7µF
- 2) C154 incremented from 27pF to 33pF
- 3) route 12V input from PCIe edge connector, added input power protection circuits for ATX 12V and PCIe edge connector (U23 with T1, T2 and U24 with T5, T6, resistors and capacitors), power priority switch T3, (priority for ATX)
- 4) added S1 (FMC_VADJ value, and JTAG_EN)
- 5) T4 and resistors added for reading the FMC_PRSNT_M2C value
- 6) U25 and capacitors added (FMC_FAN)
- 7) added screws for bracket
- 8) added 10 x FPGA LEDs D1-D10 via levelshifter (U11, U21, U22)

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	Title: TEF1001 - Revision history		
	A4	Number: TEF1001 TEF1001-02-410-2IK	Rev. 02
	Date: 2018-11-19	Copyright: Trenz Electronic GmbH	Page 33 of 33
	Filename: Revision_Changes.SchDoc		

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