

Keywords: test modes, microprocessor test mode, secret mode, watchdog, microprocessor supervisor, microprocessor-based supervisor

## APPLICATION NOTE 892

# Watchdog Timer Allows Entry to Test Mode

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*Abstract: The following application note discusses how to enter test modes in microprocessor-based devices using the MAX6360 microprocessor supervisor.*

Manuals for microprocessor-based devices often include instructions for entering a "secret mode" in which you can test or reset the device. These instructions typically ask you to depress and hold one or two switches for a minimum time interval. You can adopt several measures to avoid accidentally triggering the test mode: Depress two keys, hold both keys simultaneously and continuously through the minimum interval, and make the interval two to five seconds long.

You can implement such designs with a handful of resistors, capacitors, and diodes and a comparator or two. Even if the circuitry is never used or appreciated by the customer, it raises cost and complexity while lowering system reliability. So a better alternative is to implement the function with minimal additional components.

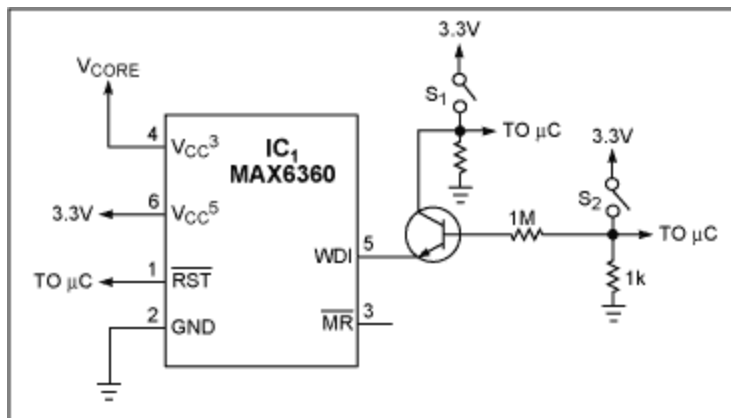


Figure 1. You can activate IC<sub>1</sub> only by depressing S<sub>1</sub> and S<sub>2</sub> simultaneously for at least 2.9sec.

Microprocessor-based devices usually include a voltage supervisor that monitors the V<sub>CC</sub> level and, in some cases, the core voltage. When either voltage drops below its threshold, the supervisor issues a reset to the microprocessor. IC<sub>1</sub> in Figure 1 monitors two voltages, provides a power-on reset, and includes a watchdog timer. If you don't need the watchdog function elsewhere in the system, it can help to implement the switch-delay circuitry. Fortunately, the watchdog timer self-resets when the WDI (watchdog input) Pin 5 is floating, an indication that the circuit is disabled. Thus, you can implement the switch-delay circuitry by enabling and disabling the watchdog timer. Simply provide an interface between WDI and the switches that enable the test mode. The nominal time-out period for IC's watchdog timer

is 2.9sec.

WDI must float when both switches are open and when you depress only one. When you depress both, WDI must assume either the active-high or the active-low state as specified in the data sheet. Note that WDI can remain floating while sinking 5  $\mu$ A. The npn transistor isolates WDI from the switches' pulldown resistors. When  $S_2$  closes, current flows through the base of the transistor to WDI, which remains floating because the 1M $\Omega$  resistor limits the current to less than 5 $\mu$ A. The transistor turns on and forces WDI to the active-high level only when you depress  $S_1$  as well. If you depress the switches in reverse order, WDI switches high only when you close  $S_2$ . You must close both switches to activate the watchdog timer. After the timer activates, IC<sub>1</sub> imposes a 2.9sec delay before asserting a reset (Pin 1). If you release either or both switches during this 2.9sec period, the timer resets. Thus, for the minimal cost of an npn transistor and three resistors, the supervisor IC can monitor two voltages, provide a power-on-reset signal, and implement a dual-switch delay function. To monitor one voltage, you can replace IC<sub>1</sub> with a MAX823.

A similar version of this article appeared in the July 19, 2001 issue of *EDN* magazine.

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