A Product Line of
Diodes Incorporated

PI3EQX2024

USB 3.2 Gen 2x2 ReDriver

Features

- 5Gbps & 10Gbps Serial Link with Linear Equalizer
- USB 3.2 Gen 2 and Gen 1 Compatible
- USB 3.2 Gen 2x2 Compatible
- Four 10Gbps Differential Signal Pairs
- Pin Adjustable Receiver Equalization
- Pin Adjustable Flat Gain
- 100Ω Differential CML I/Os
- Automatic Receiver Detect
- Auto Slumber Mode for Adaptive Power Management
- Single Supply Voltage: 3.3V
- Patented Technology
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green available):
  - 34-pin, UQFN 2.5mm × 4.5mm (ZTF34)

Description

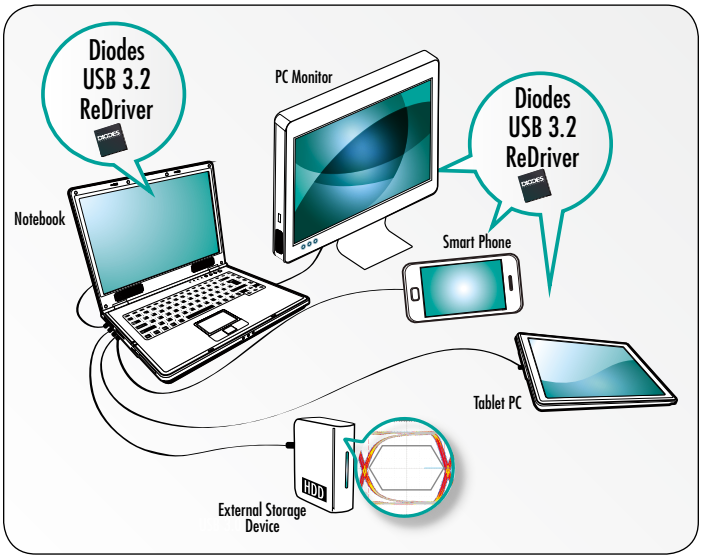
The PI3EQX2024 is a low-power, high-performance, USB 3.2 Gen 2x2 linear ReDriver™ designed specifically for the USB 3.2 protocol.

The device provides programmable equalization and flat gain to optimize performance over a variety of physical mediums by reducing intersymbol interference. PI3EQX2024 supports two 100Ω differential CML data I/Os between the Protocol ASIC to a switch fabric, over cable, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver. Each channel operates fully independently. The channels' input signal level determines whether the output is active.

The PI3EQX2024 also includes an automatic receiver detect function. The receiver detection loop is active again if the corresponding channel's signal detector is idle for longer than 7.3ms. The channel then moves to unplug mode if load is not detected, or it returns to low-power mode (slumber mode) due to inactivity.

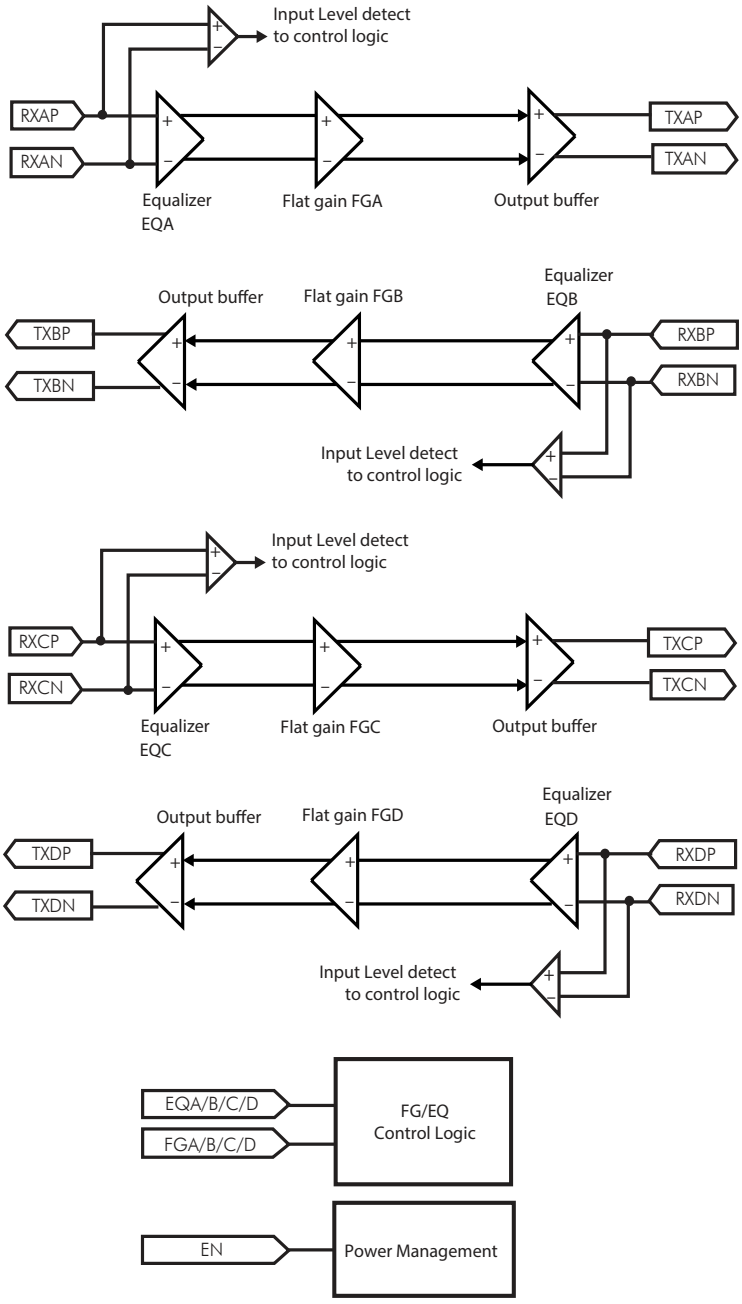
Figure 1



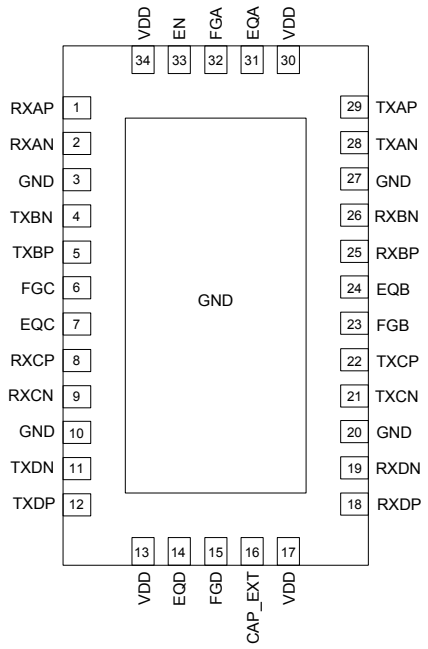
Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

ReDriver is a trademark of Diodes Incorporated.

Block Diagram



Pin Configuration



Pin Description

Pin #	Pin Name	Type	Description
13, 17, 30, 34	VDD	Power	3.3V power supply, ±0.3V
32, 23 6, 15	FGA, FGB FGC, FGD	Input	The DC flat gain selection. 4-level input pins. With internal 100kΩ pullup resistor and 200kΩ pulldown resistor.
31, 24 7, 14	EQA, EQB EQC, EQD	Input	The EQ selection. 4-level input pins. With internal 100kΩ pullup resistor and 200kΩ pulldown resistor.
1, 2 25, 26 8, 9 18, 19	RXAP, RXAN RXBP, RXBN RXCP, RXCN RXDP, RXDN	Input	CML input terminals. With selectable input termination between 50Ω to VDD, 270kΩ to VbiasRx, or 67kΩ to GND.
29, 28 5, 4 22, 21 12, 11	TXAP, TXAN TXBP, TXBN TXCP, TXCN TXDP, TXDN	Output	CML output terminals. With selectable output termination between 50Ω to VDD, 6kΩ to VDD, 6kΩ to VbiasTx or 67kΩ to GND.
33	EN	Input	Channel Enable. With internal 300kΩ pullup resistor. “High” – Channel is in normal operation. “Low” – Channel is in power down mode.
16	CAP_EXT	I/O	Decoupling Capacitor for Internal Bias.
3, 10, 20, 27, Center Pad	GND	GND	Supply Ground

Power Management

Notebooks, netbooks, and other power sensitive consumer devices require judicious use of power in order to maximize battery life. In order to minimize the power consumption of our devices, Diodes added an additional adaptive power management feature. When a signal detector is idle for longer than 1.3ms, the corresponding channel moves to low-power mode ONLY, which means both channels move to low-power mode individually.

In low-power mode, the signal detector continues monitoring the input channel. If a channel is in low-power mode and the input signal is detected, the corresponding channel wakes up immediately. If a channel is in low-power mode and the signal detector is idle longer than 6ms, the receiver detection loop is active again. If load is not detected, then the channel moves to device unplug mode and monitors the load continuously. If load is detected, it returns to low-power mode, and receiver detection is active again per 6ms.

Operating Modes

Mode	R_{IN}	R_{OUT}
PD	67kΩ to GND	67kΩ to GND
Unplug Mode	270kΩ to VbiasRx	6kΩ to VbiasTx
Deep Slumber Mode	50Ω to Vdd	6kΩ to VbiasTx
Slumber Mode	50Ω to Vdd	6kΩ to Vdd
Active Mode	50Ω to Vdd	50Ω to Vdd

Equalization Setting:

EQA/B/C/D are the selection pins for the equalization selection.

	Equalizer Settings (dB)	
EQA/B/C/D	*@ 2.5GHz*	*@ 5GHz*
0 (Tie 1KΩ to GND)	6.7	12.4
R (Tie 68KΩ to GND)	3.5	8.0
F (Leave Open)	5.3	10.6
1 (Tie 1KΩ to VDD)	8.4	14.6

Flat Gain Setting:

FGA/B/C/D are the selection pins for the DC gain.

	Flat Gain Settings
FGA/B/C/D	*dB*
0 (Tie 1KΩ to GND)	-1.6
R (Tie 68KΩ to GND)	-0.5
F (Leave Open)	1.0
1 (Tie 1KΩ to VDD)	2.7

Channel Enable Setting:

	Channel Enable Settings
EN	*Setting*
0	Disabled
1	Enabled (Default)

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....–65°C to +150°C
Supply Voltage to Ground Potential.....–0.5V to +3.8V
DC SIG Voltage.....–0.5V to V_{DD} +0.5V
Output Current .....–25mA to +25mA
ESD, Human Body Model .....-2kV to +2kV
Power Dissipation Continuous 1.2W
Max Junction Temperature.....125°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Control Pin Specifications (VDD = 3.3 ± 0.3V, TA = -40 to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
2-Level Control Pins					
V_{IH}	DC Input Logic High	VDD × 0.65	—	—	V
V_{IL}	DC Input Logic Low	—	—	VDD × 0.35	V
I_{IH}	Input High Current	—	—	25	µA
I_{IL}	Input Low Current	-25	—	—	µA
4-Level Control Pins					
V_{IH}	DC Input Logic "High"	0.92 × VDD	VDD	—	V
V_{IF}	DC Input Logic "Float"	0.59 × VDD	0.67 × VDD	0.75 × VDD	V
V_{IR}	DC Input Logic "With Rext to GND"	0.25 × VDD	0.33 × VDD	0.41 × VDD	V
V_{IL}	DC Input Logic "Low"	—	GND	0.08 × VDD	V
I_{IH}	Input High Current	—	—	50	µA
I_{IL}	Input Low Current	-50	—	—	µA
Rext	External Resistor Connects to GND (±5%)	64.6	68	71.4	kΩ

AC/DC Electrical Characteristics (VDD = 3.3 ± 0.3V TA = -40 to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Power and Latency						
$V_{dd-3.3}$	Supply Voltage		3.0	3.3	3.6	V
I_{active}	Active Mode Current Consumption	EN = 1, 10Gbps, compliance test pattern	—	260	334	mA
$I_{slumber}$	Slumber Mode Current Consumption	EN = 1, no input signal longer than $T_{slumber}$	—	32	38	mA
$I_{DeepSlumber}$	Deep Slumber Mode Current Consumption	EN = 1 no input signal longer than $T_{DeepSlumber}$	—	0.8	1.2	
I_{unplug}	Unplug Mode Current Consumption	EN = 1, no output load is detected	—	0.6	0.9	
I_{pd}	Power Down Mode Current Consumption	EN = 0	—	20	120	µA
t_{pd}	Latency	From input to output	—	—	2	ns

AC/DC Electrical Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
CML Receiver Input (100Ω Differential)						
Receiver Electrical Specification						
$C_{rxparasitic}$	The Parasitic Capacitor for RX	—	—	—	1.0	pF
$R_{RX-DIFF-DC}$	DC Differential Input Impedance	—	72	—	120	Ω
$R_{RX-SINGLE\_DC}$	DC Single Ended Input Impedance	DC impedance limits are need to guarantee RxDet. Measured with respect to GND over a voltage of 500mV max.	18	—	30	Ω
$Z_{RX-HIZ-DC-PD}$	DC Input CM Input Impedance for V>0 During Reset or Power Down	(Vcm=0 to 500mV)	25	—	—	kΩ
$C_{ac\_coupling}$	AC Coupling Capacitance	—	75	—	265	nF
$V_{RX-CM-AC-P}$	Common Mode Peak Voltage	AC up to 5GHz	—	—	150	mVpeak
$V_{RX-CM-DC-Active-Idle-Delta-P}$	Common Mode Peak Voltage $\lvert Avg_{uo}(\lvert V_{TX-D+} + V_{TX-D-}\rvert)/2\text{-}Avg_{u1}(\lvert V_{TX-D+} + V_{TX-D-}\rvert)/2\rvert$	Between U0 and U1. AC up to 5GHz	—	—	200	mVpeak
Transmitter Electrical Specification						
$V_{TX-DIFF-PP}$	Output Differential p-p Voltage Swing	Differential Swing $\lvert V_{TX-D+}\text{-}V_{TX-D-}\rvert$	—	—	1.2	Vppd
$R_{TX-DIFF-DC}$	DC Differential TX Impedance	—	72	—	120	Ω
$V_{TX-RCV-DET}$	The Amount of Voltage Change Allowed During RxDet	—	—	—	600	mV
$C_{ac\_coupling}$	AC Coupling Capacitance	—	75	—	265	nF
$T_{TX-EYE(10Gbps)}$	Transmitter Eye, Include all Jitter	At the silicon pad. 10Gbps	0.646	—	—	UI
$T_{TX-EYE(5Gbps)}$	Transmitter Eye, Include all Jitter	At the silicon pad. 5Gbps	0.625	—	—	UI
$T_{TX-DJ-DD(10Gbps)}$	Transmitter Deterministic Jitter	At the silicon pad. 10Gbps	—	—	0.17	UI
$T_{TX-DJ-DD(5Gbps)}$	Transmitter Deterministic Jitter	At the silicon pad. 5Gbps	—	—	0.205	UI
$C_{txparasitic}$	The Parasitic Capacitor for TX	—	—	—	1.1	pF
$R_{TX-DC-CM}$	Common mode DC Output Impedance	—	18	—	30	Ω
$V_{TX-DC-CM}$	The Instantaneous Allowed DC Common Mode Voltage at Connector Side of the AC Coupling Capacitors	Min1 is with 200kΩ single ended receiver load respectively.	-0.5	—	1	V
		Min2 is with 50Ω single ended receiver load respectively.	-0.3	—	1	
V_{TX-C}	Common-Mode Voltage	$\lvert V_{TX-D+}+V_{TX-D-}\rvert/2$	VDD-2	—	VDD	V
$V_{TX-CM-AC-PP-Active}$	Active Mode TX AC Common Mode Voltage	$V_{TX-D+}+V_{TX-D-}$ for both time and amplitude	—	—	100	mVpp
$V_{TX-CM-DC-Active\_Idle-Delta}$	Common Mode Delta Voltage $\lvert Avg_{uo}(\lvert V_{TEX-D+} + V_{TX-D-}\rvert)/2\text{-}Avg_{u1}(\lvert V_{TX-D+} + V_{TX-D-}\rvert)/2\rvert$	Between U0 to U1	—	—	200	mV-peak

AC/DC Electrical Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{TX\text{-}Idle\text{-}Diff\text{-}AC\text{-}pp}$	Idle Mode AC Common Mode Delta Voltage $\|V_{TX\text{-}D+}\text{-}V_{TX\text{-}D\text{-}}\|$	Between Tx+ and Tx- in idle mode. Use the HPF to remove DC components. =1/LPF. No AC and DC signals are applied to Rx terminals .	—	—	10	mVppd
$V_{TX\text{-}Idle\text{-}Diff\text{-}DC}$	Idle Mode DC Common Mode Delta Voltage $\|V_{TX\text{-}D+}\text{-}V_{TX\text{-}D\text{-}}\|$	Between Tx+ and Tx- in idle mode. Use the LPF to remove DC components. =1/HPF. No AC and DC signals are applied to Rx terminals.	—	—	10	mV
Channel Performance						
G_p	Peaking Gain (Compensation at 5GHz, Relative to 100MHz, 100$mV_{p\text{-}p}$ Sine Wave Input)	EQx=0 EQx=R EQx=F EQx=1	—	12.4 8.0 10.6 14.6	—	dB
		Variation around typical	-3	—	+3	dB
G_F	Flat Gain (100MHz, EQx=F)	FQx=0 FQx=R FQx=F FQx=1	—	-1.6 -0.5 1.0 2.7	—	dB
		Variation around typical	-3	—	+3	dB
V_{SW_100M}	-1dB Compression Point Output Swing (at 100MHz)	—	—	1000	—	mVppd
V_{SW_5G}	-1dB Compression Point Output Swing (at 5GHz)	—	—	850	—	mVppd
DDNEXT	Differential Near-End Crosstalk(1)	100MHz to 5GHz, Figure 2	—	-40	—	dB
$V_{noise\text{-}input}$	Input-Referred Noise	100MHz to 5GHz, FGx=1, EQx=R, Figure 5	—	0.6	—	mV_{RMS}
		100MHz to 5GHz, FGx=1, EQx=1, Figure 5	—	0.5	—	
$V_{noise\text{-}output}$	Output-Referred Noise(2)	100MHz to 5GHz, FGx=1, EQx=R, Figure 5	—	0.8	—	mV_{RMS}
		100MHz to 5GHz, FGx=1, EQx=1, Figure 5	—	1	—	
Signal and Frequency Detectors						
V_{th_upm}	Unplug Mode Detector Threshold	Threshold of LFPS when the input impedance of the redriver is 67kΩ to VbiasRx only. Used in the unplug mode.	200	—	800	mVppd
V_{th_dsm}	Deep Slumber Mode Detector Threshold	LFPS signal threshold in deep slumber mode	100	—	600	mVppd

AC/DC Electrical Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{th_am}	Active Mode Detector Threshold	Signal threshold in active and slumber mode	45	—	175	mVppd
F_{th}	LFPS Frequency Detector	Detect the frequency of the input CLK pattern	100	—	400	MHz
External Decoupling Capacitor value						
CAP_EXT	External decoupling capacitor for the internal bias		2.2	—	20	uF

Note:

1. Measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.
2. Guaranteed by design and characterization.

Power-up/Power-down Timing and VCM Ramp Rate

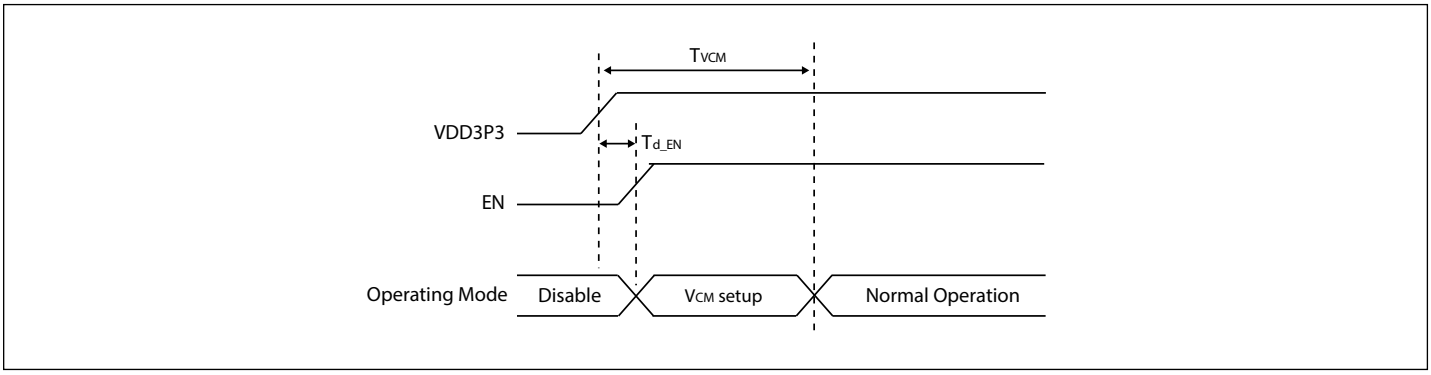


Figure 2. Power-up Timing

Power-up Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T_{d_EN}	VDD3P3 to EN assertion delay time		0			ms
T_{VCM}	Stabilization time for VCM common mode voltage			330	400	ms

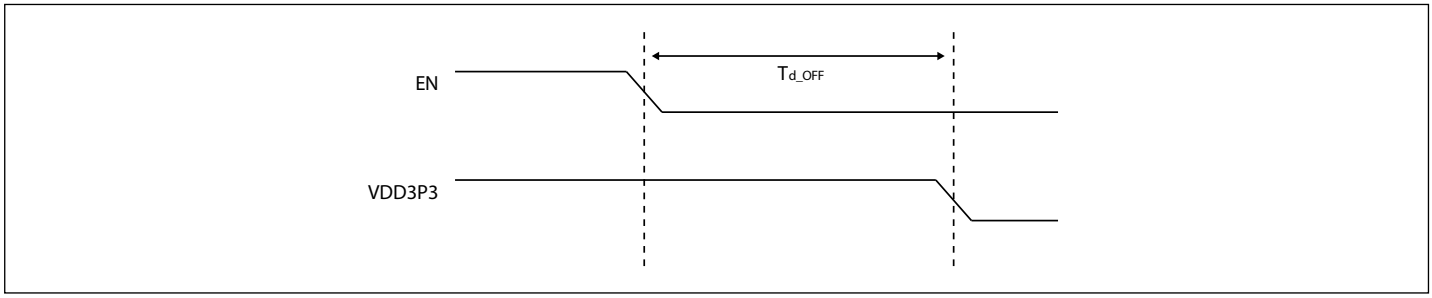


Figure 3. Power-down Timing

Power-down Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T_{d_OFF}	Delay time from EN de-assertion to VDD3P3 power off		900			ms

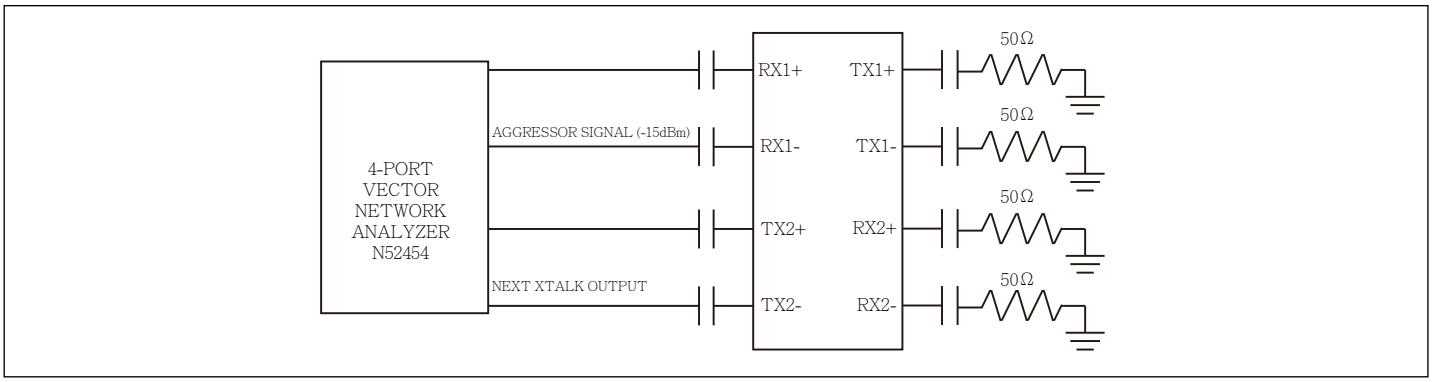


Figure 4. Channel-Isolation Test Configuration

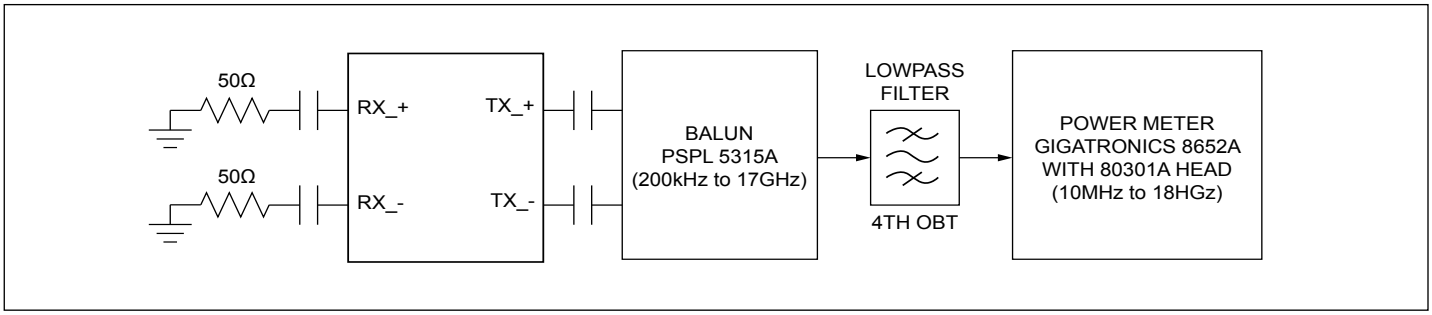


Figure 5. Noise Test Configuration

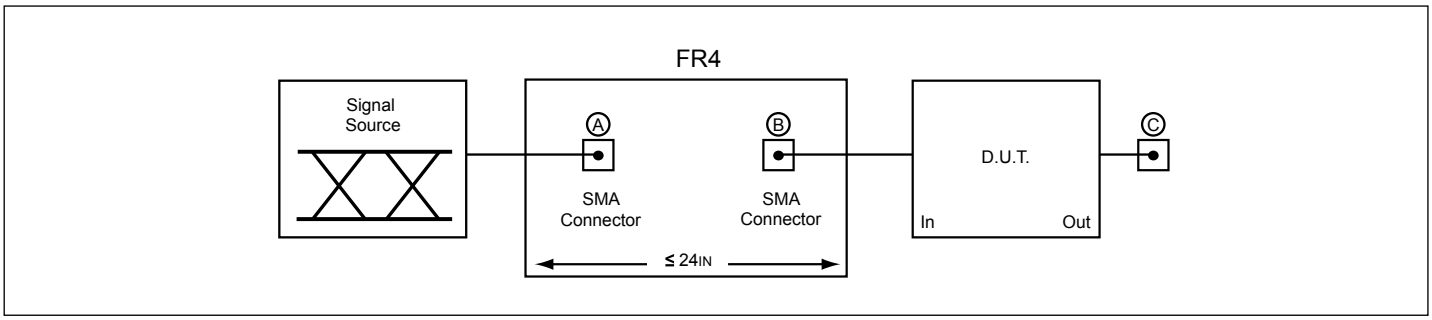
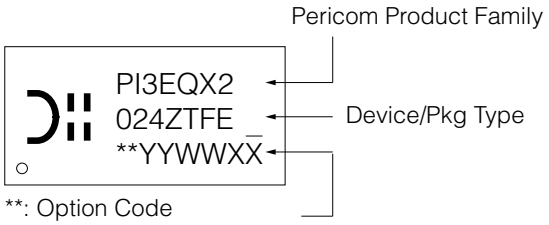


Figure 6. Test Condition Referenced in the Electrical Characteristic Table

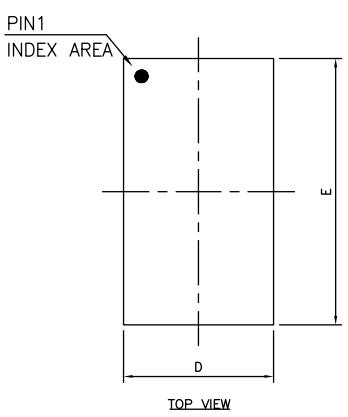
Part Marking

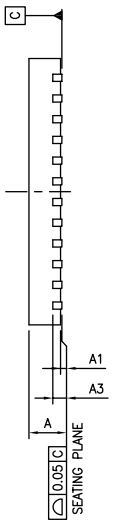


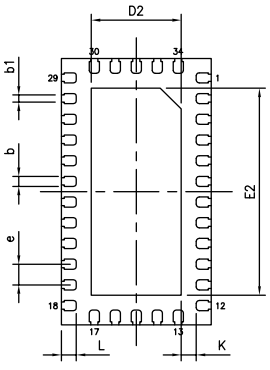
**: Option Code
YY: Date Code (Year)
WW: Date Code (Workweek)
1st X: Assembly Code
2nd X: Fab Code
Bar above 2nd "X" means Cu wire
Note: Date Code per MA-1251

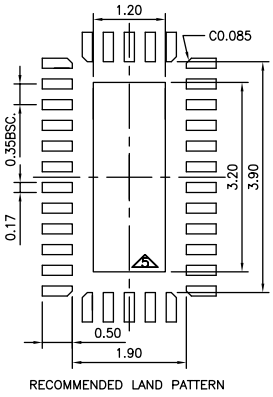
Packaging Mechanical

34-UQFN (ZTF)









SYMBOLS	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.150 REF.	
b	0.12	0.17	0.22
b1	0.07	0.12	0.17
D	2.40	2.50	2.60
E	4.40	4.50	4.60
e		0.35 BSC	
L	0.20	0.25	0.30
K	0.20	—	—
D2	1.45	1.50	1.55
E2	3.45	3.50	3.55

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-288
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

DATE: 06/07/21

DESCRIPTION: 34-Contact, Ultra Thin Quad Flat No-Lead (UQFN), U-QFN2545-34

PACKAGE CODE: ZTF (ZTF34)

DOCUMENT CONTROL #: PD-2230 REVISION: B

21-1403

For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Ordering Information

Ordering Number	Package Code	Package Description
PI3EQX2024ZTFEX	ZTF	34-Contact, Ultra Thin Quad Flat No-Lead (UQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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