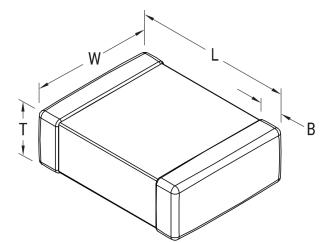


C1812T103J5GCLTU

Aliases (C1812T103J5GCL7800)

SMD COTS COG, Ceramic, 0.01 uF, 5%, 50 VDC, COG, SMD, MLCC, COTS, Ultra-Stable, Low Loss, Class I, 1812



Click here for the 3D model.

Dimensions	
Chip Size	1812
L	4.5mm +/-0.3mm
W	3.2mm +/-0.3mm
Т	1mm +/-0.10mm
В	0.6mm +/-0.35mm

Packaging Specifications	kaging Specifications	
Packaging	T&R, 180mm, Plastic Tape	
Packaging Quantity	1000	

General Informatio	n
Series	SMD COTS COG
Style	SMD Chip
Description	SMD, MLCC, COTS, Ultra-Stable, Low Loss, Class I
Features	Ultra-Stable, Low Loss, Class I
RoHS	No
Prop 65	A WARNING: Cancer and reproductive harm - http://www.p65warnings.ca.gov.
SCIP Number	2d771165-5336-48a3-96fa-3663929fd828
Termination	Lead (SnPb)
Marking	No
Failure Rate	Testing per MIL-PRF-55681 PDA 8%, DPA per EIA- 469, Humidity per MIL-STD-202, Method 103, Condition A
AEC-Q200	No
Component Weight	67 mg
Shelf Life	78 Weeks
MSL	1

Specifications				
Capacitance	0.01 uF			
Measurement Condition	1 kHz 1.0Vrms			
Capacitance Tolerance	5%			
Voltage DC	50 VDC			
Dielectric Withstanding Voltage	125 VDC			
Temperature Range	-55/+125°C			
Temperature Coefficient	COG			
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	30 ppm/C, 1kHz 1.0Vrms			
Dissipation Factor	0.1% 1 kHz 1.0Vrms			
Aging Rate	0% Loss/Decade Hour			
Insulation Resistance	100 GOhms			

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.