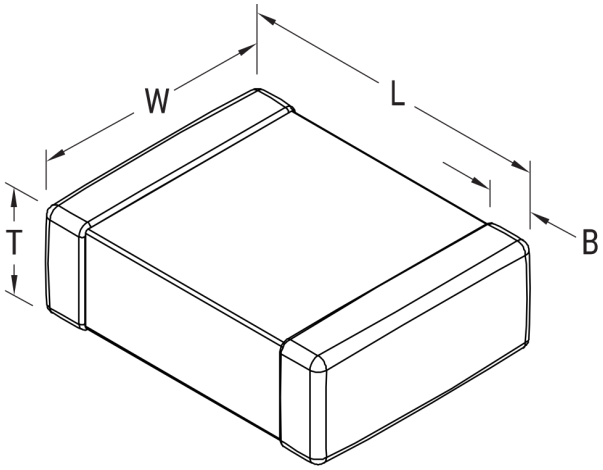
C1812T103J5GCLTU

Aliases (C1812T103J5GCL7800)

SMD COTS C0G, Ceramic, 0.01 uF, 5%, 50 VDC, C0G, SMD, MLCC, COTS, Ultra-Stable, Low Loss, Class I, 1812



Click here for the 3D model.

Dimensions	
Chip Size	1812
L	4.5mm +/-0.3mm
W	3.2mm +/-0.3mm
T	1mm +/-0.10mm
B	0.6mm +/-0.35mm

Packaging Specifications	
Packaging	T&R, 180mm, Plastic Tape
Packaging Quantity	1000

General Information	
Series	SMD COTS C0G
Style	SMD Chip
Description	SMD, MLCC, COTS, Ultra-Stable, Low Loss, Class I
Features	Ultra-Stable, Low Loss, Class I
RoHS	No
Prop 65	⚠ **WARNING:** Cancer and reproductive harm - http://www.p65warnings.ca.gov.
SCIP Number	2d771165-5336-48a3-96fa-3663929fd828
Termination	Lead (SnPb)
Marking	No
Failure Rate	Testing per MIL-PRF-55681 PDA 8%, DPA per EIA-469, Humidity per MIL-STD-202, Method 103, Condition A
AEC-Q200	No
Component Weight	67 mg
Shelf Life	78 Weeks
MSL	1

Specifications	
Capacitance	0.01 uF
Measurement Condition	1 kHz 1.0Vrms
Capacitance Tolerance	5%
Voltage DC	50 VDC
Dielectric Withstanding Voltage	125 VDC
Temperature Range	-55/+125°C
Temperature Coefficient	C0G
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	30 ppm/C, 1kHz 1.0Vrms
Dissipation Factor	0.1% 1 kHz 1.0Vrms
Aging Rate	0% Loss/Decade Hour
Insulation Resistance	100 GOhms