AOZ29303QI

30 V 3A Step-Down Integrated DC-DC Power Module

General Description

The AOZ29303QI is a versatile, wide operating range, high-efficiency, easy-to-use power module that integrates a buck converter, inductor, and passive components into a compact QFN package. The highly integrated solution significantly simplifies design efforts and enables faster time to market. The AOZ29303QI works from a wide input range of 4.5 V to 30 V and provides up to 3A of continuous output current. It supports high duty cycle operation up to 87%.

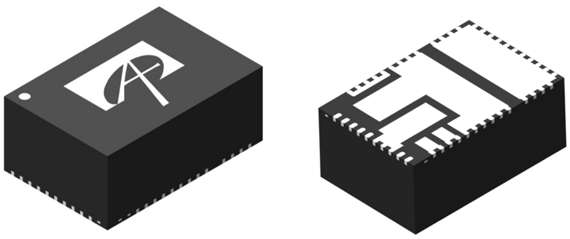
This power module is configurable using a few external components. Output voltage can be set by using a resistor divider. Soft start is programmable using an external capacitor. The switching frequency can be set from 200 kHz to 1 MHz with an external resistor. External compensation allows the user to optimize the module for a wide range of transient response requirements and output capacitance.

Features

- Versatile
  - 4.5 V to 30 V operating input voltage range
  - 0.8 V to 5.5 V adjustable output voltage
  - 87% high duty cycle operation support
- High-efficiency
  - Up to 93% peak efficiency
  - 10 µA shut down current
- Highly configurable
  - Adjustable soft start
  - 200 kHz to 1 MHz adjustable switching frequency
  - External compensation for control loop optimization
- Protection features
  - Cycle-by-cycle over current protection
  - Output short-circuit protection
  - Output over voltage protection
  - Over temperature protection
- Package
  - QFN 9 mm x 6 mm x 3.7 mm - 48L

Applications

- Industrial and commercial low power systems
- Aftermarket auto accessories
- Networking/Datacom equipment
- High voltage battery application



Typical Application

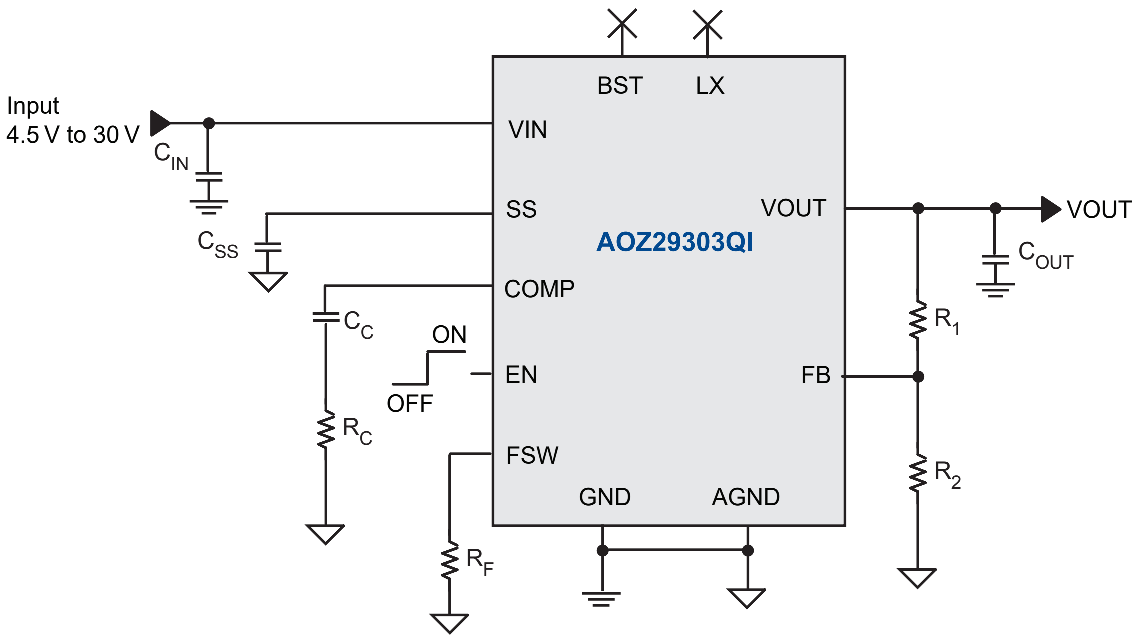


Figure 1. Typical Application AOZ29303QI

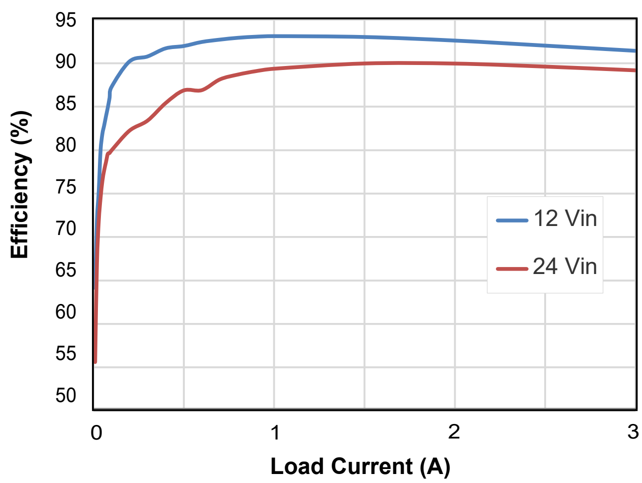


Figure 2. Efficiency vs. Load Current (Vout = 5 V, 500 kHz)

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ29303QI	-40°C to +85°C	QFN9x6-48L	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

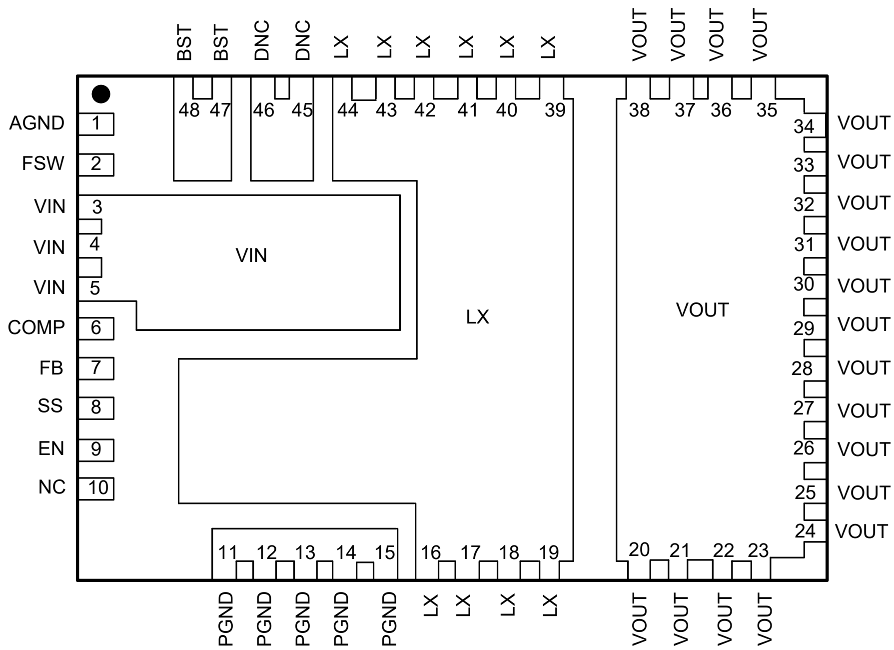


Figure 3. AOZ29303 QFN9x6 - 48L

(Top Transparent View)

Pin Description

Pin Number	Pin Name	Pin Function
1	AGND	Analog Ground. All control component return path is connected to AGND. Connect to the common GND.
2	FSW	Frequency Select Pin. Connect to a resistor R_F to AGND to set switching frequency.
3, 4, 5	VIN	Input Supply Voltage. Connect these pins to the input supply and connect C_{IN} to common GND. When VIN rises above the UVLO threshold the device starts up.
6	COMP	Loop Compensation Pin. Connect a resistor R_C and capacitor C_C to optimize the loop stability and transient response.
7	FB	Output Voltage Feedback Pin. Connect to a resistor divider network R_1 and R_2 between VOUT and AGND.
8	SS	Soft Start Pin. Connect to a capacitor C_{SS} to AGND to set the soft start time.
9	EN	Enable Pin. Enable logic is active high. Do not leave the EN pin floating.
10	NC	No Connect.
11, 12, 13, 14, 15	PGND	Power Ground. Connect to common GND.
16, 17, 18, 19, 39, 40, 41, 42, 43, 44	LX	Switching Node. For testing only and these pins should be left floating.
20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38	VOUT	Output Voltage. They are connected to the integrated inductor. Connect these pins to output capacitor C_{OUT} and load.
45, 46	DNC	Do Not Connect. Internally connected to LX. These pins should be left floating.
47,48	BST	Bootstrap Voltage Pin. For testing only and these pins should be left floating.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Supply Voltage (VIN)	32 V
LX to GND (1)	-0.7 V to VIN + 0.3 V
EN, SS, FB and COMP to GND (1)	-0.3 V to +6 V
BST to GND (1)	-0.3 V to LX +6 V
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating (2)	±1.5 kV

Notes:

1. GND is common ground connected to AGND and PGND.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5 kΩ in series with 100 pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (VIN)	4.5 V to 30 V
Output Voltage (VOUT)	0.8 V to 5.5 V
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance QFN9x6-48L (Θ_{JA})	19.3°C/W

Electrical Characteristics

T_A = 25°C, VIN = 12 V, EN = 3 V, VOUT = 3.3 V unless otherwise specified. Specifications in **BOLD** indicate ambient temperature range of -40°C to +85°C. These specifications are guaranteed by design.

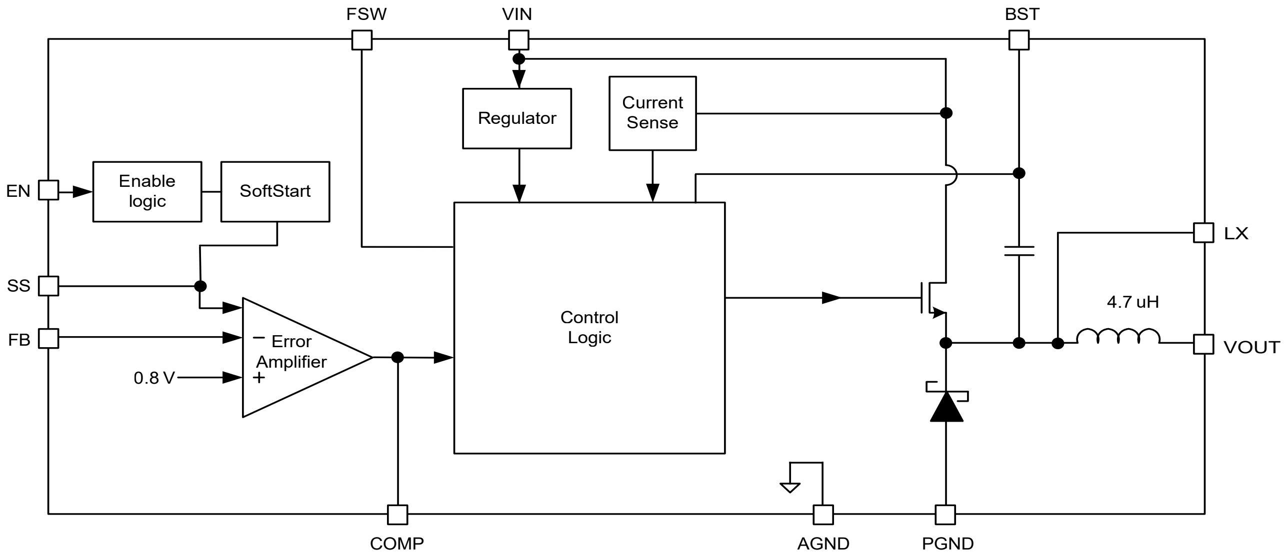
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Supply Voltage		**4.5**		**30**	V
V_{UVLO}	Input Under-Voltage Lockout Threshold	VIN rising			2.9	V
		VIN falling	2.3			V
I_{IN}	Quiescent Supply Current	I_{OUT} = 0A, FB = 1 V		**1**	**1.5**	mA
I_{OFF}	Shutdown Supply Current	EN = 0 V			10	µA
V_{FB}	Feedback Reference Voltage		788	800	812	mV
R_O	Load Regulation	0.5A < I_{OUT} < 3A		0.5		%
S_V	Line Regulation	VIN = 5 V to 30 V, I_{OUT} = 1 A		0.5		%
I_{FB}	Feedback Voltage Input Current	FB = 800 mV		0.5	1	µA
Enable						
V_{EN}	EN Input Threshold	On Threshold	**1.2**			V
		Off Threshold			**0.4**	V
V_{EN_HYS}	EN Input Hysteresis	Enable Falling		200		mV
Soft Start						
I_{SS}	Soft Start Source Current	SS = 0 V		2.5		µA

Electrical Characteristics *(Continued)*

T_A = 25°C, VIN = 12 V, EN = 3 V, VOUT = 3.3 V unless otherwise specified. Specifications in **BOLD** indicate ambient temperature range of -40°C to +85°C. These specifications are guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Modulator						
F_S	Switching Frequency	R_F = 270 kΩ	160	200	240	kHz
		R_F = 100 kΩ	400	500	600	kHz
		R_F = 46.6 kΩ	800	1000	1200	kHz
D_{MAX}	Maximum Duty Cycle	Fs = 1 MHz		87		%
t_{ON_MIN}	Minimum On Time			150		ns
Output Current						
I_{LIM}	Current Limit Threshold	VIN = 12 V, VOUT = 1 V, Fs = 200 kHz		4.7		A
V_{FB_CP}	FB Voltage Threshold for Short -Circuit Protection			0.2		V
Thermal Protection						
T_{SD}	Thermal Shutdown Threshold	Temperature Rising		145		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis	Temperature Falling		45		°C

Functional Block Diagram



Typical Characteristics

$T_A = 25°C$, VIN = 24 V, EN = 5 V, VOUT = 5 V unless otherwise specified.

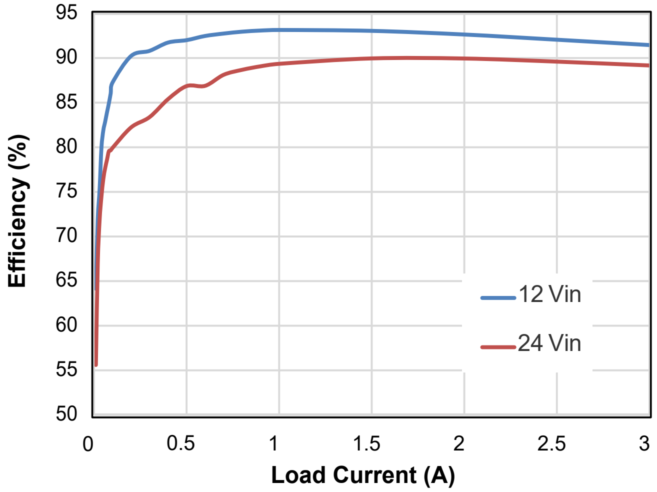


Figure 4. Efficiency at VOUT = 5 V, 500 kHz

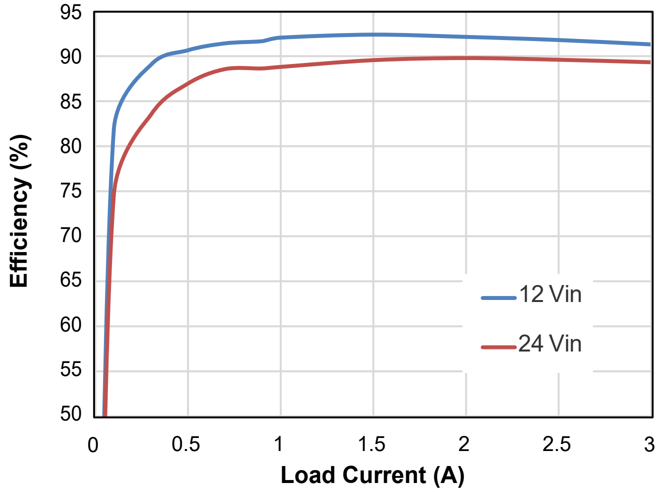


Figure 5. Efficiency at VOUT = 5 V, 400 kHz

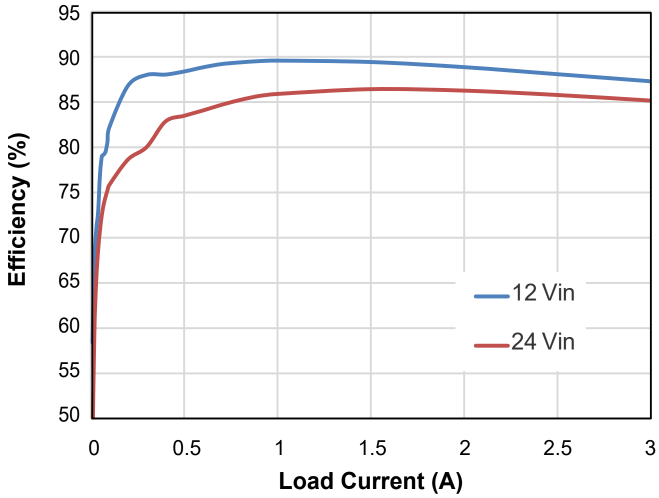


Figure 6. Efficiency at VOUT = 3.3 V, 500 kHz

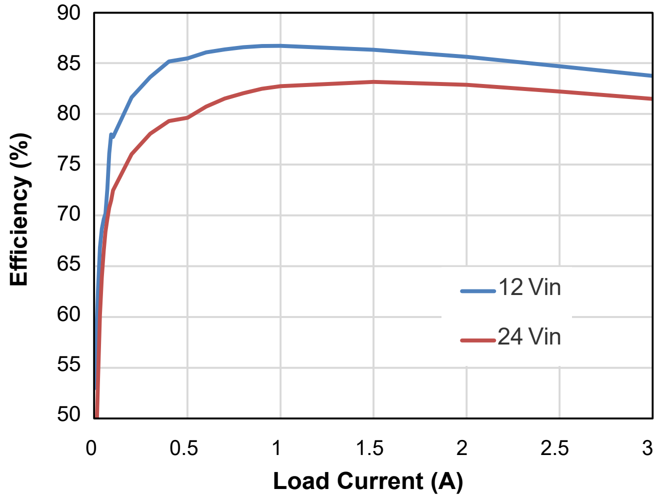


Figure 7. Efficiency at VOUT = 2.5 V, 400 kHz

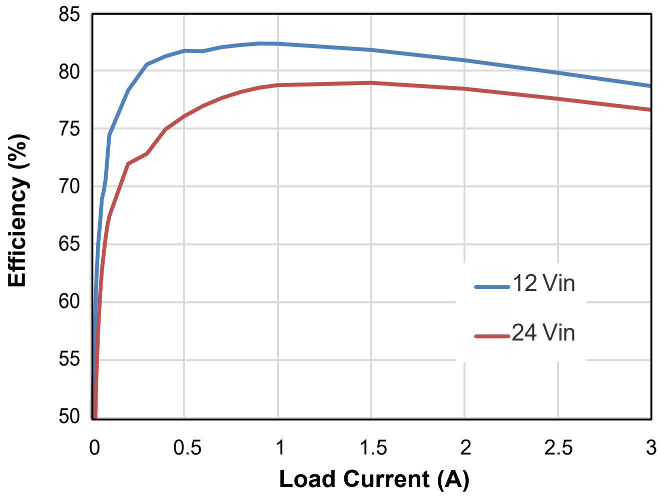


Figure 8. Efficiency at VOUT = 1.8 V, 300 kHz

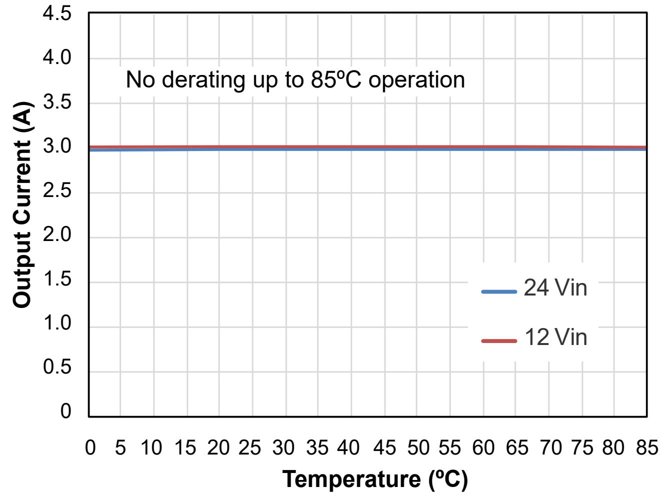


Figure 9. Power Derating with Temperature for 5 VOUT, 3.3 VOUT, 1 VOUT

Typical Characteristics

$T_A = 25°C$, VIN = 24 V, EN = 5 V, VOUT = 5 V unless otherwise specified.

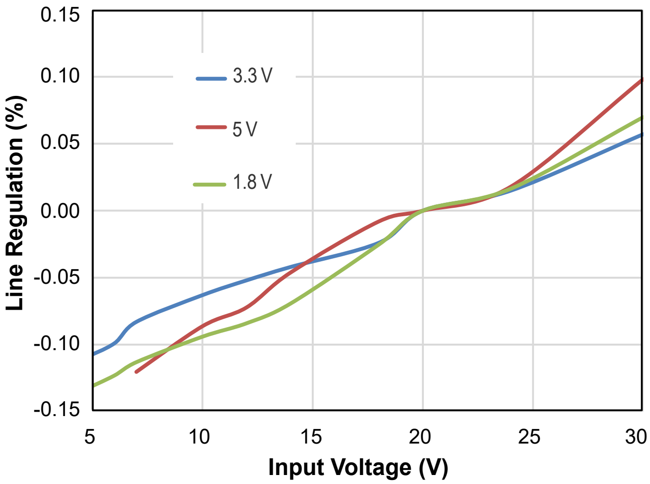


Figure 10. Line Regulation I_{OUT} = 1 A

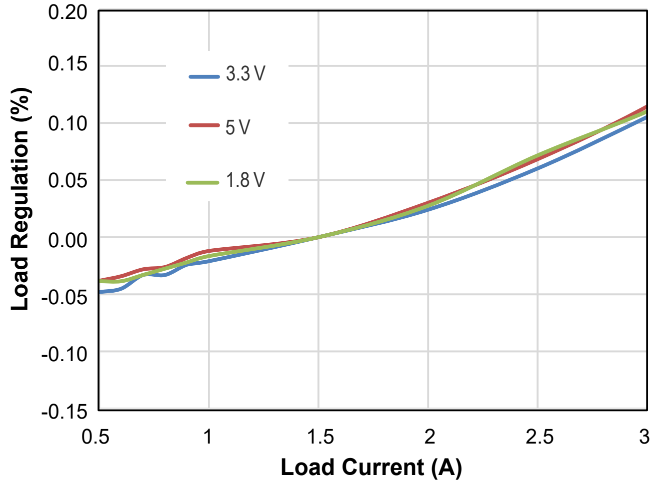


Figure 11. Load Regulation VIN = 12 V

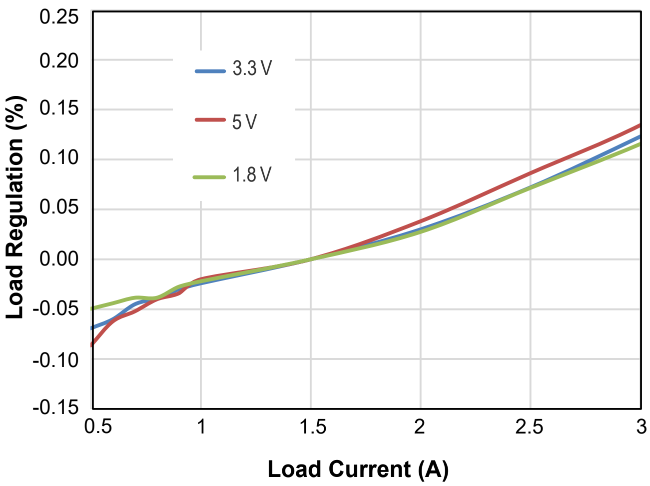


Figure 12. Load Regulation VIN = 24 V

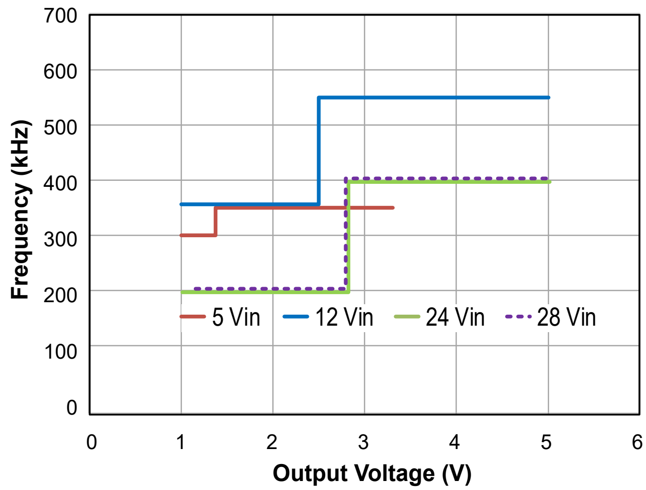
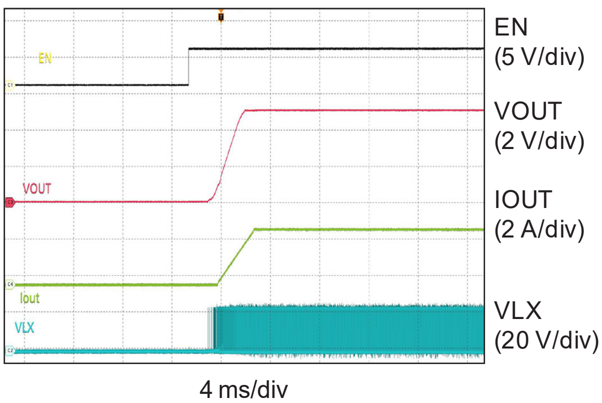


Figure 13. Recommended Frequency vs. VIN at VOUT

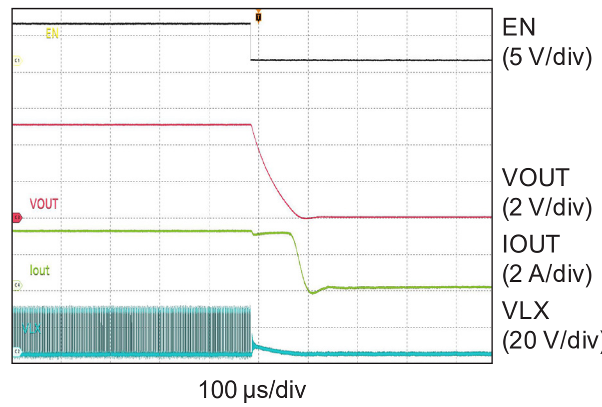
Typical Characteristics

$T_A = 25°C$, VIN = 24 V, EN = 5 V, VOUT = 5 V unless otherwise specified.

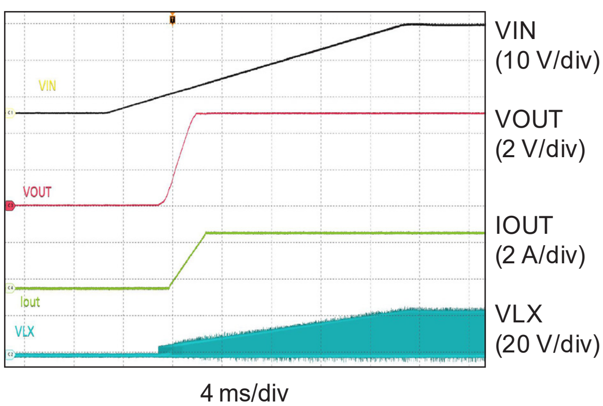
Start-up by EN to Full Load



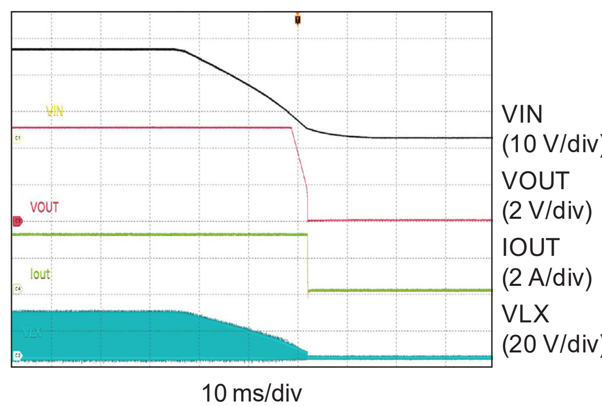
Shut-down by EN from Full Load



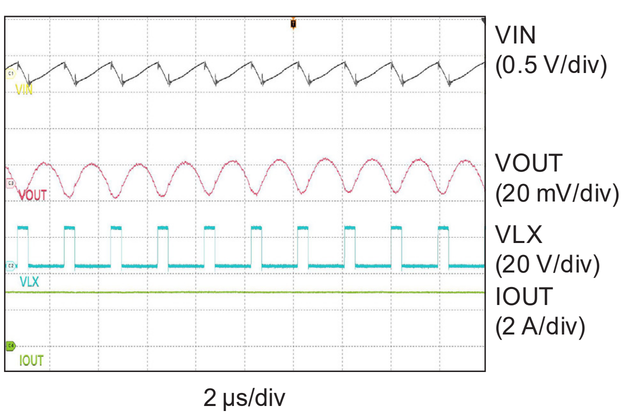
Start-up by VIN to Full Load



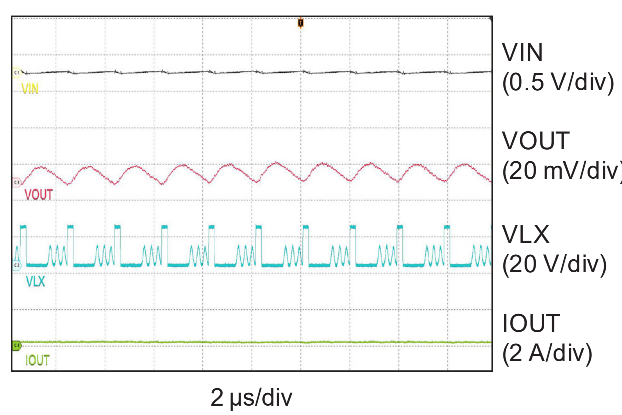
Shut-down by VIN from Full Load



Full Load 3 A Operation



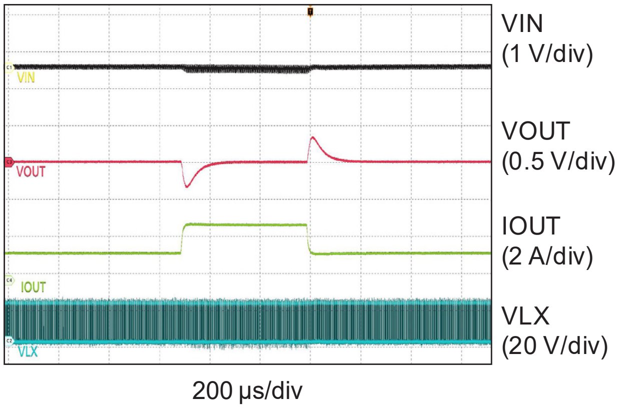
Light Load 250 mA Operation



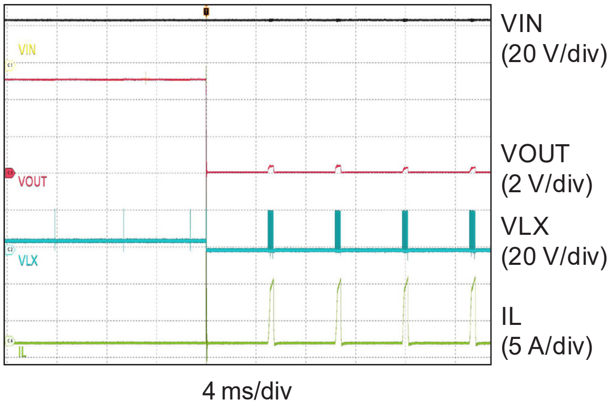
Typical Characteristics

$T_A = 25°C$, VIN = 24 V, EN = 5 V, VOUT = 5 V unless otherwise specified.

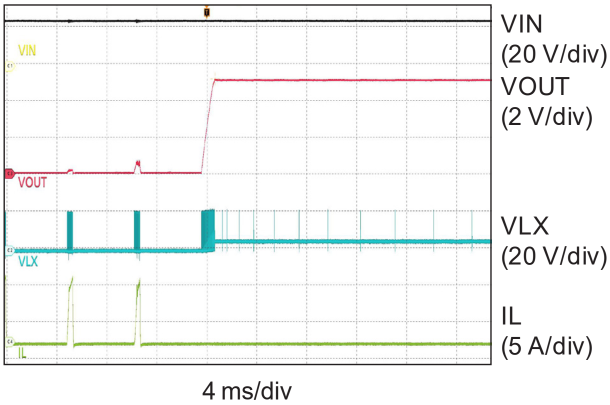
Transient from 1.5 A to 3 A



Output Short Circuit Protection



Output Short Circuit Recovery



Detailed Description

The AOZ29303QI is a power module which includes a current-mode step-down voltage regulator with integrated inductor and passive components. It operates from 4.5V to 30V input voltage range and supplies up to 3A of continuous load current. Features include enable control, power-on reset, input under voltage lockout, external soft start control, cycle-by-cycle current limit and thermal protection shut down. The circuit details can be referred to functional block diagram.

The AOZ29303QI is available in QFN 9mm x 6mm x 3.7mm package.

Enable and Soft Start

The AOZ29303QI has external soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when the input voltage rises to 2.9V and voltage on EN is >1.2V. In the soft start process, a 2.5μA internal current source charges the external capacitor (C_{SS}) at SS pin. As the SS capacitor is being charged, the voltage at SS will rise monotonically. The soft start ramp up time can be calculated by the following equation:

$$t_{SS} = 0.48 \times C_{SS}$$

where C_{SS} is soft start capacitance (nF) and t_{SS} is soft start time (ms).

The SS voltage acts like the reference voltage for the error amplifier during soft start and output voltage will follow the SS voltage ramp. The slow ramping up of output voltage is necessary to prevent high inrush current. Minimum external soft start capacitor 2.2nF is required. A typical soft start capacitance is recommended in Table 1. The very large soft start capacitance will have the long start-up time or restart-up time for OCP and SCP, which can cause the large FET, diode power dissipation and could adversely impact the reliability of power FET and diodes. The maximum external soft start capacitor is 10nF and the corresponding soft start time is about 5ms. A soft start time vs capacitance is shown in Figure 14.

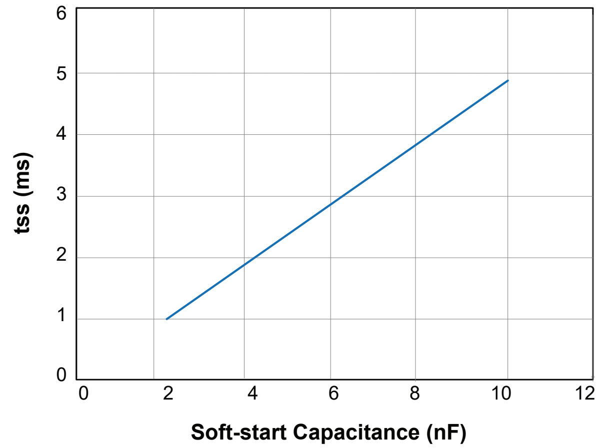


Figure 14. Soft-start Time vs. SS Capacitance

The EN pin of the AOZ29303QI is active high. The voltage on EN pin must be above 1.2V to enable the module. When voltage on EN pin falls below 0.4V, the module is disabled. Do not leave it open. The EN pin can connect to the input through a resistor divider. A resistor network (R_{EN1}, R_{EN2}) is used to set the input voltage enable threshold in Figure 15. The default on-board values for the R_{EN1} is 68kΩ and R_{EN2} is 10kΩ, which set the VIN enable rising threshold to 9.4V. These thresholds can be adjusted based on the below equations. It is recommended to use R_{EN1} with value <500kΩ

$$V_{IN\_EN} = 1.2 \times \left(1 + \frac{R_{EN1}}{R_{EN2}}\right)$$

where V_{IN_EN} is the VIN enable rising threshold.

For external enable drive, a resistor is required to be in series connection with external voltage source. A typical resistance is 10kΩ.

Light Load and PWM Operation

Under low output current condition, AOZ29303QI will operate in Pulse Energy Mode (PEM) to achieve high-efficiency. Under PEM operation, the PWM will not turn off until the on-time gets a fixed time which is defined by input voltage (VIN), output voltage (VOUT), and switching frequency. This would significantly reduce the switching frequency of the modulator to reduce power loss.

Steady-State Operation

Under steady-state condition, the module operates in fixed frequency and Continuous Conduction Mode (CCM).

The AOZ29303QI integrates an internal N-MOSFET as the High-Side switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the High-Side MOSFET. Since the N-MOSFET requires a gate voltage higher than the input voltage, a boost capacitor (C_{BOOT}) connected between LX and BST is integrated to drive the gate. The boost capacitor is charged while LX is low. An internal 10 Ω switch from LX to GND to pull the LX to GND even under the light load. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and internal reference (0.8 V) is amplified by the internal transconductance error amplifier. The error voltage, which shows on the COMP pin, is compared against the current signal from High-Side switch at PWM comparator input. At the beginning of each clock, High-Side switch will be turned on. The inductor current flows from the input through the inductor to the output. When the current signal exceeds the error voltage, the High-Side switch turns off. The inductor current is then freewheeling through the Schottky diode from PGND to LX.

Switching Frequency

The AOZ29303QI switching frequency can be programmed by using an external resistor at FSW. External resistor value can be calculated by following equation:

$$R_F(k\Omega) = \frac{50{,}000}{f_S(kHz)} - 5\,k\Omega$$

Output Voltage Programming

Output voltage can be set by feeding back the output to the FB pin with a resistor divider network in the application circuit shown in Figure 15. The resistor divider network includes R_1 and R_2. Usually, a design is started by picking a fixed R_2 value and calculating the required R_1 with equation below:

$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Some standard value of R_1, R_2 for most commonly used output voltage values are listed in Table 1. Combination of R_1 and R_2 should be large enough to avoid drawing excessive current from the output, which cause additional power loss.

Protection Features

The AOZ29303QI has multiple protection features to prevent system circuit damage under abnormal conditions.

Over Current Protection (OCP)

The cycle-to-cycle current limit threshold is internally set. When the peak load current reaches the current limit threshold, the cycle-to-cycle current limit circuit turns off the High-Side switch to terminate the current duty cycle. When cycle-to-cycle current limit circuit is triggered, the output voltage will drop if the load demand is higher than the average current.

Short-Circuit Protection (SCP)

The AOZ29303QI has internal short-circuit protection to protect itself from catastrophic failure under output short-circuit conditions. The FB voltage is proportional to the output voltage. Whenever FB voltage is below 0.2 V, the short-circuit protection circuit is triggered. FET is turned off, output voltage and inductor current discharge to zero. After the controller shuts off for about 6 ms, module will try to restart. It'll shut down again if the short-circuit still exists. The module works in hiccup mode under short-circuit condition.

Power-On Reset (POR)

A power-on reset circuit monitors the input voltage VIN. When the input voltage exceeds 2.9 V, the module starts the operation if EN is high. When input voltage falls below 2.3 V, the converter will stop switching.

Thermal Protection

An internal temperature sensor monitors the junction temperature of the controller. The High-Side switch will turn off if the junction temperature exceeds 145ºC. The regulator will restart automatically under the control of soft start circuit when the junction temperature decreases to 100°C.

Application Information

A 5 V output typical application circuit is shown in Figure 15. Components selection for most applications are listed in Table 1. User should select the components value by input and output voltage from Table 1.

Input and Output Capacitor Selection

To ensure loop stability, low noise, and good transient system performance, minimum input and output capacitance are recommended in Table 1.

Ceramic capacitors are usually chosen for input and output capacitors due to small size and low ESR. The types of ceramic capacitors should be X5R or X7R for stable temperature characteristics and acceptable derating at applied voltage.

Input ceramic capacitor (C_{IN}) should have the enough voltage rating, which must be higher the maximum input voltage. The margin is at least 20% higher the applied voltage due to the derating voltage value of ceramic capacitors. A 68 µF input non-ceramic capacitor is recommended for system with long wire to the power module.

Output ceramic capacitors (C_{OUT}) should have voltage rating higher than output voltage and have at least 20% voltage margin. The capacitance derating under DC bias and temperature variation must be considered. Additional capacitor can be ceramic or low ESR polymer electrolytic. The more output capacitance will reduce the output ripple voltage and improve the load transient response. A large output capacitance will increase the start-up inrush current, so the bigger soft start capacitor may be used and the loop gain needs to be checked to ensure the stability.

Frequency Selection

The switching frequency can be set by an external resistor (R_F) from FSW to AGND. A frequency setting is recommended in Table 2 based on input and output voltage condition. Inductor ripple current is function of switching frequency, which can be calculated by the following equation:

$$\Delta I_L = \frac{(V_{IN} - V_0) * V_0}{L * V_{IN} * f_S}$$

Where L is the output inductance (=4.7 µH),
f_S is the switching frequency,
V_{IN} is the input voltage,
V_O is the output voltage.

Output ripple voltage is also a function of switching frequency, inductor value, output capacitor value, and ESR resistance. It can be calculated by the following equation:

$$\Delta V_0 = \Delta I_L \times \left(ESR_{CO} + \frac{1}{8 \times f_S \times C_O} \right)$$

Where C_O is the output filter capacitor,
ESR_{CO} is the equivalent series resistance of output, capacitor.

If the frequency is set too low, it causes higher ripple current and voltage. The high peak current may trigger OCP before the output reach full load. If the frequency is set too high, switching power loss will be higher and lower efficiency which leads to the higher temperature of the module. The highest frequency is also limited by the minimum on-time of controller. Figure 13 is the frequency selection guide at different operating conditions for best operation and Table 2 for frequency setting range at each output voltage.

Loop Compensation

External compensation is available to optimize the system stability and transient performance. A resistor (R_C) and a capacitor (C_C) are connected from COMP to AGND. The compensation resistance and capacitance values are recommended in Table 1 for stability and fast dynamic response for given conditions.

The AOZ29303 employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole and can be calculated by:

$$f_{P1} = \frac{1}{2\pi \times C_0 \times R_L}$$

The zero is a ESR zero due to output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_0 \times ESR_{CO}}$$

Where C_O is the output filter capacitor,
R_L is load resistor value,
ESR_{CO} is the equivalent series resistance of output, capacitor.

The compensation design is actually to shape the converter close loop transfer function to get desired gain and phase. Several different types of compensation network can be used for AOZ29303. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ29303, FB pin and COMP pin are the inverting input and the output of internal transconductance error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{P2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

Where G_{EA} is the error amplifier transconductance, which is $200 \cdot 10^{-6}$ A/V;
G_{VEA} is the error amplifier voltage gain, which is 500 V/V;
C_C is compensation capacitor.

The zero given by the external compensation network, capacitor C_C and resistor R_C in Figure 15, is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

To design the compensation circuit, a target crossover frequency f_C for close loop must be selected. The system crossover frequency is where control loop has unity gain. The crossover frequency is also called the converter bandwidth. Generally, a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high due to system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be less than 1/10 of switching frequency.

The strategy for choosing R_C and C_C is to set the crossover frequency with R_C and set the compensator zero with C_C. Using selected crossover frequency, f_C, to calculate R_C:

$$R_C = f_C \times \frac{V_0}{V_{FB}} \times \frac{2\pi \times C_0}{G_{EA} \times G_{CS}}$$

Where f_C is desired crossover frequency;
V_{FB} is 0.8 V; G_{EA} is the error amplifier transconductance,which is $200 \cdot 10^{-6}$ A/V;
G_{CS} is the current sense circuit transconductance, which is 4.5 A/V.

The compensation capacitor C_C and resistor R_C together make a zero. This zero is put somewhere close to the dominate pole f_{p1} but lower than 1/5 of selected crossover frequency. C_C can is selected by:

$$C_C = \frac{1.5}{2\pi \times R_C \times f_{P1}}$$

Equation above can also be simplified to:

$$C_C = \frac{C_0 \times R_L}{R_C}$$

Thermal Management

The AOZ29303QI power module thermal performance depends on total power dissipation of module and PCB design. It's critical to keep the power module temperature within desirable value. The good PCB design can improve the power module thermal performance. The details can be found in layout section. AOZ29303QI can operate 3A up to $T_A = 85°C$ without thermal derating.

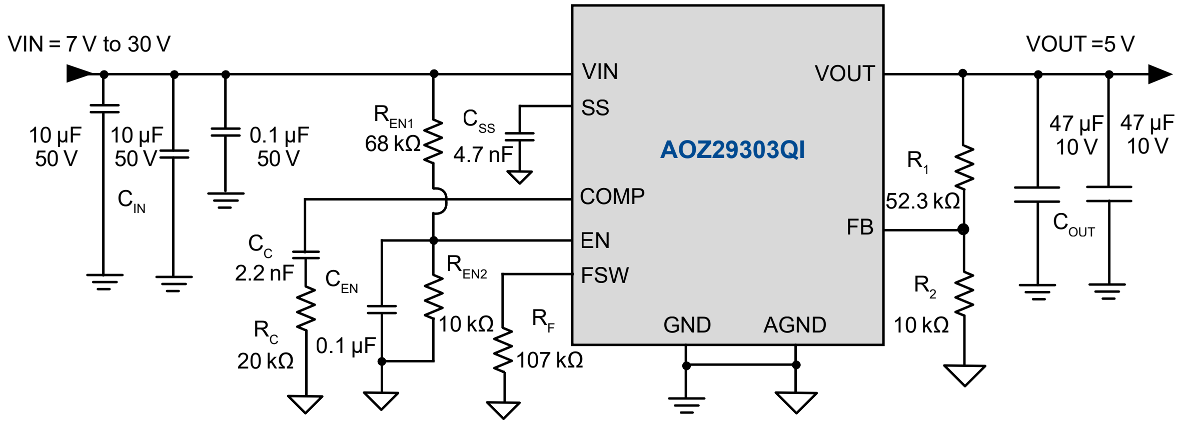


Figure 15. Typical Application Circuit for 5 V Output with Recommended Passive Components

Table 1. External Component Selection

VIN (V)	VOUT (V)	R_1 (kΩ)	R_2 (kΩ)	C_{IN} (µF)	C_{OUT} (µF)	C_C (nF)	R_C (kΩ)	C_{SS} (nF)
4.5-25	1	2.5	10	2 x 10	4x47	2.2	20	4.7
4.5-20	1.2	4.99	10	2 x 10	2x47	2.2	20	4.7
4.5-25	1.5	10	11.5	2 x 10	2x47	2.2	20	4.7
4.5-30	1.8	12.7	10.2	2 x 10	2x47	2.2	20	4.7
4.5-30	2	15	10	2 x 10	2x47	2.2	20	4.7
4.5-30	2.5	21.5	10	2 x 10	2x47	2.2	20	4.7
4.5-30	3.3	31.6	10	2 x 10	2x47	2.2	20	4.7
7-30	5	52.3	10	2 x 10	2x47	2.2	20	4.7

Note:

+/-1% resistor is recommended for Rf.

Table 2. Recommended Frequency Range for Setting

Vin_max (V)	Vout (V)	Freq Setting Min (kHz)	Freq Setting Max (kHz)	R_F Recommendation for Freq_Setting (kΩ)
30	5	400	450	107
30	3.3	300	450	124
30	2.5	300	400	137
24	5	400	450	124
24	3.3	300	450	124
24	2.5	300	450	124
24	1.2	200	250	196
12	5	400	800	953
12	3.3	300	800	953
12	2.5	300	500	124
12	1	200	400	162

Note:

+/-1% resistor is recommended for Rf.

PCB Layout

AOZ29303QI power module integrates the inductor and passive components into the package to minimize the parasitic inductance. The switching noise issue is much alleviated. But the board layout is still extremely important to power module performance. The following layout guidelines are given for optimal electrical and thermal performance.

1. Use large copper area for power traces (VIN, PGND, VOUT) to minimize the conduction loss and maximize the thermal performance.
2. Place input capacitors C_{IN} as close as possible to VIN pins and PGND pins.
3. Place output capacitors C_{OUT} as close as possible to VOUT pins and PGND pins.
4. Place R_F, C_{SS}, C_C, and R_C as close as possible to their respective pins.
5. Place R_1 & R_2 as close as possible to FB pin.
6. Connect all power components return to PGND.
7. Connect all control components return to AGND.
8. Use single point connection for AGND and PGND.
9. Make large solid ground plane with minimum interruption.
10. Make components connection to the ground as short as possible.
11. Use multiple VIAs for power traces (VIN, PGND, VOUT) connection to reduce the conduction loss and enhance the thermal performance.

A top layer of example board is used to demonstrate the recommended board layout in Figure 16. It shows the input capacitors, output capacitors, power module, ground and thermal VIAs. It is important to separate AGND and PGND to minimize the noise interference issue. A bottom layer for external control components, PGND and AGND are shown in Figure 17.

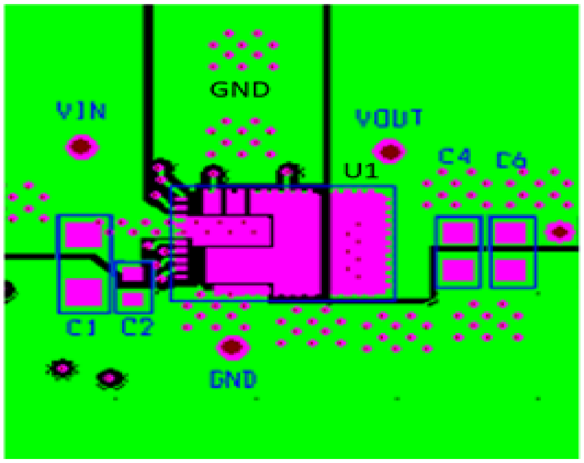


Figure 16. Top PCB Layer of AOS Evaluation Board

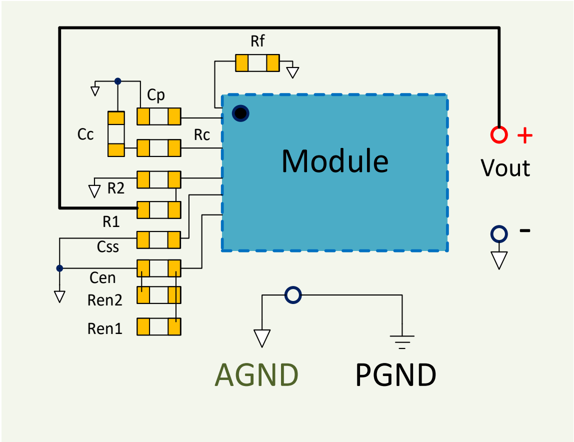
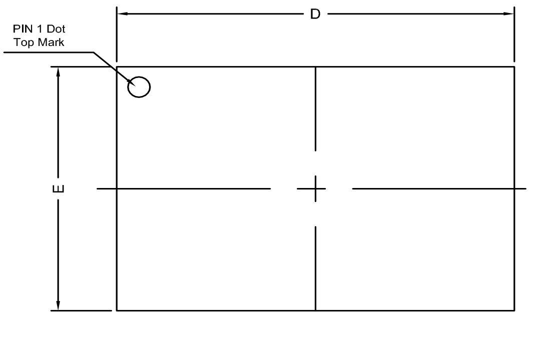
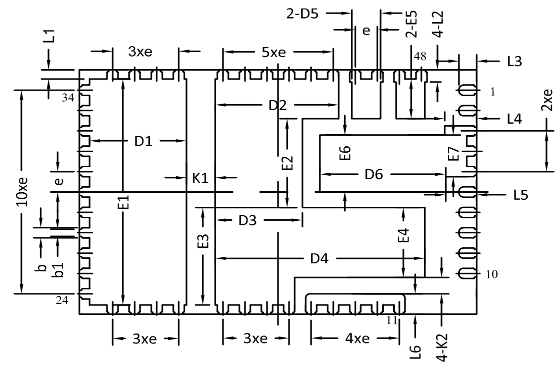


Figure 17. Bottom Layer of AOS Evaluation Board

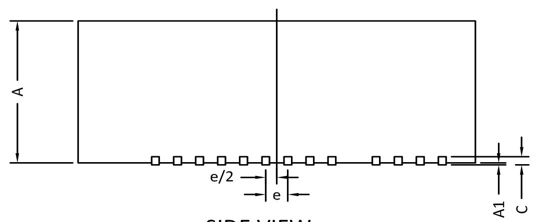
Package Dimensions, QFN9x6-48L



TOP VIEW

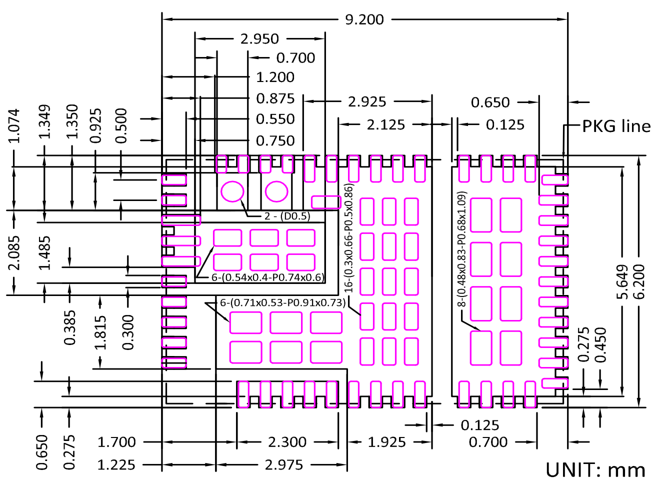


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN & SOLDER PASTE EXAMPLE



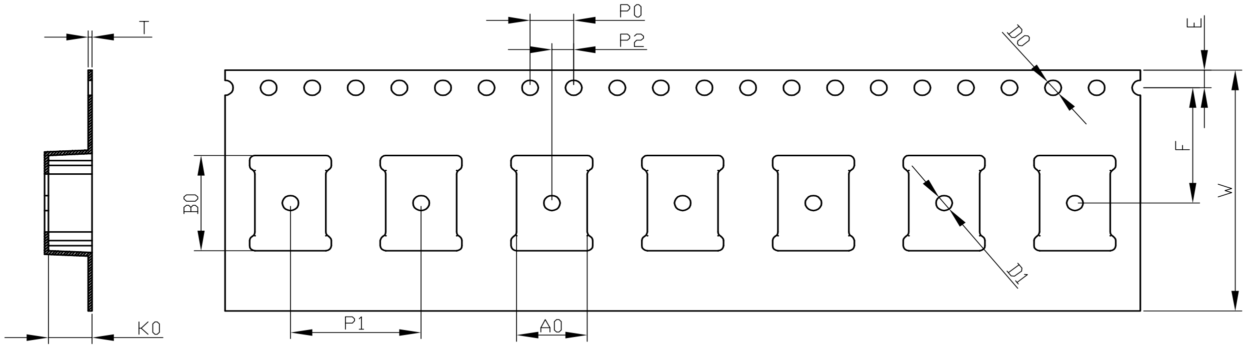
SOLDER PASTE EXAMPLE (Pattern with Pink Color)
Based on 0.1mm Thick Stencil
50% printed solder coverage by area

SYMBOLS	DIM. IN MILLIMETERS			DIM. IN MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.600	3.700	3.800	0.142	0.146	0.150
A1	0.000	---	0.050	0.000	----	0.002
b	0.200	0.250	0.300	0.008	0.010	0.012
b1	0.175REF			0.007REF		
c	0.20REF			0.008REF		
D	8.900	9.000	9.100	0.350	0.354	0.358
D1	2.100	2.200	2.300	0.083	0.087	0.091
D2	2.700	2.800	2.900	0.106	0.110	0.114
D3	1.875	1.975	2.075	0.074	0.078	0.082
D4	4.650	4.750	4.850	0.183	0.187	0.191
D5	0.550	0.650	0.750	0.022	0.026	0.030
D6	2.725	2.825	2.925	0.107	0.111	0.115
E	5.900	6.000	6.100	0.232	0.236	0.240
E1	5.450	5.550	5.650	0.215	0.219	0.222
E2	2.085	2.185	2.285	0.082	0.086	0.090
E3	2.290	2.390	2.490	0.090	0.094	0.098
E4	1.615	1.715	1.815	0.064	0.068	0.071
E5	0.875	0.975	1.075	0.034	0.038	0.042
E6	1.285	1.385	1.485	0.051	0.055	0.058
E7	0.925	1.025	1.125	0.036	0.040	0.044
L1	0.125	0.225	0.325	0.005	0.009	0.013
L2	0.200	0.300	0.400	0.008	0.012	0.016
L3	0.300	0.400	0.500	0.012	0.016	0.020
L4	0.625	0.725	0.825	0.025	0.029	0.032
L5	0.600	0.700	0.800	0.024	0.028	0.031
L6	0.400	0.500	0.550	0.016	0.020	0.022
K1	0.550	0.650	0.700	0.022	0.026	0.028
K2	0.300	0.400	0.450	0.012	0.016	0.018
e	0.50REF			0.020REF		

NOTES:
CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN9x6-48L

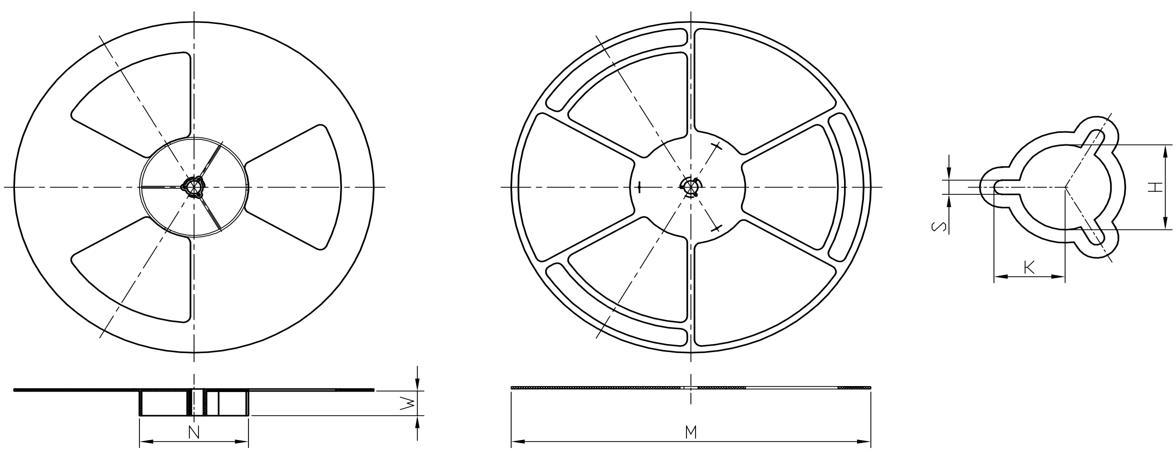
QFN9x6_48L_EP3_S Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	W	E	F	P0	P1	P2	T
QFN9x6	6.50 ±0.10	9.50 ±0.10	4.00 ±0.10	1.50 +0.10 -0.00	1.50 +0.20 -0.00	24.00 +0.30 -0.10	1.75 ±0.10	11.50 ±0.10	4.00 ±0.10	12.00 ±0.10	2.00 ±0.10	0.40 ±0.04

QFN9x6_48L_EP3_S Reel



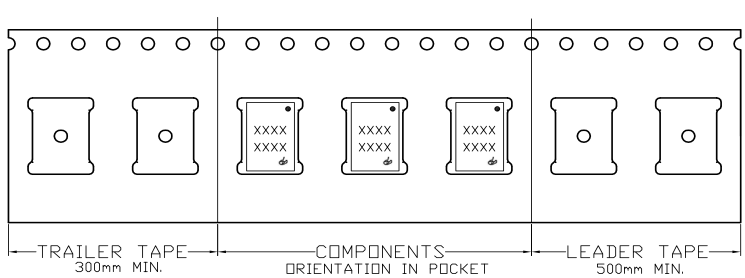
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	H	K	S
24 mm	ø330	ø330.00 +0.25 -4.00	ø100.00 ±0.2	24.4 +2.0 -0.0	ø13.00 +0.50 -0.20	10.5 ±0.25	2.2 ±0.25

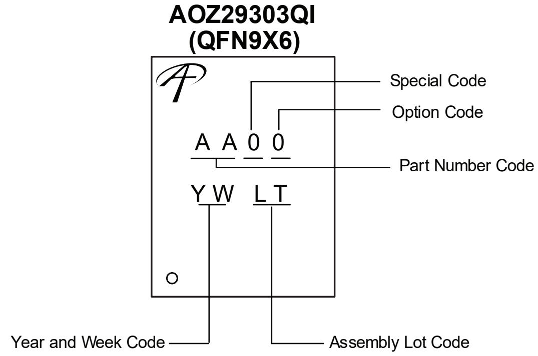
QFN9x6_48L_EP3_S Tape

Leader / Trailer
& Orientation

Unit Per Reel:
1000pcs



Part Marking



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.