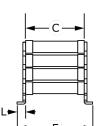
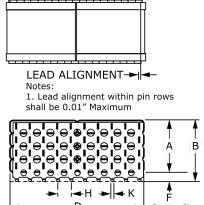




KPS-MCC Indust COG HT200C, Ceramic, 1 uF, 10%, 630 VDC, COG





← C→	Notes: 1. Lead alignment within pin rows shall be 0.01" Maximum
- - - - - - - - - - - - - - - - - - - - - - - - -	A B

Click here for the 3D model.

Dimensions	,
D	25.64mm +/-0.635mm
L	1.4mm +/-0.127mm
Н	2.54mm NOM
F	1.778mm +/-0.25mm
Α	10.67mm MAX
В	12.702mm MAX
С	11.43mm +/-0.635mm
E	13.7mm +/-0.89mm
K	0.5mm NOM

Packaging Specifications	
Packaging	Waffle, Box
Packaging Quantity	16

General Information		
Series	KPS-MCC Indust COG HT200C	
Style	Leaded Stacked Chip	
Description	Low ESR, Stacked Ceramic Chips	
Features	200C, Low ESR, High Thermal Stability, Bulk Capacitance	
RoHS	With Exemptions	
REACH	SVHC (Pb - CAS 7439-92-1)	
SCIP Number	297427bb-2a48-4853-b594-641304a2cc24	
Termination	Silver	
Lead	L Leads	
AEC-Q200	No	
Notes	Number of chips in this stack: 8.	

Specifications		
Capacitance	1uF	
Capacitance Tolerance	10%	
Voltage DC	630 VDC	
Dielectric Withstanding Voltage	819 VDC	
Temperature Range	-55/+200°C	
Temperature Coefficient	COG	
Dissipation Factor	0.1% 1 kHz 25C	
Aging Rate	0% Loss/Decade Hour	
Insulation Resistance	1GOhms	

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