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LNA_024_005

Low Noise Amplifier 24 – 29 GHz

Preliminary Data Sheet

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Version Control

Version	Changed section	Description of change	Reason for change
0.1	All	Document creation	
0.2	4.1 Absolute Max Ratings	ESD robustness values defined	ESD test passed
1.0	Raised to final version Figure 14 added	 Reference planes for S-parameter measurement	According to QMS release procedure Clarification

Table of Contents

1 Features 4
1.1 Overview 4
1.2 Applications 4
2 Block Diagram 5
3 Pin Configuration 5
3.1 Pin Assignment 5
3.2 Pin Description 6
4 Specification 6
4.1 Absolute Maximum Ratings 6
4.2 Operating Range 7
4.3 Thermal Resistance 7
4.4 Electrical Characteristics 7
5 Packaging 8
5.1 Outline Dimensions 8
5.2 Package Footprint 8
5.3 Package Code 9
5.4 Qualification Test 9
6 Application 9
6.1 Application Circuit Schematic 9
6.2 Evaluation Board 10
6.3 Input / Output Stages 10
7 Measurement Results 11

1 Features

- Low-noise amplifier (LNA) for 24-GHz ISM band an beyond
- Single supply voltage of 3.3 V
- Low power consumption of 18 mW
- Fully ESD protected device
- Gain control input
- Power-down mode
- Fast on / off switching for pulsed operation
- QFN16 leadless plastic package 3 mm × 3 mm
- Pb-free, RoHS compliant package
- IC is available as bare die as well

1.1 Overview

The low-noise amplifier LNA_024_005 is a two stage amplifier operating in two gain modes (high gain and low gain) with a power-down feature. The first stage employs a cascode configuration with inductive load and inductive emitter degeneration for stability reasons. The input matching network of the LNA consists of shunt inductor and series capacitor. The input shunt inductor provides ESD protection. In order to provide compact design and galvanic isolation between amplifier stages, transformers were used for interstage coupling and output matching. The second stage is a common-base structure with two gain states. This stage is loaded with a transformer providing appropriate output impedance. The gain mode is defined by an external digital signal at the Vctrl input. The LNA can be powered down via the PWR pin.
The LNA_024_005 features improved ESD robustness and replaces its predecessor LNA_024_004.

1.2 Applications

The main use of the LNA is in wireless communication systems and in radar systems for the ISM band at 24 GHz and for ultra-wide band systems up to 29 GHz.

2 Block Diagram

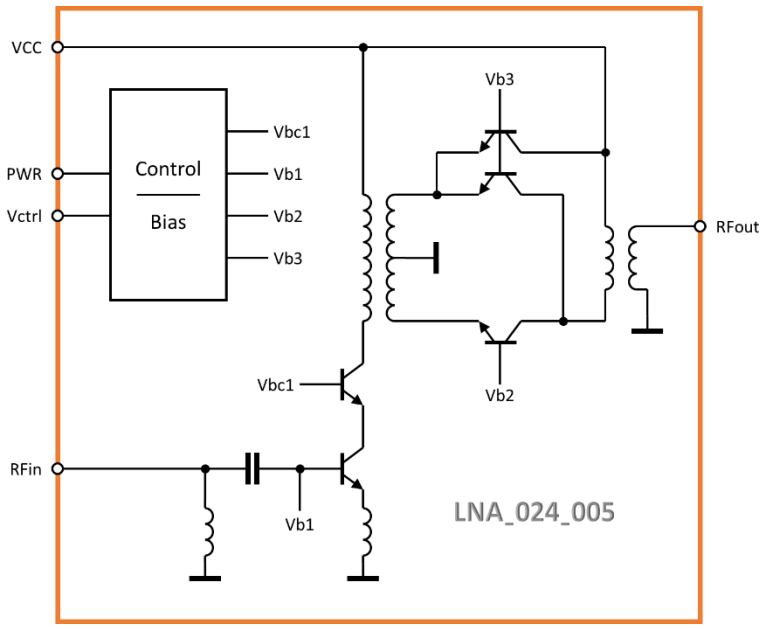


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

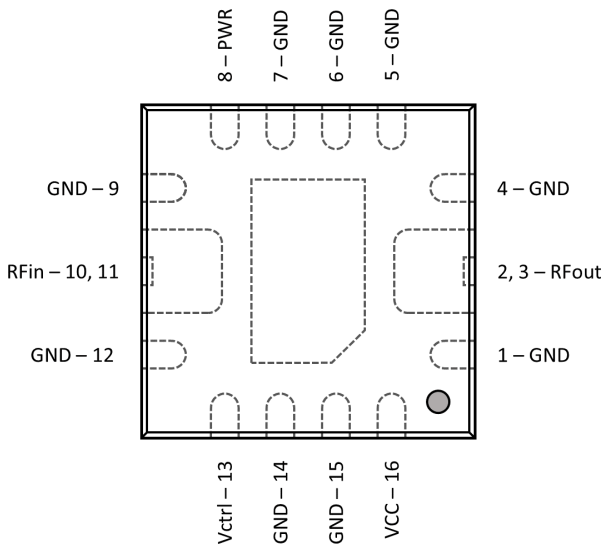


Figure 2 Pin Assignment (QFN16, 3 mm × 3 mm, Top View)

3.2 Pin Description

Table 1 Pin Description

Pin		Description
No.	Name	
1	GND	Ground
2	RFout	RF output, 50 Ω. Pin 2 and 3 have to be shorted on board close to the QFN package. (See recommended land pattern in Figure 4.)
3	RFout	
4	GND	Ground
5	GND	
6	GND	
7	GND	
8	PWR	Power-down input: high – power-down, low – operate. PMOS input with pull-down resistor as shown in Figure 9, Equivalent I/O Circuits.
9	GND	Ground
10	RFin	RF input, 50 Ω. Pin 10 and 11 have to be shorted on board close to the QFN package. (See recommended land pattern in Figure 4.)
11	RFin	
12	GND	Ground
13	Vctrl	LNA gain control input: high – high gain, low – low gain. CMOS logic input with pull-down resistor as shown in Figure 9, Equivalent I/O Circuits.
14	GND	Ground
15	GND	
16	VCC	Supply voltage, 3.3 V
(17)	GND	Exposed die attach pad of the QFN package, must be soldered to ground.

4 Specification

4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition / Remark
Supply voltage	V_{CC}		3.6	V	to GND
DC voltage at RF pins	V_{DCRF}	0	2	mV	IC provides low ohmic circuit to GND for pin RFout and RFin
Junction temperature	T_J		150	°C	
Storage temperature range	T_{STG}	-65	150	°C	
DC voltage at control inputs	V_{CTL}	-0.3	V_{CC} + 0.3	V	Pins Vctrl and PWR
Input power into pin RFin	P_{IN}		0	dBm	
ESD robustness, HBM	V_{ESD1}		2000	V	Note 1
ESD robustness, CDM	V_{ESD2}		500	V	Note 2

Note 1 According to JEDEC JESD22-A114C Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component (HBM), Component Level

Note 2 According to JEDEC JS-002-2018 Joint Standard for Electrostatic Discharge Sensitivity Testing, Charged Device Model (CDM) - Device Level

4.2 Operating Range

Table 3 Operating Range

Parameter	Symbol	Min	Max	Unit	Condition / Remark
Ambient temperature	T_A	-40	85	°C	
Supply voltage	V_{CC}	3.13	3.47	V	(3.3 V ± 5%)
DC voltage at control inputs	V_{CTL}	0	V_{CC}	V	Pins Vctrl and PWR

Note: Do not drive input signals without power supplied to the device.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit	Condition / Remark
Thermal resistance, junction-to-ambient	R_{thja}			77	K/W	JEDEC Standard JESD51-5

4.4 Electrical Characteristics

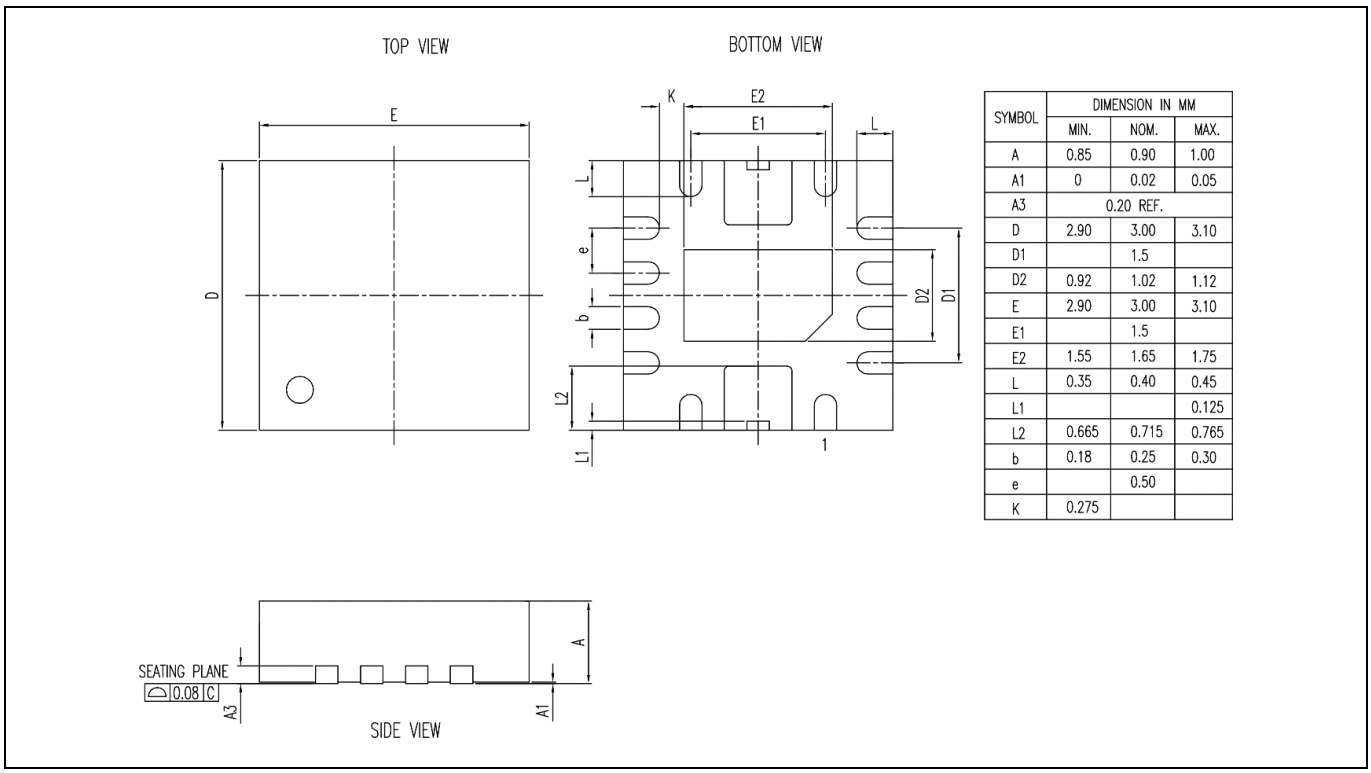
T_A = -40 °C to +85 °C unless otherwise noted. Typical values measured at T_A = 25 °C and V_{CC} = 3.3 V.

Table 5 Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition / Remark
DC Parameters						
Supply current consumption	I_{CC}	5	5.6	6.5	mA	V(Vctrl) = V(PWR) = 0
Vctrl input voltage, low level	V_{Ctrl_L}	0		$0.3 \times V_{CC}$	V	CMOS logic input stage
Vctrl input voltage, high level	V_{Ctrl_H}	$0.7 \times V_{CC}$		V_{CC}	V	
PWR input voltage, low level	V_{PWR_L}	0		$0.2 \times V_{CC}$	V	PMOS input stage
PWR input voltage, high level	V_{PWR_H}	V_{CC} - 0.3		V_{CC}	V	
Logic input current, low level	I_{IN_L}	-1		1	µA	V(Vctrl) = V(PWR) = 0
Logic input current, high level	I_{IN_H}	30	64	150	µA	V(Vctrl) = V(PWR) = 3.3 V
RF Parameters						
Frequency range	f_{3dB}	21.5		28.7	GHz	
Output impedance	Z_{TXout}		50		Ω	
Number of LNA gain settings	N_G		2			controlled by input Vctrl
LNA gain, high gain	$S_{21}H$	13.5	15	17	dB	at 24.15 GHz, V(Vctrl) = 3.3 V
LNA gain, low gain	$S_{21}L$	6.5	8	10	dB	at 24.15 GHz, V(Vctrl) = 0
Noise figure, high gain	NF_H		3.2		dB	V(Vctrl) = 3.3 V, simulated
Noise figure, low gain	NF_L		5		dB	V(Vctrl) = 0, simulated
Input return loss	$\lvert S_{11} \rvert$	0.3	0.4	0.5		at 24.15 GHz
	$Ph(S_{11})$	157	177	197	deg	
Output return loss	$\lvert S_{22} \rvert$	0.4	0.5	0.6		
	$Ph(S_{22})$	-155	-140	-125	deg	
Input Compression Point	CP_I	-10		-6.5	dBm	

5 Packaging

5.1 Outline Dimensions



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.85	0.90	1.00
A1	0	0.02	0.05
A3		0.20 REF.	
D	2.90	3.00	3.10
D1		1.5	
D2	0.92	1.02	1.12
E	2.90	3.00	3.10
E1		1.5	
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
L1			0.125
L2	0.665	0.715	0.765
b	0.18	0.25	0.30
e		0.50	
K	0.275		

Figure 3 Outline Dimensions of QFN16, 3 mm × 3 mm, Pitch 0.5 mm

5.2 Package Footprint

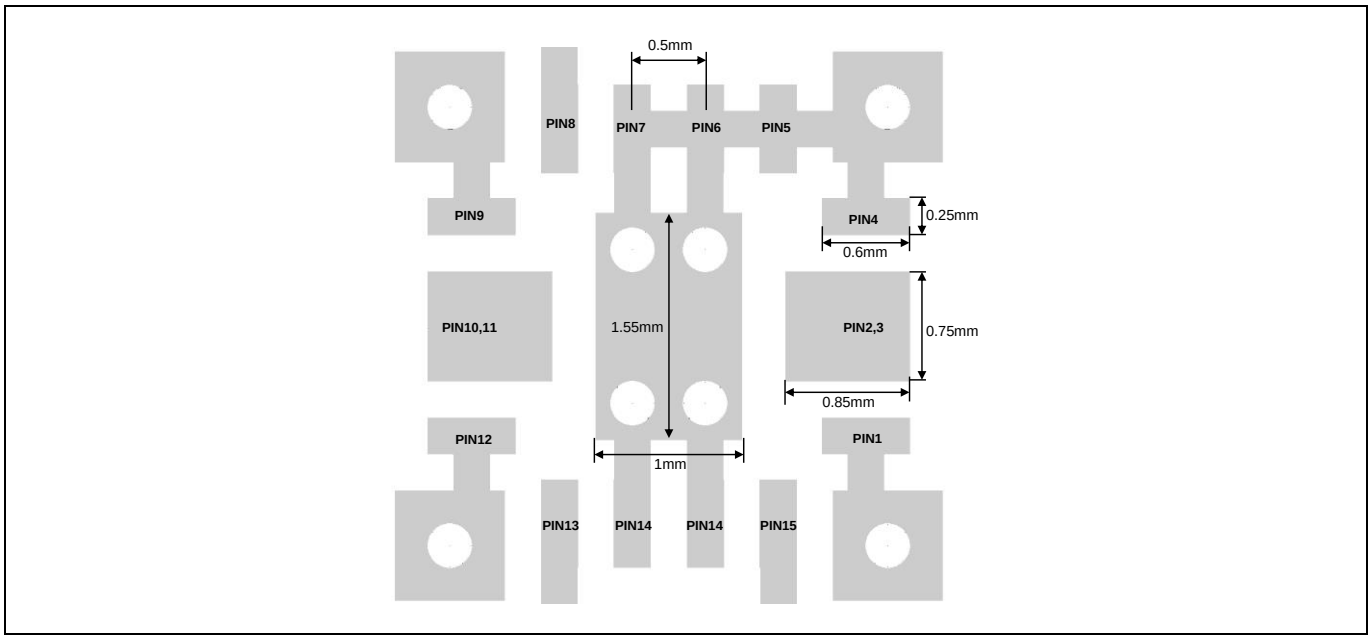


Figure 4 Recommended Land Pattern

5.3 Package Code

Top-Side Marking LNA005
YYWW

5.4 Qualification Test

Table 6 Reliability and Environmental Test

Qualification Test	JEDEC Standard	Condition	Pass / Fail
MSL3	J-STD-020E	Reflow simulation 3 times at 260 °C	pass

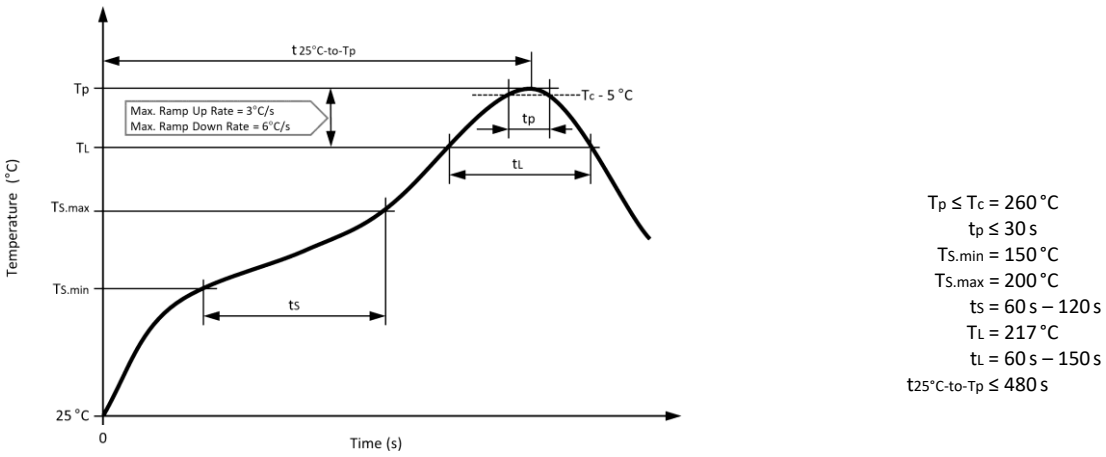


Figure 5 Reflow Profile for Pb-Free Assembly according to JEDEC Standard J-STD-020E

6 Application

6.1 Application Circuit Schematic

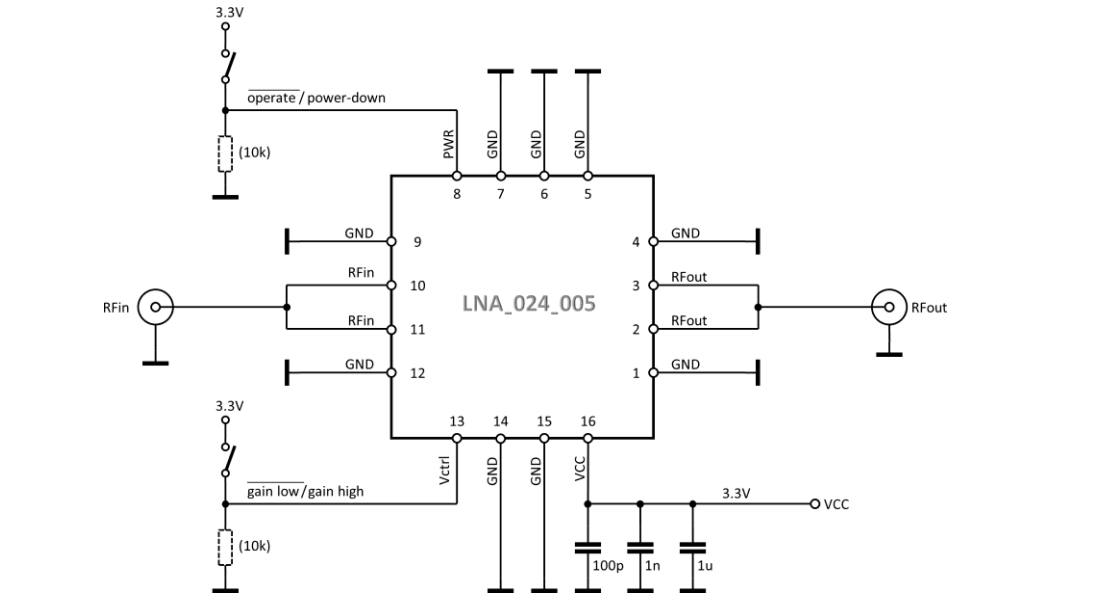


Figure 6 Application Circuit

6.2 Evaluation Board

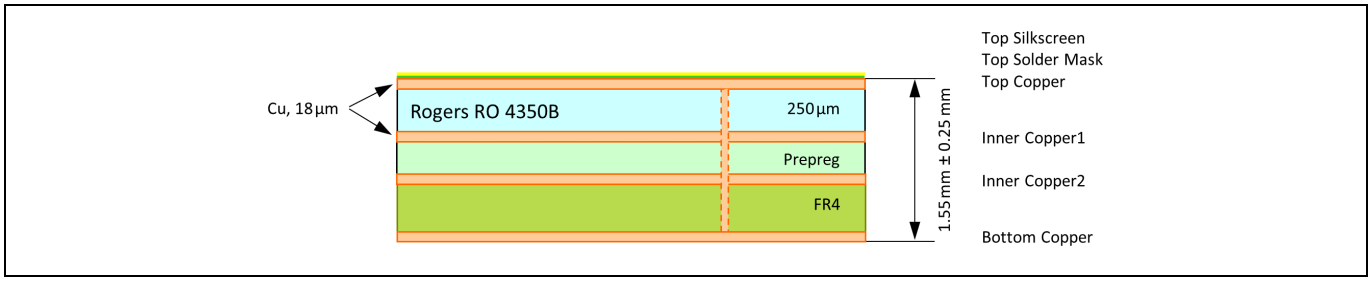


Figure 7 Evaluation Board Stack-up

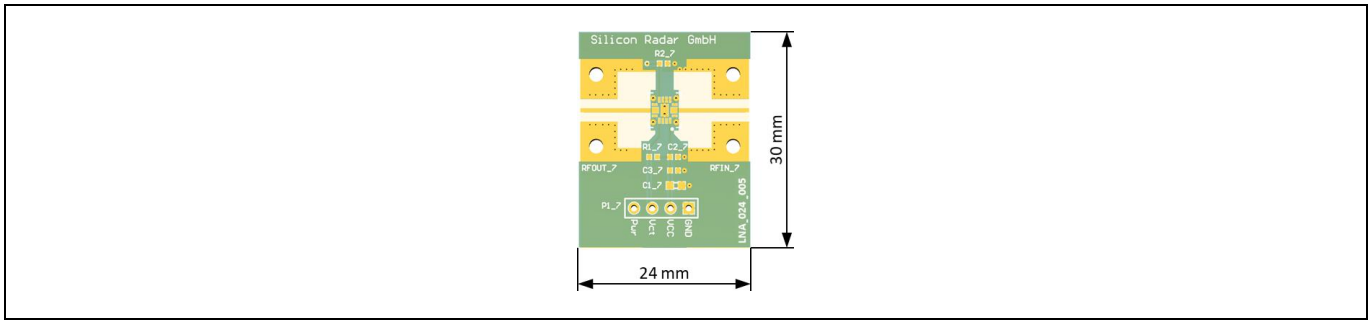


Figure 8 Evaluation Board Layout (Top View)

6.3 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins should never exceed V_{CC} by more than 0.3 V. Otherwise, the supply current may be sourced through the upper ESD protection diode connected at the pin.

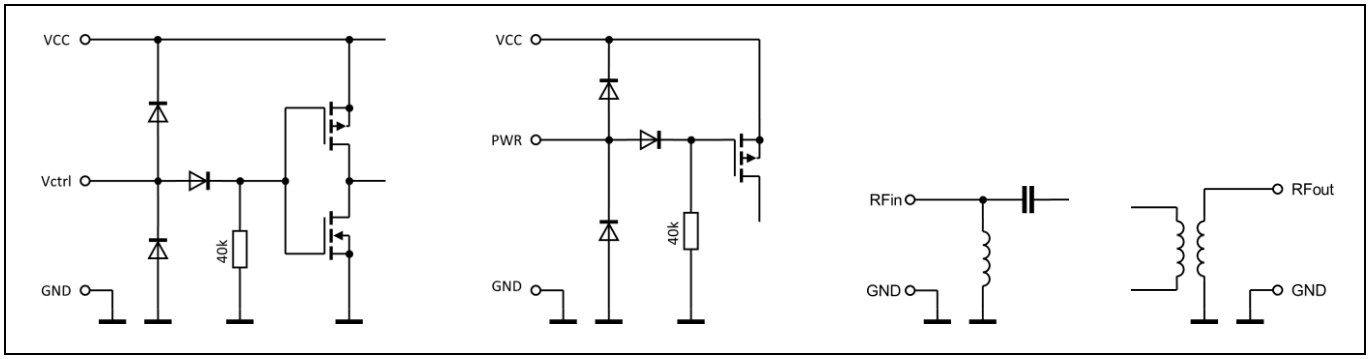


Figure 9 Equivalent I/O Circuits

7 Measurement Results

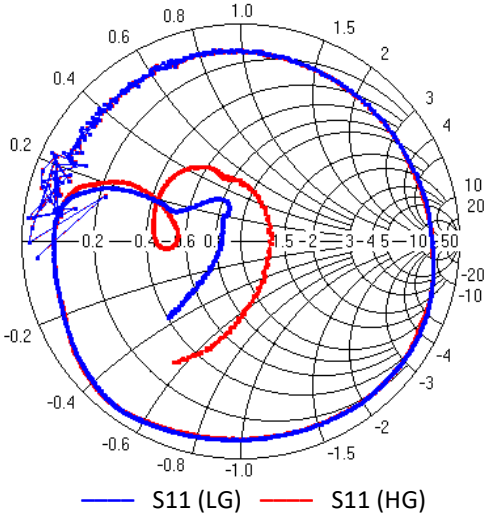


Figure 10 Input Reflection Coefficient, low and high gain

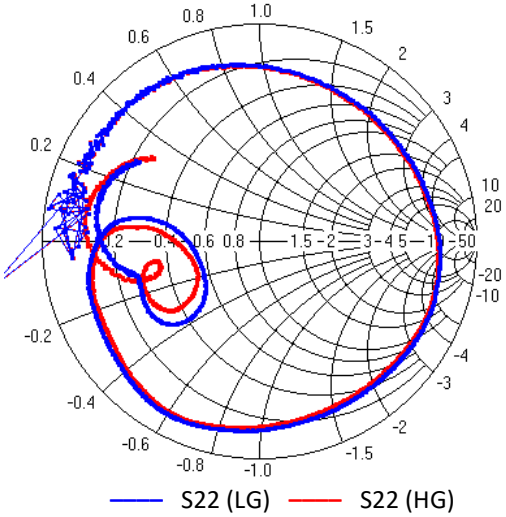


Figure 11 Output Reflection Coefficient, low and high gain

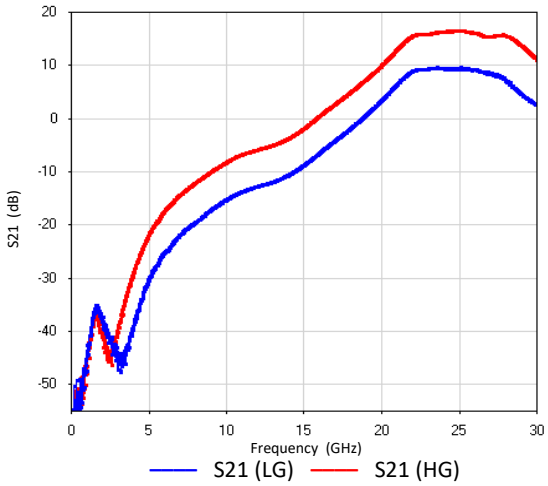


Figure 12 S21, low and high (with -30 dBm input power)

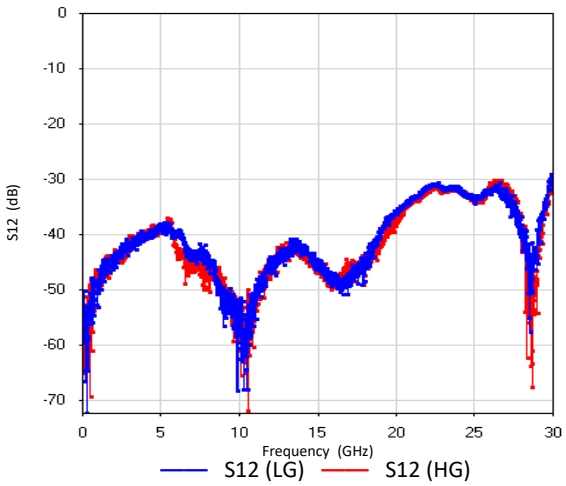


Figure 13 S12, low and high gain

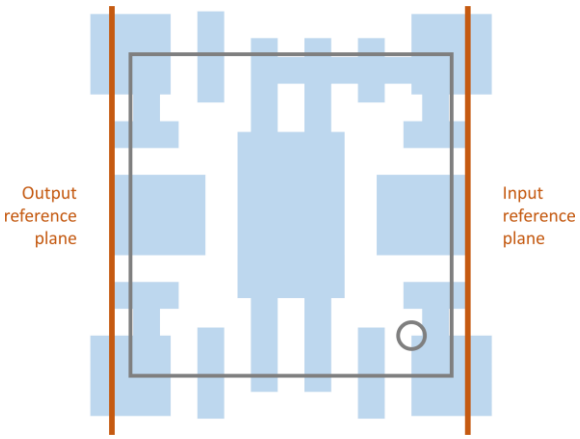


Figure 14 Reference planes for S-parameter measurement

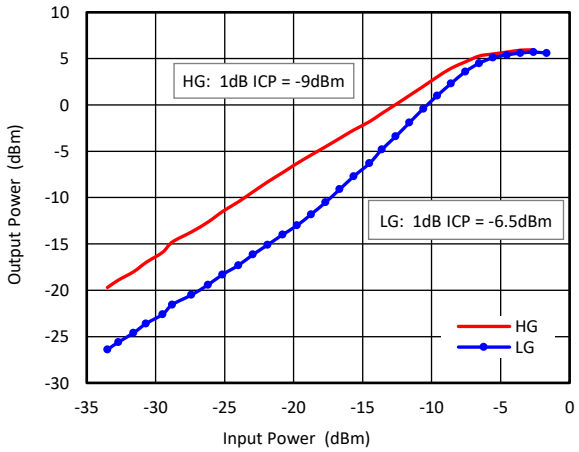


Figure 15 Linearity, low and high gain

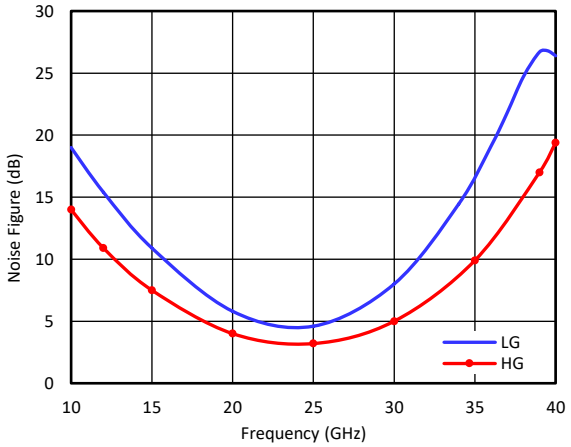


Figure 16 Simulated Noise Figure, low and high gain

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