AIF12W300, 600W, DC-DC Converter Module

The single output AIF is an isolated, single output DC to DC converter module, providing up to 600W output with a maximum baseplate operating temperature of 100°C with no derating. The AIF features full safety isolated low voltage secondary side control and Astec Linear Programming (ALP™) or through I^2C bus for convenient adjustment of the module's parameters.

Special Features

- **600W continuous power at 100°C baseplate temperature**
- **108W/in^3 (6.6W/cm^3)**
- **High efficiency – 91.8% typical**
- **Low output ripple and noise**
- **Positive and Negative Enable function**
- **Excellent transient response**
- **OVP, OCP, V Adj control with ALP^{TM} analog mode linear control, or through I^2C bus for digital mode control.**
- **Paralleable with accurate current sharing**
- **Switching Frequency 400KHz**

Environmental Specifications

-20°C to 100°C Operating Baseplate Temperature
-55°C to 125°C Storage Temperature
MTBF > 0.3Mhours
Pb-free reflow compatible and ROHS Compliant

Electrical Parameters

Input

Input range	**250 - 420 VDC**
Input Surge	**500V / 100ms**
Efficiency	**91.8% (Typical)**

Output

Regulation	**0.2% typical down to no load**
Noise / Ripple	**480mV typical**

Control

Voltage Adjust	**80 to 120%**
Enable	**TTL compatible (positive & negative enable options)**
Current Limit Adjust	**20% to 100%**
Over Voltage Protection Adjust	**110% to 150% V_O**

Safety

UL, cUL	**60950 Recognized**
TUV	**EN60950 Licensed**

Electrical Specifications

STANDARD TEST CONDITION on a single unit, unless otherwise indicated, electrical specifications apply over all operating input voltage and temperature conditions.

T_{amb}	25°C
V_{in}	300 V± 2%
Enable	Open
CLK IN	Open
CLK OUT	Open
CSHARE	Open
I_{out}	75% $I_{o\ max}$ ± 2%
AUX OUTPUT	Open
-Sense	connect to –Vout
V ADJ	Open
C MON	Open
TEMP MON	Open
C LIM ADJ	Open
OVP ADJ	Open
PG/ID	Open
I/P Cap requirement	68µF/450V min.

ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the IPS. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage: Continuous: Transient (100ms)	 V_I $V_{I,\ trans}$	 250 	 - -	 420 500	 V_{dc} V_{dc}
Operating Baseplate Temperature	Tc	-20	-	100	°C
Start up Baseplate Temperature	-	-40	-	100	°C
Storage Temperature	T_{STG}	-55	-	125	°C
Operating Humidity	-	15	-	95	%
I/O Isolation	-	2700	-	-	V_{dc}

INPUT SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	V_I	250	300	420	V_{dc}
Undervoltage Threshold (I_O = 10% $I_{O\ max}$) Turn-on point Turn-off point	 - -	 205 175	 - -	 245 215	 V V
Input Current [1] ($V_I = V_{I\ min}$, $I_O = I_{O\ max}$, $V_O = V_{O\ nom}$) (V_I = 0 to $V_{I\ max}$, $I_O = I_{O\ max}$, $V_O = V_{O\ nom}$)	 $I_{I\ max}$ $I_{I\ max}$	 - -	 - -	 2.8 3.4	 A A
Input Reflected Ripple Current [2] (5Hz to 20MHz: 12µH source impedance: T_{amb} = 25°C)	I_I	-	30	-	mA_{pk-pk}
Inrush Transient [3]	I^2t	-	-	2.8	A^2s
Break Regulation	-	-	215	245	V
CLK IN Frequency Voltage Level (internal ac coupled)	 - -	 720 3.3	 800 -	 880 5.5	 kHz V_{pk-pk}
Enable Positive Logic Low Logic - Module Off High Logic - Module On (Enable pin opened) Enable Low Sourced Current (V_{enable} = 0.7V) Turn-On Delay	 V_{enable} V_{enable} - -	 0 2 - -	 - - - -	 0.7 10 150 380	 V V µA mS
No load input power	-	-	-	5	W
Turn-On Time ($I_O = I_{O\ max}$; V_O within 1%) (No external O/P capacitance)	-	-	-	650	mS
Input Capacitance	-	-	0.6	0.8	µF

OUTPUT SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltage Setpoint ($V_{I\ min}$ to $V_{I\ max}$: $I_O = I_{O\ max}$; $T_{amb} = 25°C$)	$V_{O\ set}$	47.52	48	48.48	V
Output Regulation: Line Load	- -	- -	- -	0.2 0.2	% %
Output Voltage Adjust [4, 5] $V_{adj} = 0V$ $V_{adj} = 2V$	- -	78 118	80 120	82 122	$\%V_O$ $\%V_O$
Output Ripple and Noise Peak-to-Peak (5 Hz to 20MHz)	-	-	110	480	mV_{pk-pk}
External Load Capacitance	-	-	-	2000	µF
Switching Frequency	-	360	400	440	kHz
Output Power	P_O	-	-	600	W
Efficiency ($V_I = V_{I\ nom}$, $I_O = I_{O\ max}$, $T_{amb} = 25°C$)	-	90	91.8	-	%
Output Current	I_O	0	-	12.5	A
Output Current-limit Inception (Hiccup) (V_O = 97% $V_{O\ set\ nom}$)	I_O	105	-	120	$\%I_{O\ max}$
Output Current Limit Adjust [5]	-	20	-	100	$\%I_{O\ max}$
Output Current Monitor I_{mon} at $I_{O\ max}$ Monitored I_O Range I_{mon} Compliance Voltage	- - -	0.9 20 -	1.0 - -	1.1 100 5.0	mA $\%I_{O\ max}$ V
Current Share Accuracy [6] (Cshare connected together, $I_O \geq 80\%I_O$ max) No. of Parallel Unit	- -	- -	± 3 -	± 5 10	$\%I_{avg}$ pcs
Over Current Protection Level (V_O dropped to 97% of $V_{O\ nom}$)	-	105	110	115	$\%I_{O\ max}$
Over Voltage Protection Level	-	120	125	130	$\%V_O$
Over Voltage Protection Adjust [5]	-	120	-	150	$\%V_O$
Over Temperature Protection Trip Point (Baseplate temperature)	-	105	-	120	°C
Internal Temperature Monitor Temperature Coefficient Source Impedance	- -	9.8 -	10.0 1.0	10.2 -	mV/°C kΩ
Temperature Coefficient (T_C = -40°C to 100°C)	-	-	-	0.02	$\%V_O/°C$

OUTPUT SPECIFICATIONS *(continued)*

Parameter	Symbol	Min	Typ	Max	Unit
Step-load Excursion (25% to 75% load change @ 1A/µS, recovery to 1%V_O; V_I = $V_{I\ nom}$; T_{amb} = 25°C) Output Overshoot Output Undershoot Step Load Response (25% to 75% load change @ 1A/µS, recovery to 1%V_O; V_I = $V_{I\ nom}$; T_{amb} = 25°C; measure from end of transition)	- - -	- - -	- - -	2.4 2.4 250	V V µS
Turn-on Output Voltage Overshoot (I_O = $I_{O\ max}$; T_{amb} = 25°C; no external O/P capacitor)	-	-	3	5	%V_O
Short Circuit Current (Hiccup Mode)	-	-	-	150	%$I_{O\ max}$
CLK OUT Frequency Voltage Level (internal ac coupled) No. of Fan Out Unit	- - -	720 3.3 -	800 - -	880 5.5 2	kHz V_{pk-pk} pcs
Turn-Off Negative Voltage (resistive loading, wire length of 10cm)	-	-	-	-0.7	V
AUX Output Voltage	-	10.5	12	13.5	V
AUX Output Current [7]	-	-	-	10	mA
AUX Output Voltage Ripple and Noise	-	-	-	600	mV
Power Good Monitor / Identification PG/ID Low (Power Fault, I_{sink} ≤ 10mA) PG/ID Internal Pull-up Resistance to V_O	- -	- 46	- 47	0.2 48	V kΩ

Notes:
1. An input line fuse is recommended for use (e.g. Littelfuse type, 10A 250V FB).
2. External input capacitance required. See Figure 1 for the Input Reflected-Ripple Current Test Setup. Measure input reflected-ripple current with a simulated source inductance of 12µH.
3. See Figure 2 for the Inrush Current Test Setup. Measure input inrush current with a simulated source inductance of 12µH and input bulk capacitor of 68µF/450Vmin must always be added.
4. The combination of remote sense and trim do not exceed a total of 0.5V.
5. Refer to Basic Operation and Features section.
6. See Figure 3 for modules in parallel connection.
7. The AUX output pin does not allow for any short circuit and OCP testing.

Electrical Specifications *(continued)*

ISOLATION SPECIFICATIONS

Parameter	Device	Symbol	Min	Typ	Max	Unit
Isolation Capacitance	All	-	-	300	-	PF
Isolation Resistance	All	-	10	-	-	MΩ

SAFETY AGENCY

Parameter	Device	
Safety Approval	All	UL/cUL 60950, 3rd Edition – Recognized EN 60950 through TUV

SHOCK AND VIBRATION

Vibration test

Endurance random vibration (non-operating)
Random vibration shall be applied at the following test condition:

Frequency range	10 – 200Hz; 200 – 2000Hz
PSD	$0.01g^2$/Hz; $0.003g^2$/Hz
Acceleration	2.5g RMS (typical level)
Duration	20 mins per axis

Endurance random vibration (operating)
Random vibration shall be applied at the following test condition with the unit at operating mode at nominal lines and full load condition, with POK monitored:

Frequency range	10 – 500Hz
PSD	$0.002g^2$/Hz flat
Acceleration	1g RMS
Duration	20 mins per axis

Shock test
The non-operating test condition is selected as typical of:

Acceleration	30g
Pulse	Halfsine
Duration	6ms minimum
Directions	all 6 faces, 3 times in each positive and negative directions

Electrical Specifications *(continued)*

Shock test
The operating test condition is selected as typical of:

Acceleration	4g
Pulse	Halfsine
Duration	22ms minimum
Directions	all 6 faces, 3 times in each positive and negative directions

ESD

Contact discharge	6KV
Air discharge	8KV

EMC (CONDUCTED)
FCC Class A and CISPR22 Class A – This is a system test and not a component level test. See Figure 4 for EMI Filter Schematic.

Electrical Specifications *(continued)*

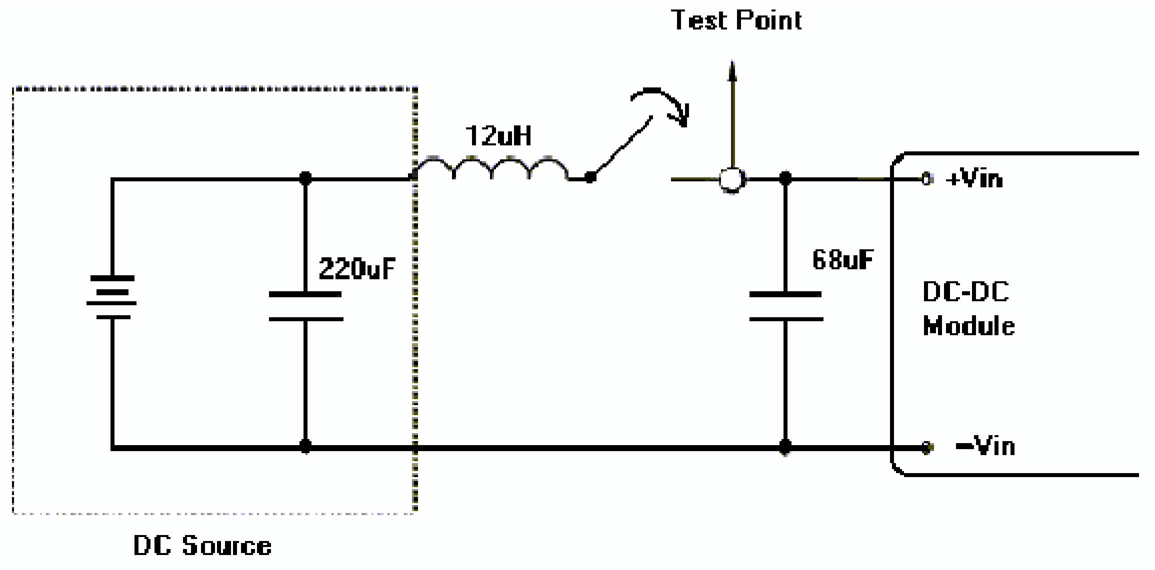


Figure 1. Input Reflected-Ripple Current Test Setup

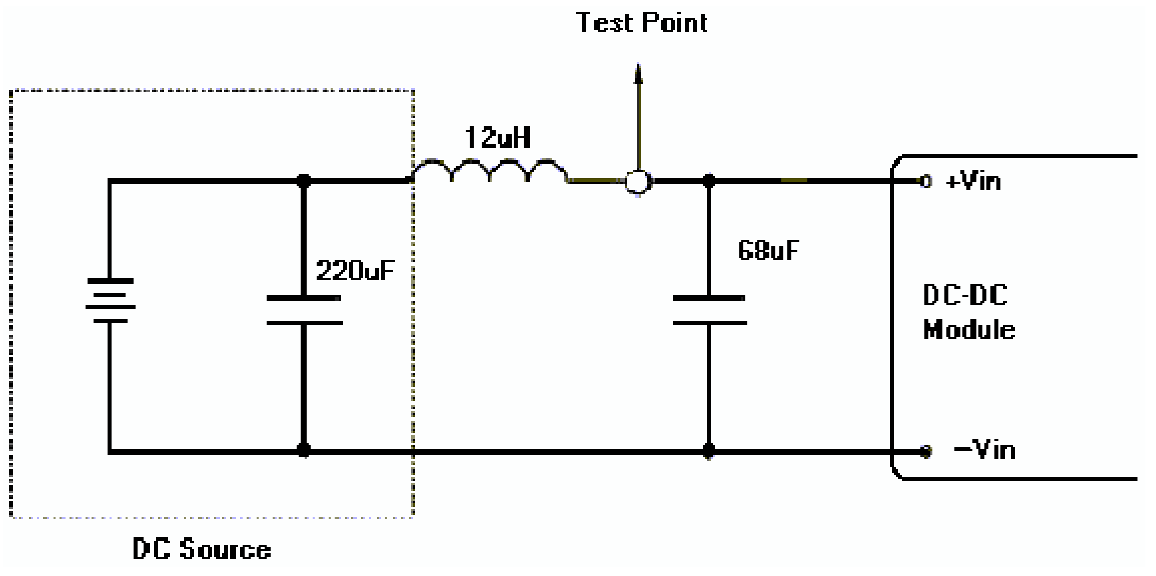
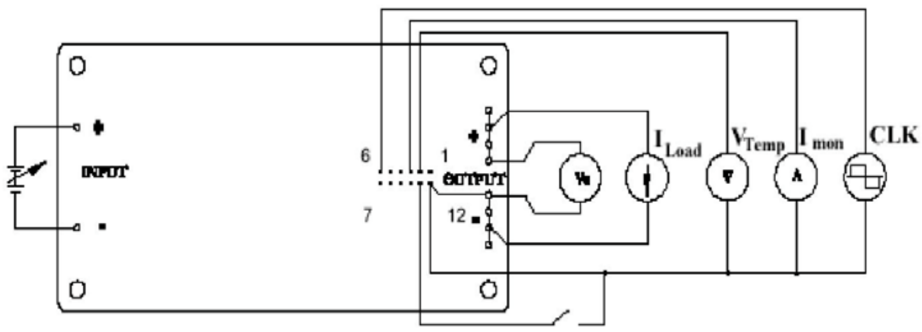
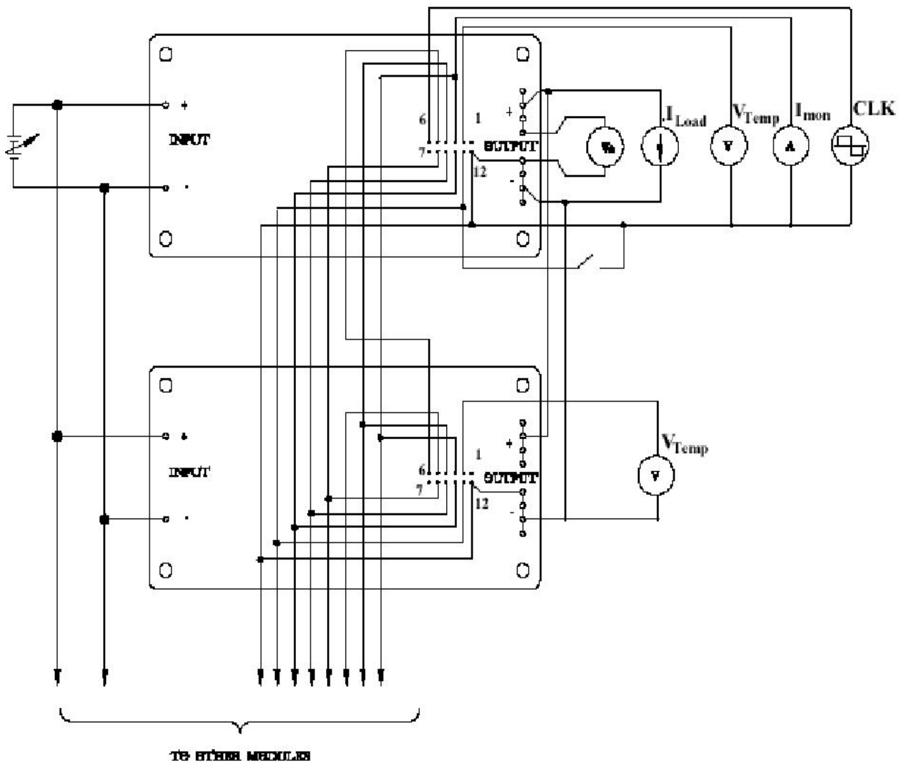


Figure 2. Inrush Current Test Setup

Electrical Specifications *(continued)*



Single Module Operation



Parallel Module Operation

Figure 3. Module Connections for Single and Parallel Operation

Electrical Specifications *(continued)*

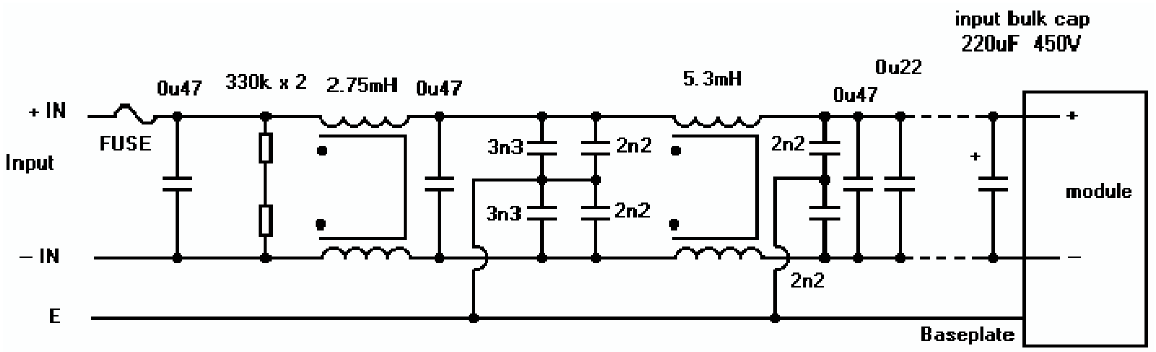


Figure 4. EMI Filter Schematic for AIF Series

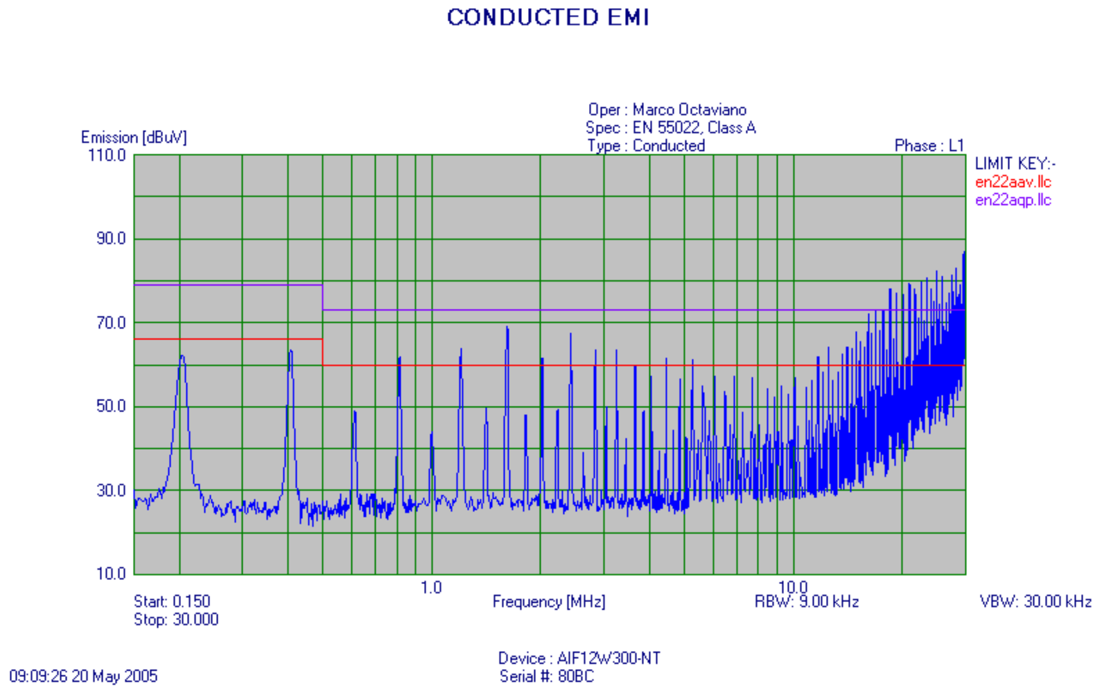


Figure 5. EMI Filter Scan (without Filter)

Performance Curves

AIF12W300

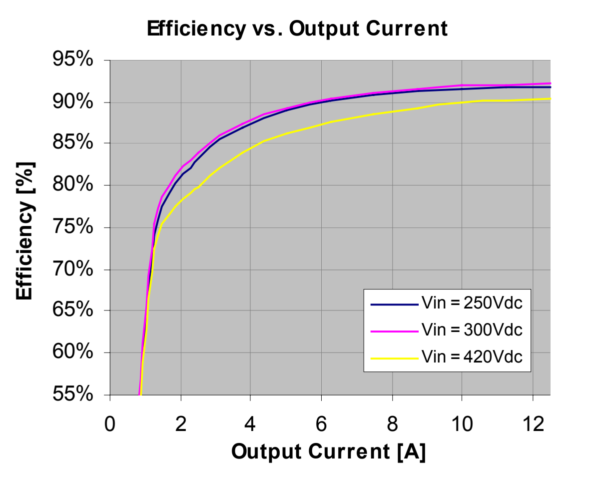


Figure 6. Efficiency vs. Load Current at Ambient Temperature (T_A) = 25°C.

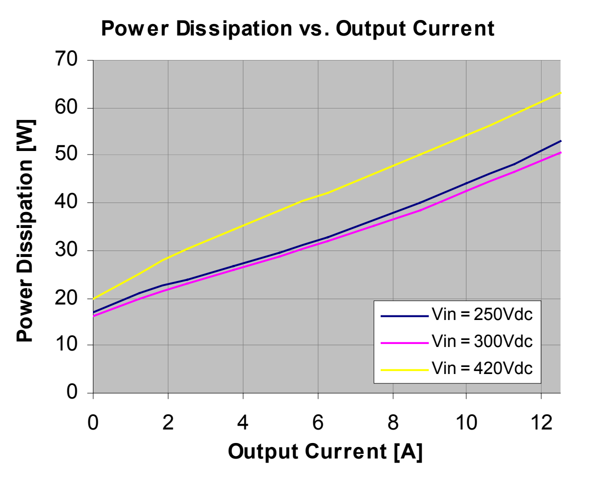


Figure 7. Power Dissipation vs. Load Current at Ambient Temperature (T_A) = 25°C.

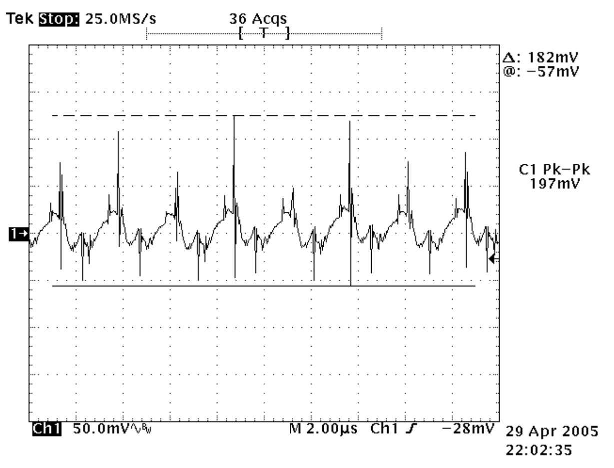


Figure 8. Output Ripple Waveform, Vin = 300V, Io = 12.5A, at Ambient Temperature (T_A) = 25°C.

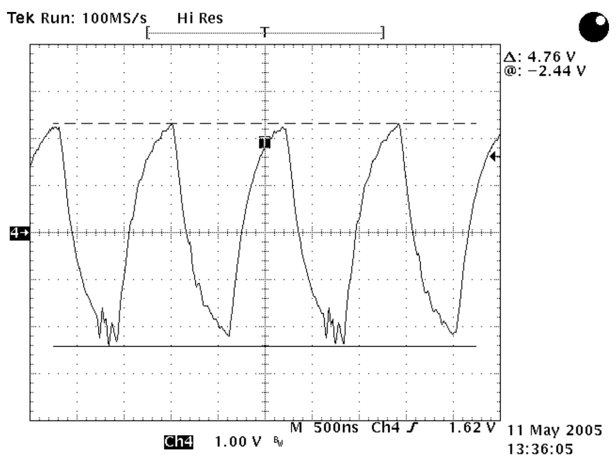


Figure 9. Clock Out Waveform, Vin = 300V, Io = 12.5A, at Ambient Temperature (T_A) = 25°C.

Performance Curves

AIF12W300 ***(continued)***

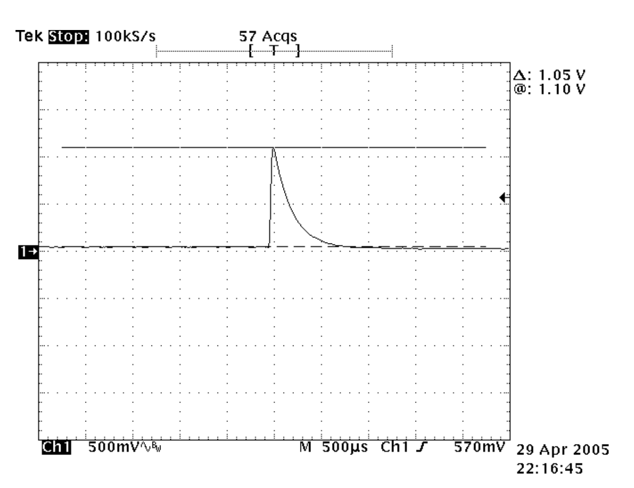


Figure 10. Transient Response-Vout Deviation (Hi-Lo) at Ambient Temperature (T_A) = 25°C.

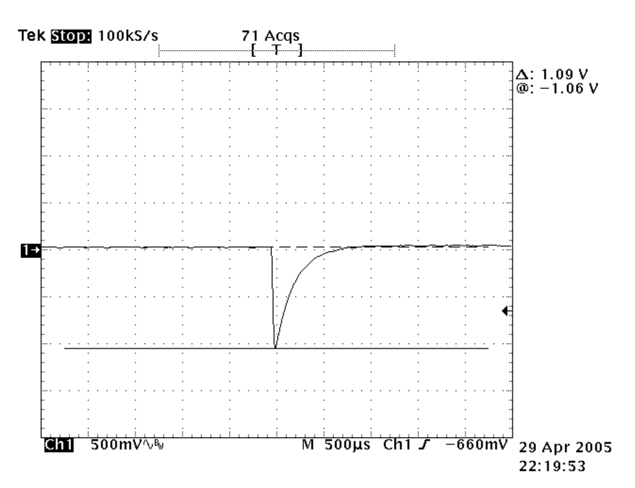


Figure 11. Transient Response-Vout Deviation (Lo-Hi) at Ambient Temperature (T_A) = 25°C.

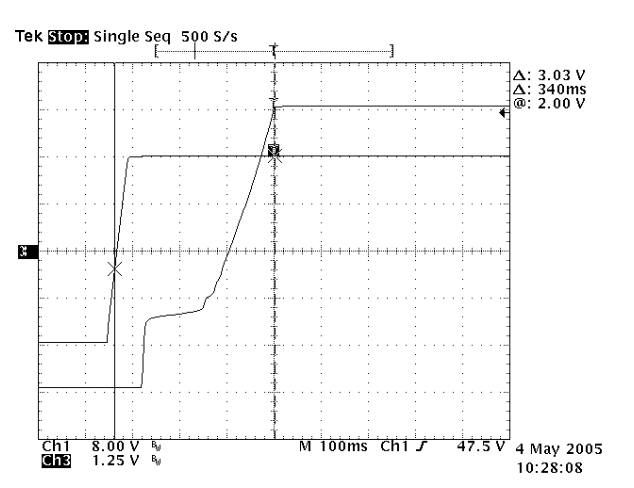


Figure 12. Turn-on Time (Enable to Output) at Ambient Temperature (T_A) = 25°C.

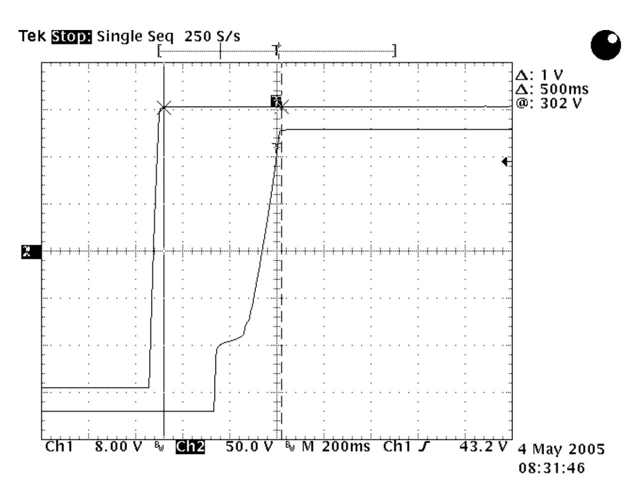
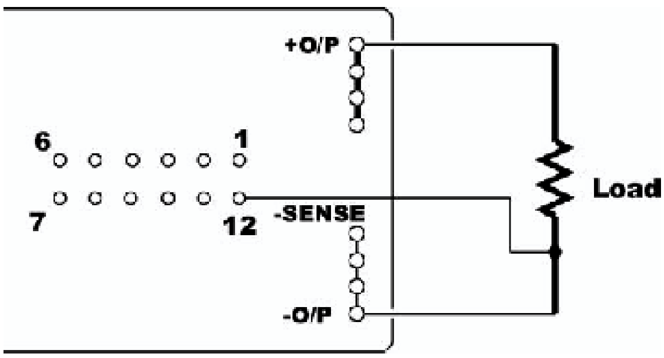


Figure 13. Turn-on Time (Input to Output) at Ambient Temperature (T_A) = 25°C.

Basic Operation and Features

Remote Sense (+SENSE, -SENSE)

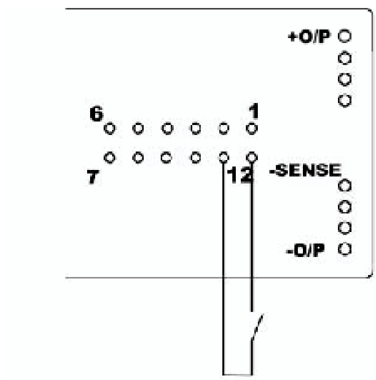
Connect the +SENSE and –SENSE pins of the module directly to the load to allow the module to compensate for the voltage drop across the conductors carrying the load current. If remote sensing is not required (for example if the load is close to the module) the sense pins should be connected directly to the module's output pins to ensure accurate regulation.

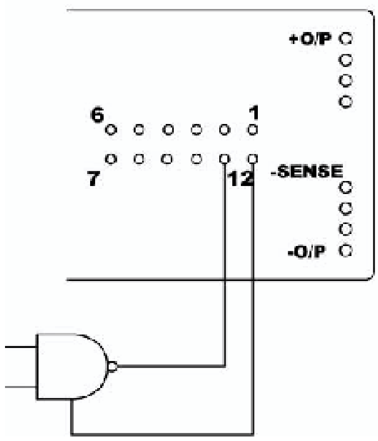


Note: If the sense leads fail open circuit, the module will revert to local sense at the output pins. Incorrect connection of sense leads may damage the module. Remote Sense compensation at nominal V_O only.

Enable Control (ENABLE)

The enable pin is a TTL compatible input used to turn the output of the module on or off. The output is enabled when the ENABLE pin open or driven to a logic high >2V, and disabled when the ENABLE pin is connected to –SENSE or driven to a logic low of < 0.7V.

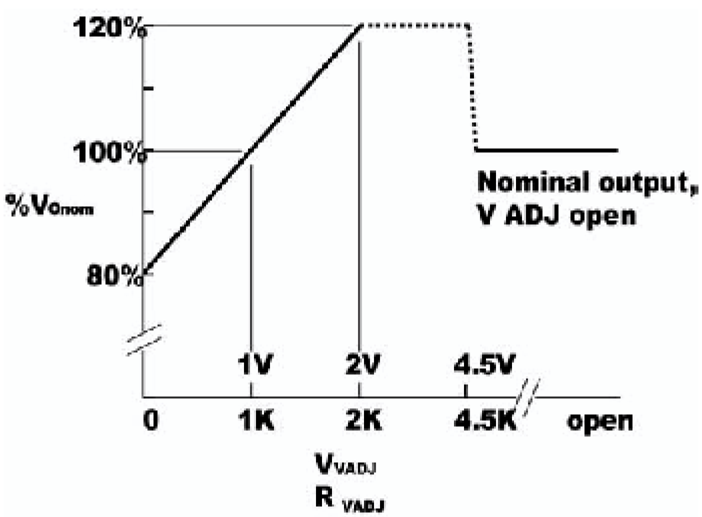


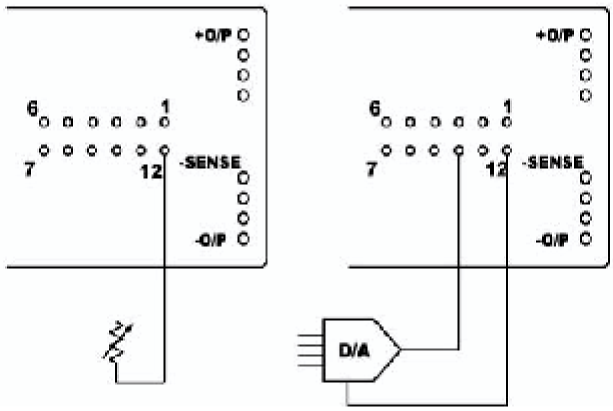


Basic Operation and Features *(continued)*

Output Voltage Adjustment (V ADJ)

The output voltage of the module may be accurately adjusted by up -20%, +20% of the nominal factory set output. Adjustment is carried out using either an external voltage source (0 to 2V, capable of sinking 1mA) or resistor (0 to 2K) connected between VADJ and –SENSE.

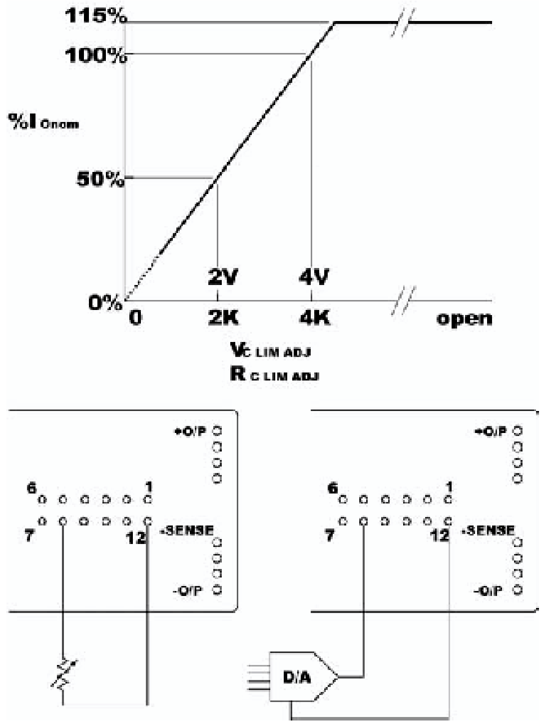




Basic Operation and Features *(continued)*

Current Limit Adjustment (C LIM ADJ)

A constant current limiting circuit protects the module under overload or short circuit conditions. With the C LIM ADJ pin left unconnected, the current limit is factory set to 115% of the module's rated output. Current limit may be adjusted across the range from 20% to 100% using an external voltage source (0.8 to 4V, capable of sinking 1mA) or a resistor (800R to 4K) connected between C LIM ADJ and –SENSE.

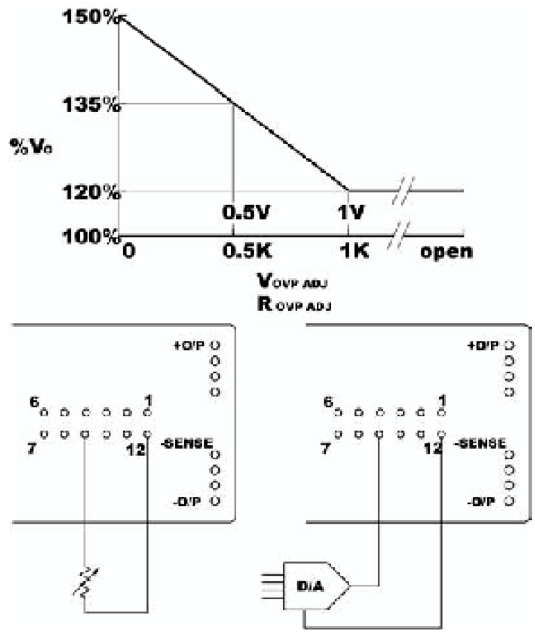


Overvoltage Protection Adjustment (OVP ADJ)

An independent overvoltage circuit monitors the module's output pins and will shut the module down in the event of an internal or external fault which causes the output voltage to rise above the preset limit. The module is reset by removing and re-applying the input power or toggle the ENABLE OFF/ON.

The overvoltage set point may be adjusted between 20% and 50% above the output voltage (V_O), and automatically track adjustments made to the output voltage using V ADJ.

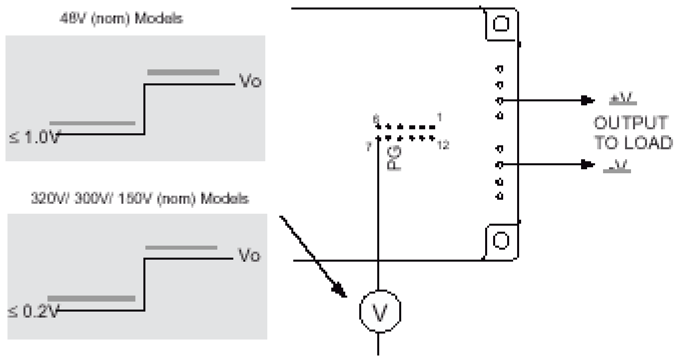
OVP ADJ should be used to increase the OVP margin when the voltage drop between power output pins and remote sense is more than 0.2V.



Basic Operation and Features *(continued)*

Power Good / Identification (PG/ID)

This pin provides an indication that the module's converters are working, and can also be used to identify the factory set output voltage of the module. The PG/ID pin goes high to the level of the output voltage (V_O) to indicate that the module is operating and delivering power. The output goes low if the converters stop operating due to a fault such as an overtemperature or overvoltage condition. The PG/ID pin will also go low if the module is disabled via the ENABLE pin or under light load condition.



The resistance between the PG/ID pin and the +ve output of the module can be used to identify the module with no power applied according to the table:

Model Number	Resistance (kΩ)
AIF12W300-L	47
AIF12W300N-L	47
AIF12W300-NTL	47
AIF12W300N-NTL	47

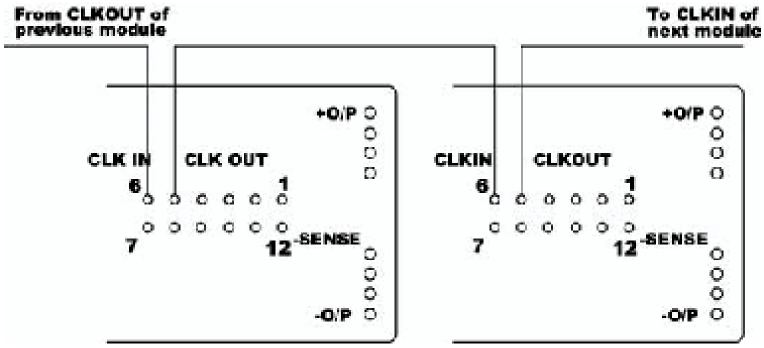
Basic Operation and Features *(continued)*

Clock Signals (CLK IN, CLK OUT)

The module's internal clock is accurate and stable over its full operating range and synchronization is not normally required, but it can reduce noise in paralleled systems.

Clock signals can be wired in series (the CLK OUT pin of one module to the CLK IN pin of the next etc) in which case all the modules will be synchronized with the first module in the chain. Alternatively, an external clock signal of $5V_{pk\text{-}pk}$ at 800KHz ±10% can be connected to the CLK IN pins of all the modules.

If the clock input to any module fails, the module will automatically switch back to its internal clock and will continue to operate normally. The CLK IN and CLK OUT signals are AC coupled, so any module can clock another module regardless of polarity.

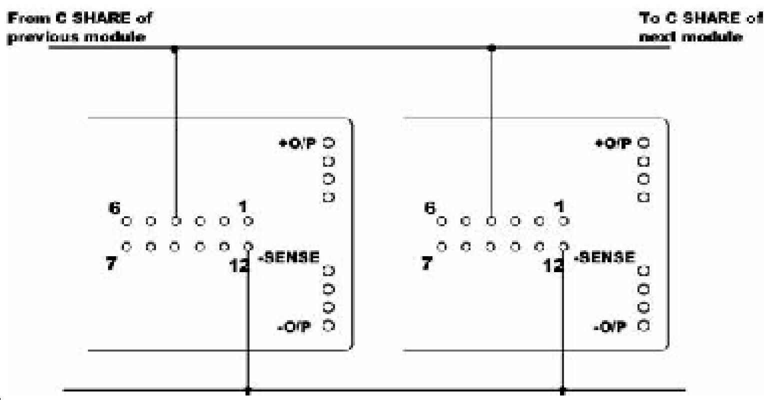


Current Share (CSHARE)

To ensure that all modules in a parallel system accurately share current, the C SHARE pins on each module should be connected together.

The voltage on the C SHARE pins represents the average load current per module. Each module compares this average with its own current and adjusts its output voltage to correct the error. In this way the module maintains accurate current sharing.

Note: The –SENSE and +SENSE pins of each module must also be connected together to ensure accurate current_sharing.

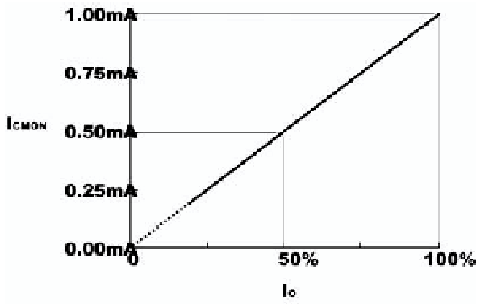


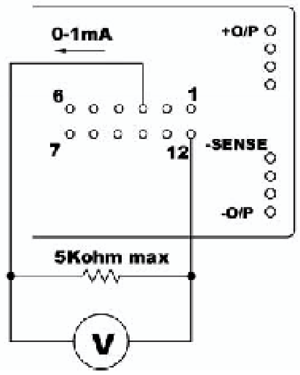
Basic Operation and Features *(continued)*

Current Monitoring (C MON)

The C MON pin provides an indication of the amount of current supplied by the module. The output of the C MON pin is a current source proportional to the output current of the module, where 0.2 to 1mA = 20 to 100% Iorated.

The C MON output can be paralleled with C MON outputs from other modules to indicate the total current supplied in a paralleled system.



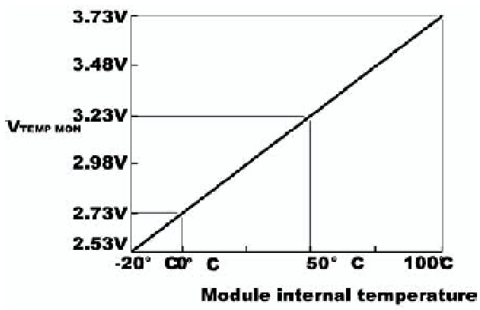


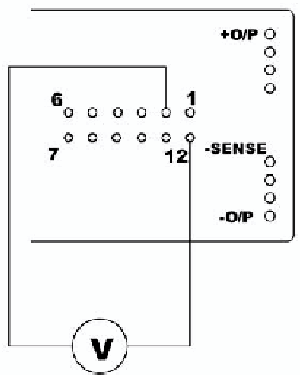
Temperature Monitoring (TEMP MON)

The TEMP MON pin provides an indication of the module's internal temperature. The voltage at the TEMP MON pin is proportional to the temperature of the module baseplate at 10mV per °C, where:

Module temperature (°C) = (Vtemp mon X 100) – 273

The temperature monitor signal can be used by thermal management systems (e.g. to control a variable speed fan). It can also be used for overtemperature warning circuits and for thermal design verification of prototype power supplies and heatsink.

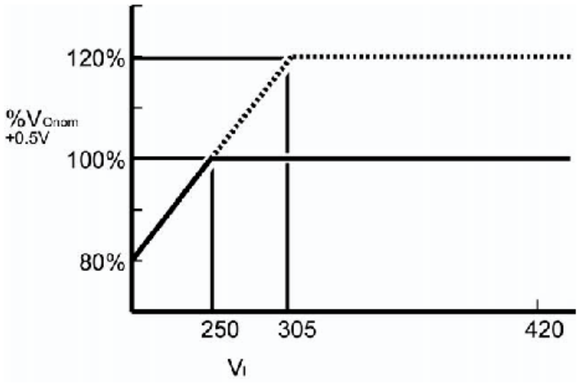




Basic Operation and Features *(continued)*

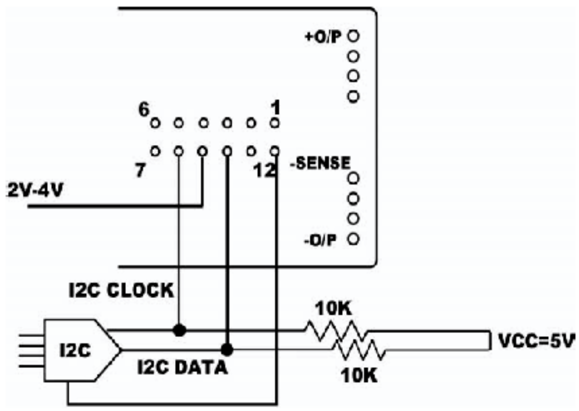
Break Regulation

AIF12W300–Series modules are designed to deliver full rate output current at up to 0.5V above $V_{O\ nom}$ at the minimum specified input voltage.



I²C Digital Control (DCS, I²C CLK, I²C DATA)

The module shall be capable to be controlled by I²C interface, which is SMBus compatible, via I²C CLK and I²C DATA pins. These two pins share the same pin location of CLIM ADJ and V ADJ pins respectively. Digital control is selected when Digital Control Select (DCS) pin voltage is between 2V to 4V. When digital control is selected, analog adjust pin function is disabled. DCS signal shall only be applied when the module is powered off or disabled. An external 10k pull-up resistor is necessary for each I²C CLK, and I²C DATA pin, for 100kHz I²C bus frequency.



Basic Operation and Features *(continued)*

I[2]C COMMUNICATION PROTOCOL

1. Command word

Command word is sent by master system to inform slave device that what kind of operation the master like to do. It is a 16-bit data. Bit 0 to bit 9 indicate the data need to transfer (e.g. the value of OV_ADJ). As there are two different lengths of data, one is 8-bit and the other is 10-bit. So, if 10-bit data is transmitting/receiving, whole 10 bits (DATA9 – DATA0) will be used. In 8 bits case, only the least significant 8 bits (DATA7 – DATA0) will be used. The two bits (DATA9 and DATA8) will be cleared. The 5 bits (REG4 – REG0) indicate which command needs to. When the master requests data from the slave, the DATA9-DATA0 bits should be cleared. And during setting the four information items (Model Name, Serial No., Firmware Version, Model Revision), DATA9-DATA8 should be cleared and is followed by the actual data.

The format of the 16-bits command word is as follow:

Bit 15 … Bit 8

DSR	REG4	REG3	REG2	REG1	REG0	DATA9	DATA8

Bit 7 … Bit 0

DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

The DSR (Data Set Read) bit controls read/write of data. If the master send a 0 (write operation) for this bit, the slave device will get the command register and data. And then set the value of the corresponding command register. If the master sends a 1 (read operation) for this bit, the slave device will get the current value of the corresponding command register and send it to the master.

The table below shows the register mapping:

Command Register	Coding (REG4 – REG0)
MODEL_NO (read/write*)	00000
SERIAL_NO (read/write*)	00001
FIRMWARE_VER (read/write*)	00010
MODEL_REV (read/write*)	00011
SLAVE_ADDRESS (read/write)	00100
OVP_ADJ (read/write)	00101
V_ADJ (read/write)	00110
CLIM_ADJ (read/write)	00111
TMON (read only)	01000
VOUT (read only)	01001
CMON (read only)	01010
RESET (write only)	01111
LOCK (write only*)	10000
UNLOCK (write only*)	10001

* Remark: write functions only used to production.

I²C COMMUNICATION PROTOCOL *(continued)*

2. Data Transfer Structure on I²C Bus

Terms	Description	No. of bits
Stt	Start bit	1
Sadd	Slave address	8
Ack	Acknowledge	1
Bt-H	Higher byte	8
Bt-L	Lower byte	8
StD(1st, 2nd,…nth)	String of bytes(1st byte, 2nd byte,……nth byte)	8
Stp	Stop Bit	1

In the block diagram below, gray boxes indicate master-send signal; white boxes indicate slave-send signal.

Master	Slave

2.1 Set data to slave

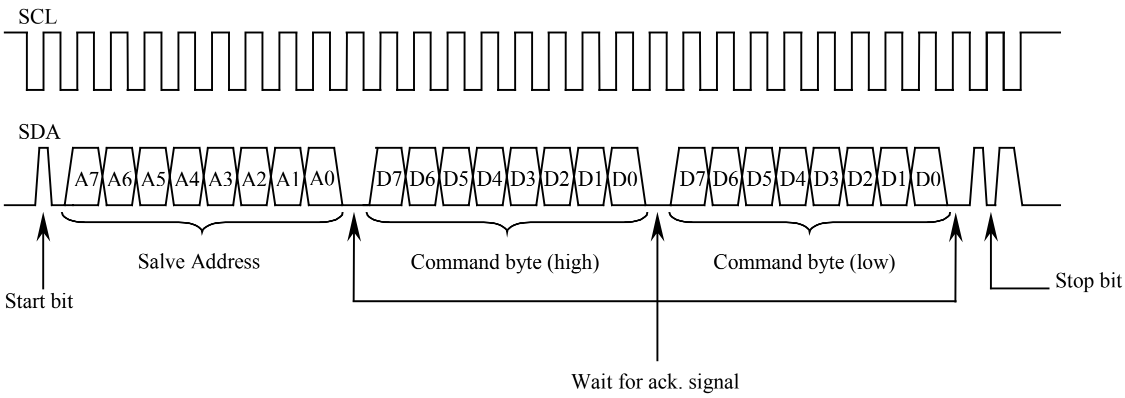


Fig 1.1 SCL and SDA signal in write mode.

S	SAdd	Ack	Bt-H (command)	Ack	Bt-L (command)	Ack	Stp

Fig 1.2 Block diagram of write mode.

Procedures:
1. The master device gives a Start condition via SDA.
2. Master sends the 8-bit slave address in which bit 0 of it should be 0 (0 indicate a write condition to slave) via SDA.
3. The addressed slave device give out acknowledge via SDA.
4. The master sends the high byte of command code via SDA.
5. The slave give out acknowledge via SDA.
6. The master sends the low byte of command code via SDA.
7. Slave gives out acknowledge after receiving the last byte.
8. Master gives a STOP condition via SDA to stop the transaction.

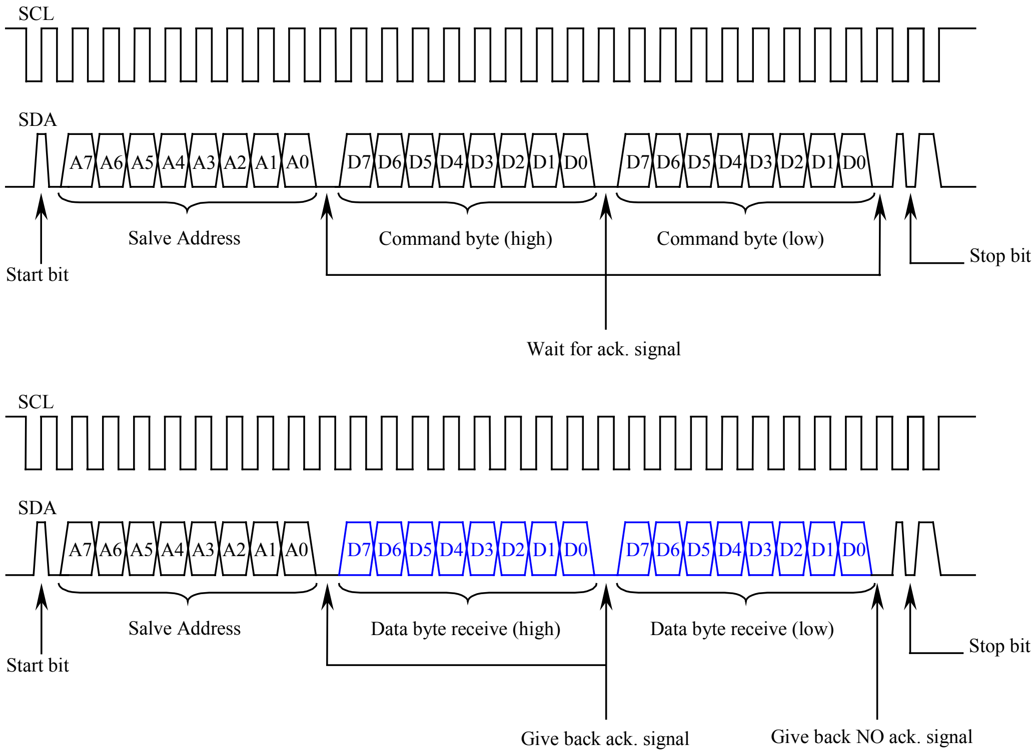


Fig. 2.1 SCL and SDA signal of read mode (2 bytes of data read).

S	SAdd	Ack	Bt-H (command)	Ack	Bt-L (command)	Ack	Stp

S	SAdd	Ack	Bt-H (data)	Ack	Bt-L (data)	Ack	Stp

Fig. 2.2 Block diagram of read mode (2 bytes of data read).

2.2 Read data from slave (2-byte data)

Procedures:

1. The master device gives out a start condition on SDA.
2. Master sends the 8 bits slave address which bit 0 of it should be 0 (0 indicates write mode for slave) via SDA.
3. The addressed slave device gives back acknowledge via SDA.
4. Master sends out the high byte of the 2-bytes command word.
5. Slave device gives back acknowledge again.
6. Master sends out the low byte of the 2-bytes command word.
7. Slave device gives back acknowledge again.
8. Master sends out a stop condition to prepare for the next transaction.
9. Master gives out a start condition again for the next transaction.
10. Master sends the 8 bits slave address which bit 0 of it should be 1(1 indicates read mode for slave) via SDA.
11. Slave give back an acknowledge.
12. Slave then sends out the high byte of desired data.
13. Master gives back acknowledge to slave.

14. Slave sends the low byte of the desired data.

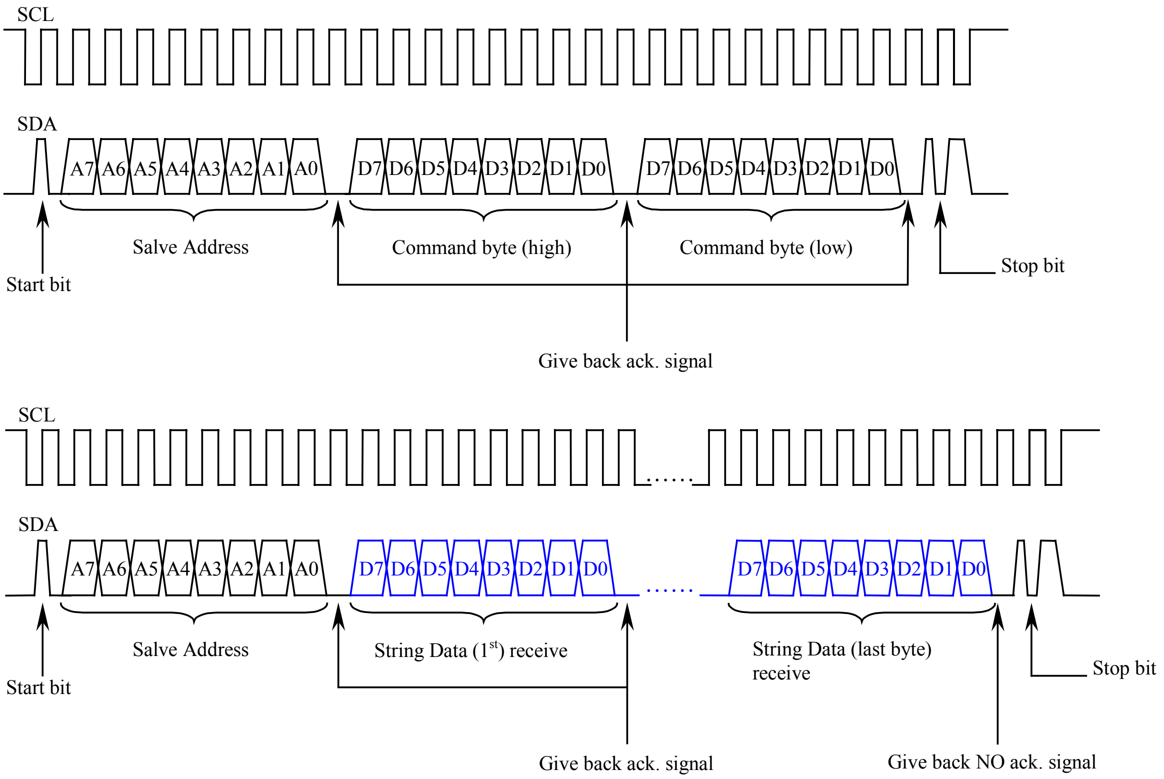


Fig 3.1 SCL and SDA signal of read mode (String of data).

S	SAdd	Ack	Bt-H (command)	Ack	Bt-L (command)	Ack	Stp

S	SAdd	Ack	StD(1st)	Ack	StD(2nd)	Ack	……	StD(nth)	Ack	Stp

Fig 3.1 Block diagram of read mode (String of data).

15. Master gives back acknowledge and sends out a stop condition to close the transaction.

2.3 Read data from slave (string of data)

Procedures:

1. The master device gives out a start condition on SDA.
2. Master sends the 8 bits slave address which bit 0 of it should be 0 (0 indicates write mode for slave) via SDA.
3. The addressed slave device gives back acknowledge via SDA.
4. Master sends out the high byte of the 2-bytes command word.
5. Slave device gives back acknowledge again.
6. Master sends out the low byte of the 2-bytes command word.
7. Slave device gives back acknowledge again.
8. Master sends out a stop condition to prepare for the next transaction.
9. Master gives out a start condition again for the next transaction.
10. Master sends the 8 bits slave address which bit 0 of it should be 1(1 indicates read mode for slave) via SDA.
11. Slave give back an acknowledge.
12. Slave then sends out the first byte of desired data.

13. Master gives back acknowledge to slave.
14. Repeat 12 and 13 until the end of bytes.
15. Master gives back acknowledge and sends out a stop condition to close the transaction.

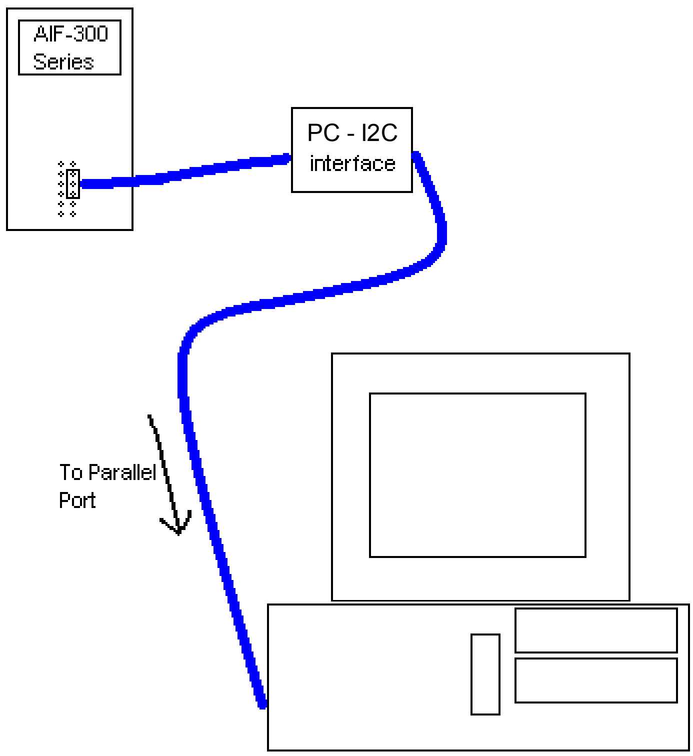
Basic Operation and Features *(continued)*

DIGITAL CONTROL DEMO USER GUIDE

This Demo program is developed to test and evaluate I^2C control features of AIF-300 DC/DC modules.

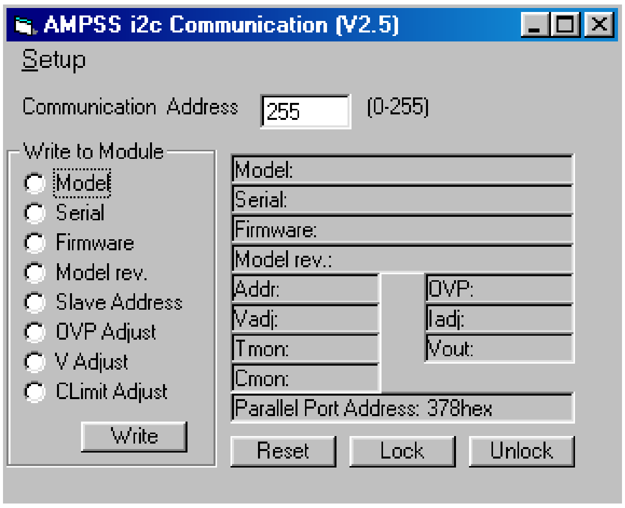
Equipment required:
1. One or more modules of AIF-300 series.
2. PC – Module interface hardware.
3. PC (with windows 98 / Me inside)

Hardware setup:
The picture shown below is the setup of the hardware.

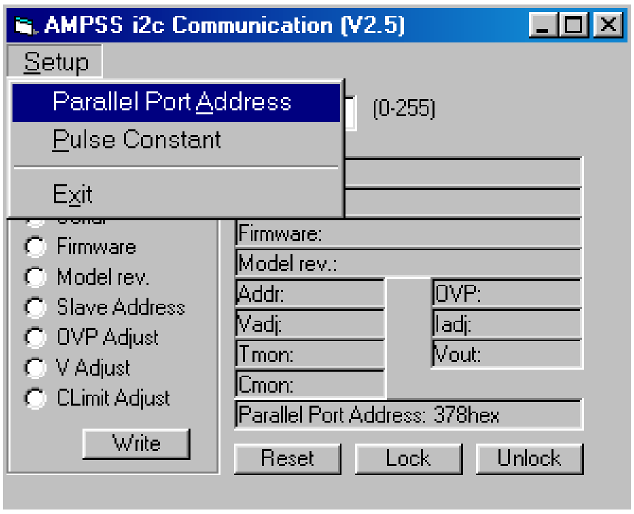


DIGITAL CONTROL DEMO USER GUIDE ***(continued)***

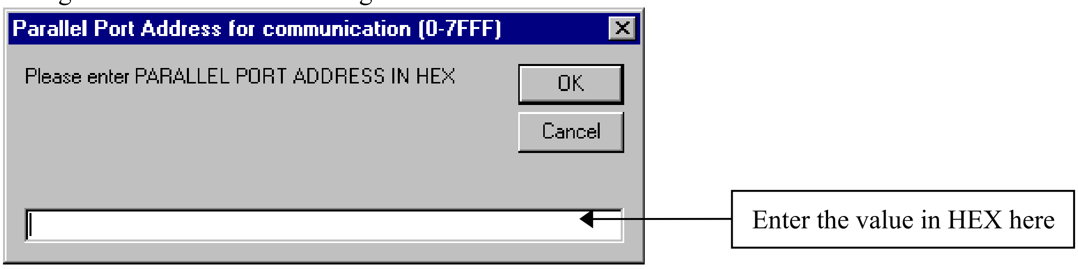
Software Setup:
1. Click on the program "Ampss68.exe". Then following dialog box shows:



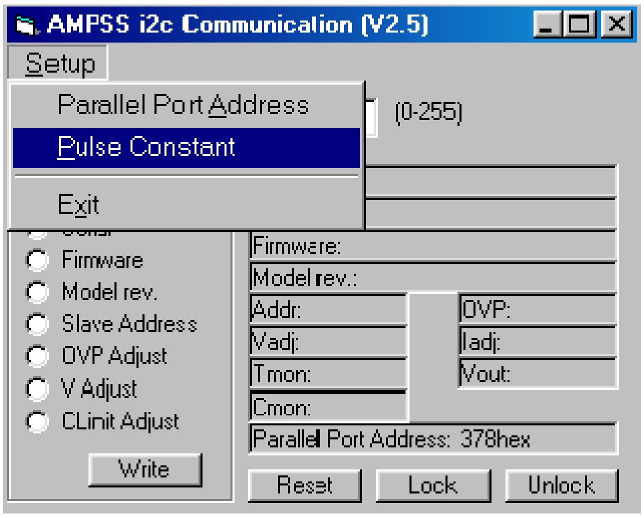
2. Click on "Setup" and choose "Parallel Port Address".



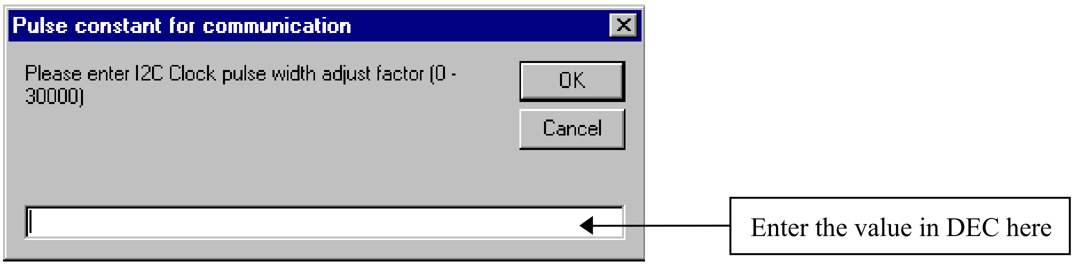
Then a new dialog box shows and enter the right value into it and click "OK":



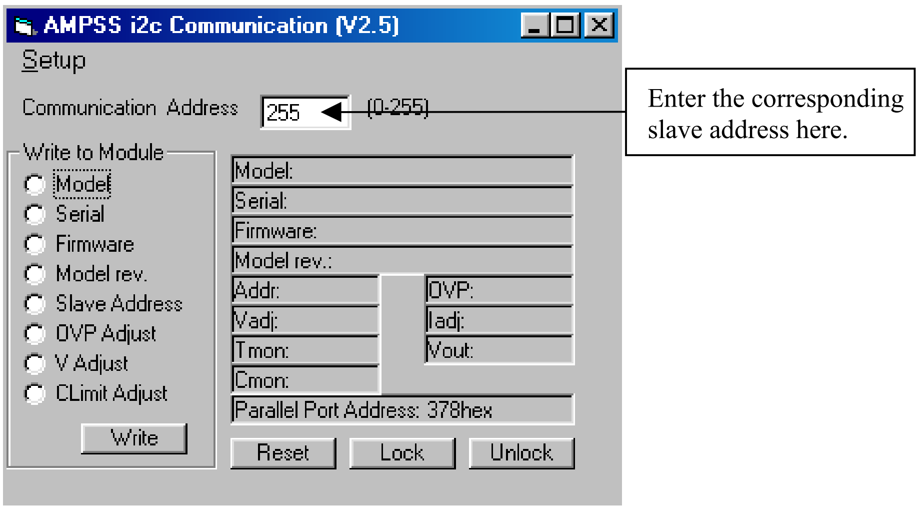
3. Then click on “Setup” and choose “Pulse Constant”.



Also set the desired pulse constant value into the dialog box below and click “OK”:

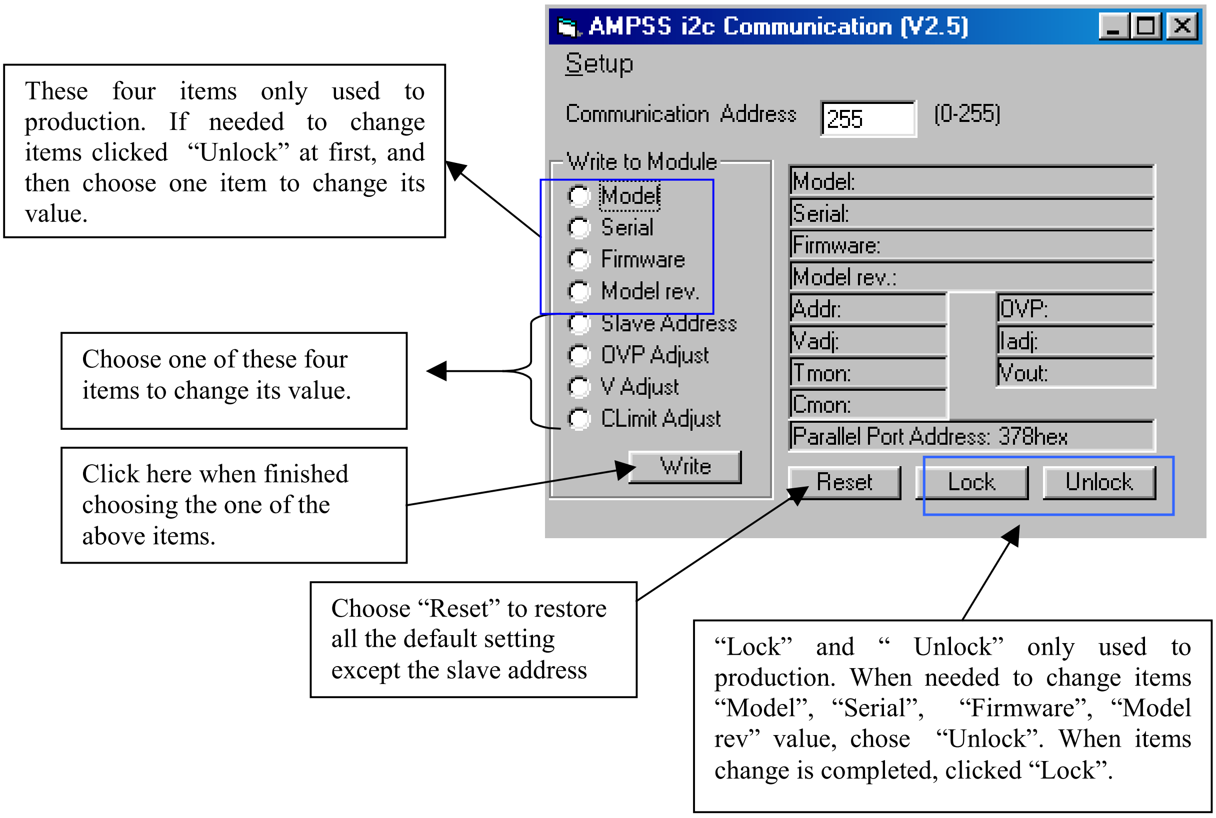


4. Select Module:
Enter the slave address of the module that you want to control:



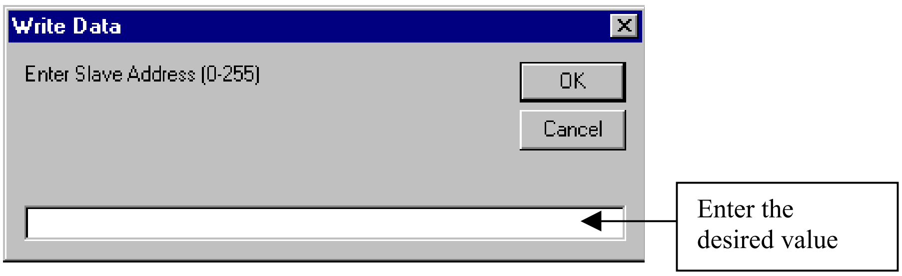
Note: “0” and “1” are the globe address of MMIIC. So, it can only perform “write” function when the UUT address is set to 0 or 1.

5. Write Value:



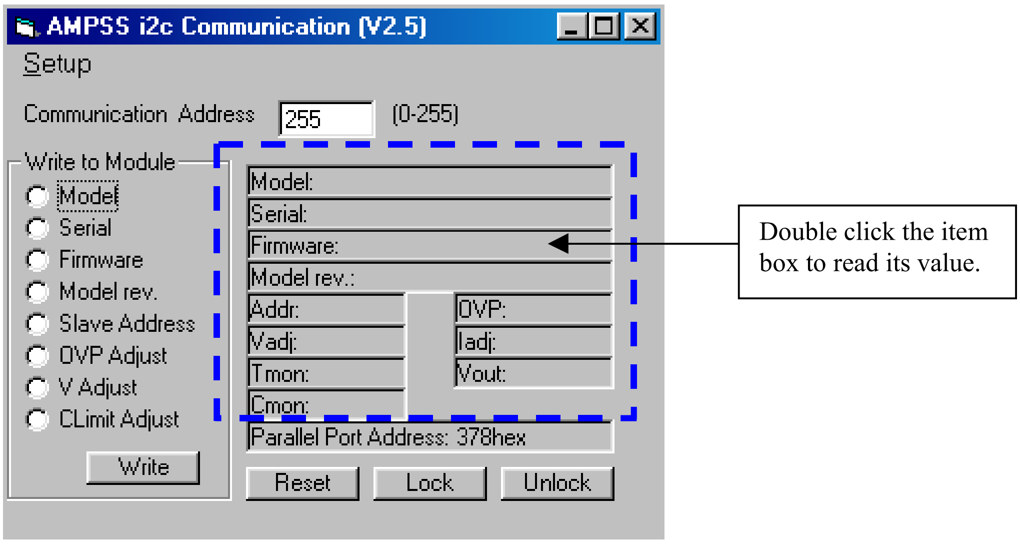
Click on the circle beside the desired item that needs to be changed its value.

After choosing the desired item, click on "Write" below the items. Then a new dialog box shows (except "Reset" option).

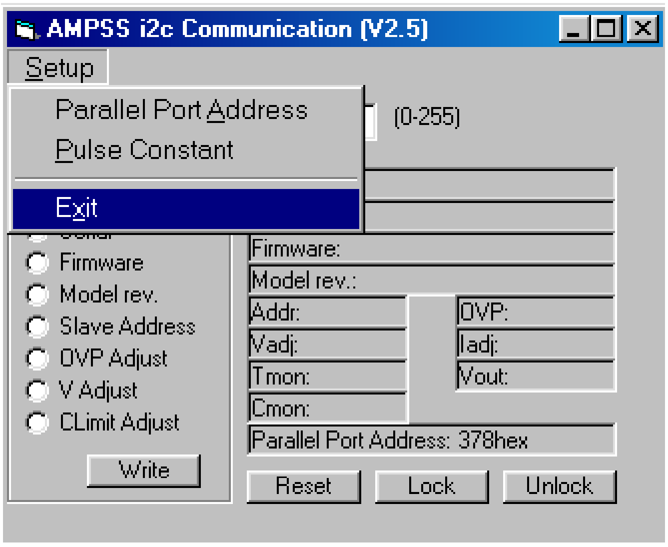


Fill the box with the new value and click "OK". Or click "Cancel " to cancel this operation.

6. Read Value:
Double click on the item box to read the corresponding value:

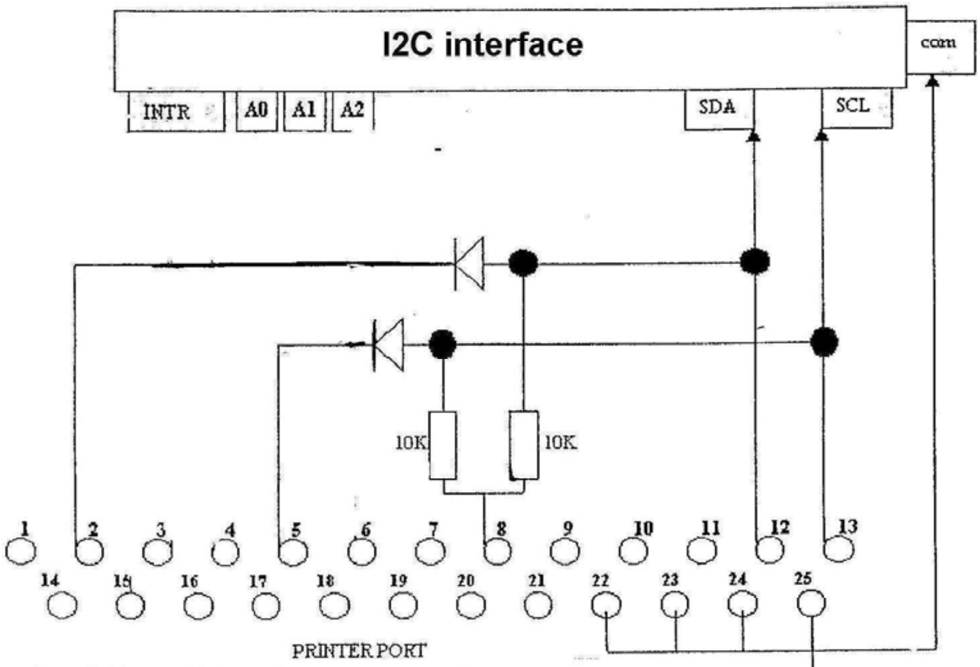


7. Exit Program:
Click on "Setup" and choose "Exit" to exit the program.



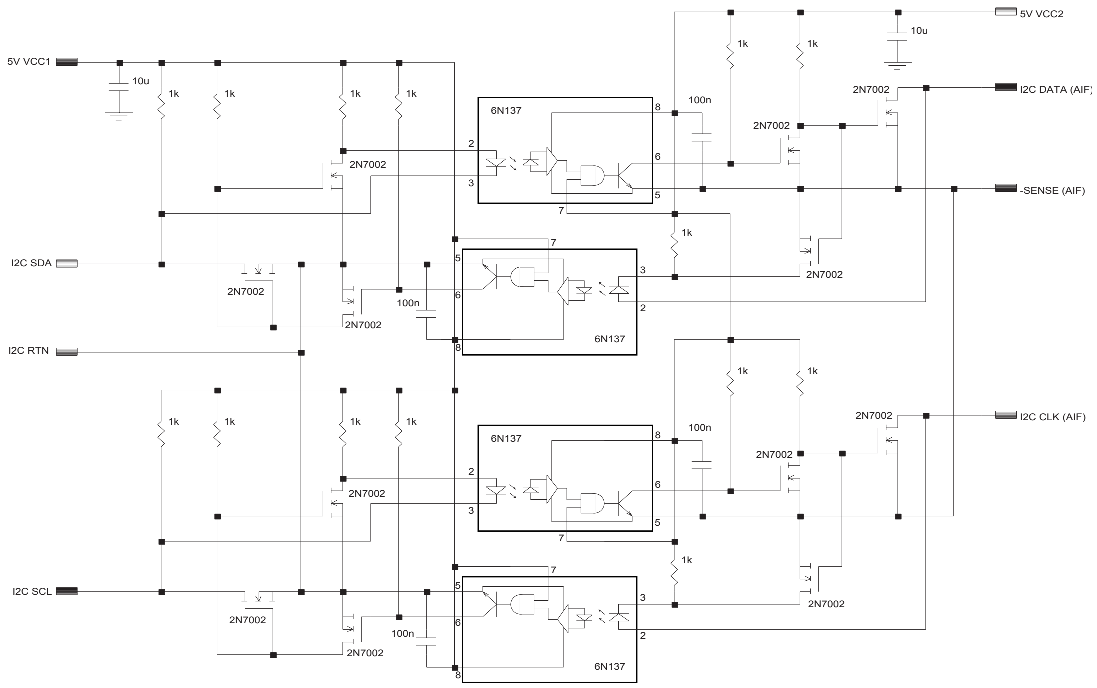
Basic Operation and Features *(continued)*

PC-I2C INTERFACE CIRCUIT DIAGRAM

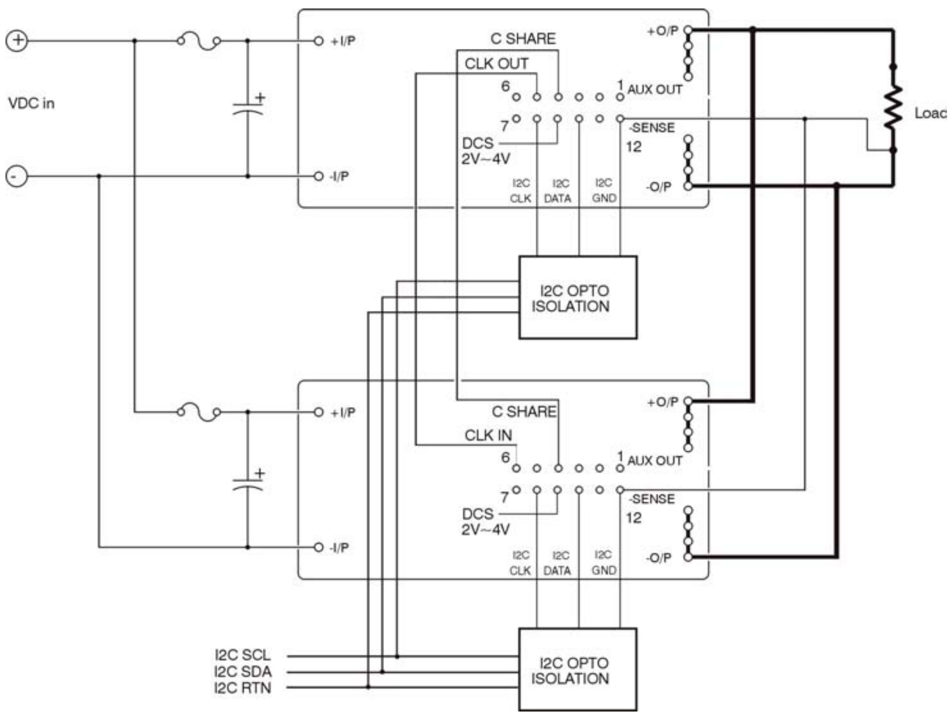


Base Address: (data port)
Pin2 = D0, Pin 5= D3, Pin 8=D6
Base Address+1 (status register)
Pin12 = Bit 5: Paper End, Pin 13= Bit 4: Select, Pin 15 = Bit 3: Fault
Ground Pin (Pin 18 to 25)

Basic Operation and Features *(continued)*



RECOMMENDED OPTO ISOLATION CIRCUIT



PARALLEL OPERATION WITH OPTO ISOLATION

Basic Operation and Features *(continued)*

DIGITAL CONTROL

The module shall be capable to be controlled by I^2C interface, which is SMBus compatible, via I^2C CLK and I^2C DATA pins. These two pins share the same pin location of CLIM ADJ and V ADJ pins respectively. Digital control is selected when Digital Control Select (DCS) pin voltage is between 2V - 4V.

There are 7 command registers for read operation, 4 command registers for read/write operation and 1 command register for write operation.

Command Register	Description
MODEL_NO (read only)	Read model name of the module
SERIAL_NO (read only)	Read serial number on bar code label
FIRMWARE_VER (read only)	Read firmware version
MODEL_REV (read only)	Read model revision
SLAVE_ADDRESS (read/write)	Read or set slave address of the module
OVP_ADJ (read/write)	Read or set overvoltage protection threshold of the module
V_ADJ (read/write)	Read or set output voltage of the module
CLIM_ADJ (read/write)	Read or set current limit protection threshold of the module
TMON (read only)	Read baseplate temperature of the module
VOUT (read only)	Read output voltage of the module
CMON (read only)	Read output current of the module
RESET (write only)	Reset all control parameters to factory setting

DIGITAL DATA CONVERSION

Each control and monitoring data is in 10-bit format. The data conversion formulae are as follows.

OVP_ADJ:

The range of the OVP_ADJ can be adjusted from 125% to 145% of V_O (nom). The received/transmitted data is calculated by the equation below.

Receive Data (from module to PC):
Input Data: MCU OVPadj (integer)
Output Data: OVPadj% (round to 1decimal place)

$$\text{OVPadj\%} = 145\% - \frac{\text{MCU OVPadj}}{205} \times 20\%$$

Transmit Data (from PC to module):
Input Data: OVPadj (round to 1 decimal place)
Output Data: MCU OVPadj (integer)

$$\text{MCU OVPadj} = \frac{145\% - \text{OVPadj}\%}{20\%} \times 205$$

DIGITAL DATA CONVERSION *(continued)*

V_ADJ:

1. V_adj range between 80% to 120% module: (5Vo and above model)
   The range of the V_ADJ can be adjusted from 80% to 120% of V_O (nom). The received/transmitted data is calculated by the equation below.

Receive Data (from module to PC):
Input Data: MCU Vadj (integer)
Output Data: Vadj% (round to 1decimal place)

$$\text{Vadj}\% = 80\% + \frac{\text{MCU Vadj}}{410} \times 40\%$$

Transmit Data (from PC to module):
Input Data: Vadj (round to 1 decimal place)
Output Data: MCU Vadj (integer)

$$\text{MCU Vadj} = \frac{\text{Vadj}\% - 80\%}{40\%} \times 410$$

2. V_adj range between 50% to 110% module: (Below 5Vo model)
   The range of the V_ADJ can be adjusted from 50% to 110% of V_O (nom). The received/transmitted data is calculated by the equation below.

Vadj between 50% ~100%

Receive Data (from module to PC):
Input Data: MCU Vadj (integer)
Output Data: Vadj% (round to 1decimal place)

$$\text{Vadj}\% = 50\% + \frac{\text{MCU Vadj}}{205} \times 50\%$$

Transmit Data (from PC to module):
Input Data: Vadj (round to 1 decimal place)
Output Data: MCU Vadj (integer)

$$\text{MCU Vadj} = \frac{\text{Vadj}\% - 50\%}{50\%} \times 205$$

DIGITAL DATA CONVERSION *(continued)*

Vadj between 100% ~110%.

Receive Data (from module to PC):

Input Data: MCU Vadj (integer)

Output Data: Vadj% (round to 1decimal place)

$$Vadj\% = 100\% + \frac{MCU\ Vadj - 205}{205} \times 10\%$$

Transmit Data (from PC to module):

Input Data: Vadj (round to 1 decimal place)

Output Data: MCU Vadj (integer)

$$MCU\ Vadj = \frac{Vadj\% - 90\%}{10\%} \times 205$$

CLIM_ADJ:

The range of the CLIM_ADJ can be adjusted from 0% to 102.5% or 110% of rated I_O. The received/transmitted data is calculated by the equation below.

Receive Data (from module to PC):

Input Data: MCU CLIMadj (integer)

Output Data: CLIMadj% (round to 1decimal place)

Case 1: MCU CLIMadj $\neq 841$

$$CLIMadj\% = \frac{MCU\ CLIMadj}{840} \times 102.5\%$$

Case 2: MCU CLIMadj >= 841

$$CLIMadj\% = 110\%$$

Transmit Data (from PC to module):

Input Data: CLIMadj (round to 1 decimal place)

Output Data: MCU CLIMadj (integer)

Case1: CLIMadj% $\neq 110\%$

$$MCU\ CLIMadj = \frac{CLIMadj\%}{102.5\%} \times 840$$

Case2: CLIMadj% >= 110%

$$MCU\ CLIMadj = 841$$

DIGITAL DATA CONVERSION *(continued)*

TMON:

Baseplate temperature monitoring is a read only data. It is ranged from -40°C to 120°C. The temperature of module can be calculated by the equation below:

Receive Data (from module to PC):
Input Data: MCU Tmon (integer)
Output Data: Baseplate Temperature in °C (round to 1 decimal place)

$$\text{Baseplate Temperature in °C} = \frac{\text{MCU Tmon}}{1024} \times 500 - 273$$

VOUT:

Output Voltage is a read only data. The output voltage can be calculated by the equation below:

Receive Data (from module to PC):
Input Data: MCU Vout (integer)
Output Data: Output Voltage in %Vonom (round to 1 decimal place)

$$\text{Output Voltage in \%Vonom} = \frac{\text{MCU Vout}}{Vo\_REF} \times 100\%$$

Module name	**$Vo_{\_REF}$**
AIF120Y300-L/N-L/-NTL	369
AIF120F300-L/N-L/-NTL	676
AIF80A300-L/N-L/-NTL	813
AIF50B300-L/N-L/-NTL	820
AIF40C300-L/N-L/-NTL	830
AIF25H300-L/N-L/-NTL	820
AIF12W300-L/N-L/-NTL	820

DIGITAL DATA CONVERSION *(continued)*

CMON:

Current monitoring is a read only data. It is ranged from 0% to 100% of rated I_O. The output current of module can be calculated by the equation below:

Receive Data (from module to PC):
Input Data: MCU Cmon (round to 1 decimal place)
Output Data: Output Current Monitor in % $I_{O\ max}$ (integer)

$$\text{Output Current Monitor in \%Iomax} = \frac{\text{MCU Cmon}}{614} \times 100\%$$

DEFAULT FACTORY SETTING

Control data	Factory Setting
Slave address	0010100000 (A0h = 160) (8 bit addressing)
OVP_ADJ	0011001101 (00CDh = 205) (125% of V_O)
V_ADJ	0011001101 (00CDh = 205) (100% of V_O (nom))
CLIM_ADJ	1111111111 (0349h = 841) (110% of rated I_O)

Mechanical Specifications

Parameter	Device	Symbol	Min	Typ	Max	Unit
Dimension	All	L W H	- - -	4.60 [116.8] 2.40 [61.0] 0.50 [12.7]	- - -	in [mm] in [mm] in [mm]
Weight	All		-	250	-	g [oz]

PIN ASSIGNMENTS		
Input	**Output**	**Control Pins**
31. Positive 32. Negative	21. Positive 22. Positive 23. Positive 24. Positive 25. Negative 26. Negative 27. Negative 28. Negative	1. AUX 2. TEMP MON 3. C MON 4. C SHARE 5. CLK OUT 6. CLK IN 7. PG/ID 8. C LIM ADJ/I^2C CLK 9. OVP ADJ/DCS 10. V ADJ/I^2C DATA 11. ENABLE 12. - SENSE

PART NUMBERING SCHEME

AIF	O/P CURRENT	O/P VOLTAGE	Vin	Enable	-	Suffix	Suffix
	xxx	x	300	x		NT	
"AIF" = Astec Integrated Full Brick Series	12 = 12.5A	W = 48V	300V DC	"N" = Negative Logic Enable No suffix = Positive Logic Enable		"-NT" = Non-thread mounting hole	"-L" or "L" = Rohs Compliance

Mechanical Specifications *(continued)*

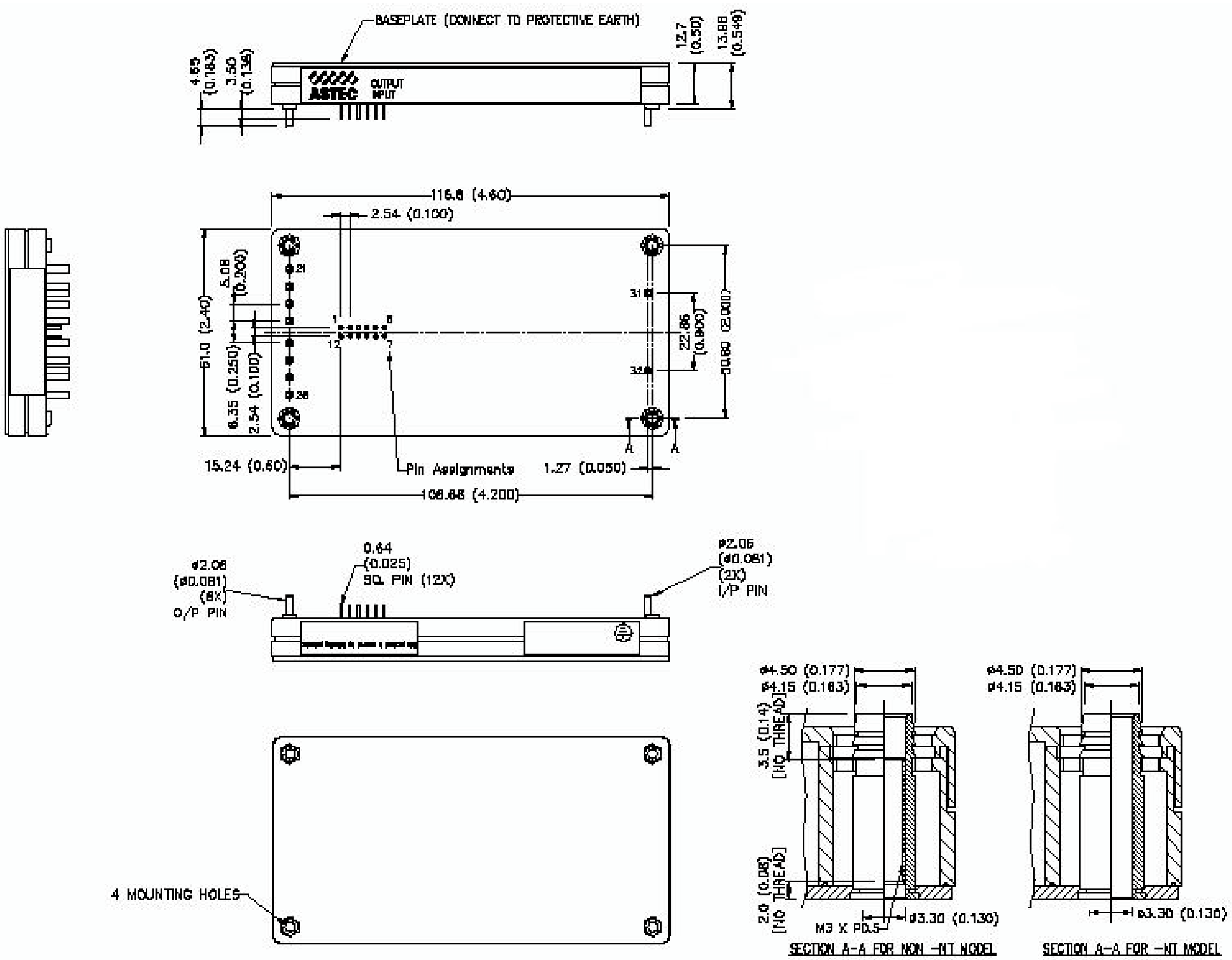


Figure 14. Mechanical Outline Drawing

Please call 1-888-41-ASTEC for further inquiries
or visit us at www.astecpower.com