4-Mbit (256 K × 16) Static RAM

Features

- Temperature ranges
  - Automotive-E: –40 °C to 125 °C
- High speed
  - t_{AA} = 10 ns
- Low active power
  - 468 mW (max)
- 2.0 V data retention
- Automatic power down when deselected
- Independent control of upper and lower bits
- Easy memory expansion with Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) features
- Available in Pb-free 48-ball grid array (BGA) package

Functional Description

The CY7C1041CV33 Automotive is a high performance complementary metal oxide semiconductor (CMOS) static RAM organized as 262,144 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

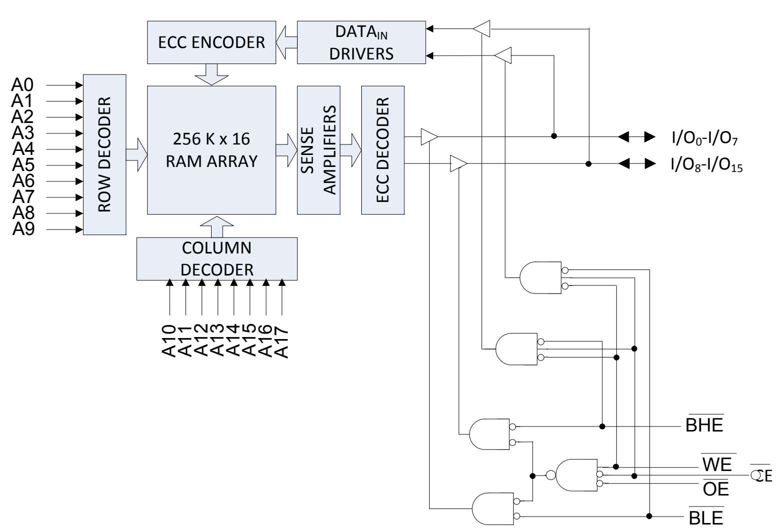
To write to the device, take $\overline{CE}$ and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take $\overline{CE}$ and $\overline{OE}$ LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If $\overline{BLE}$ is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. For more information, see the Truth Table on page 10 for a complete description of Read and Write modes.

The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

For a complete list of related resources, click here.

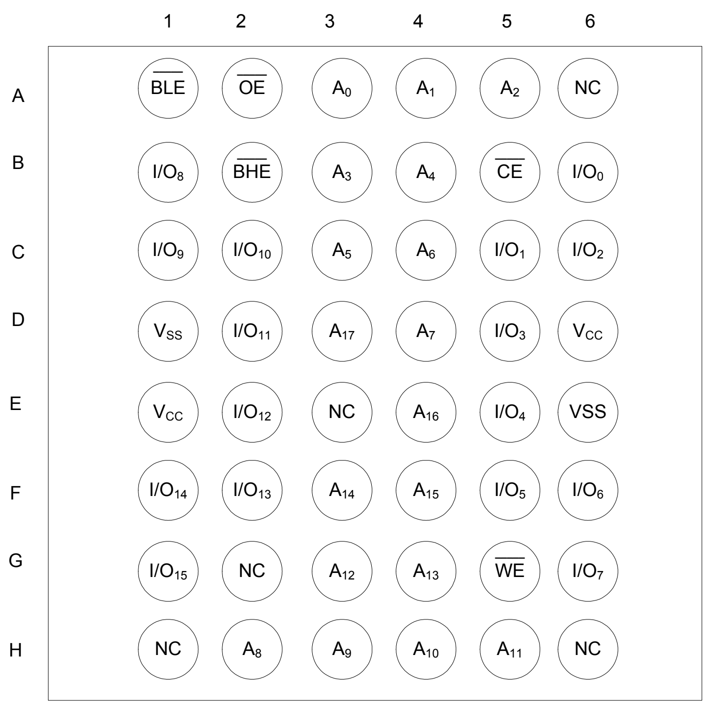
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 48 ball BGA pinout [1]



Selection Guide

Description		-10	Unit
Maximum access time		10	ns
Maximum operating current	Automotive-E	130	mA
Maximum CMOS standby current	Automotive-E	15	mA

Note
1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied .... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND [2] ....–0.5 V to +4.6 V

DC voltage applied to outputs in High Z state [2] ....–0.5 V to V_{CC}+ 0.5 V

DC input voltage [2] ....–0.5 V to V_{CC}+ 0.5 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) ....> 2001 V

Latch up current ....> 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Automotive-E	–40 °C to +125 °C	3.3 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10		Unit
				Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 8.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage [2]			–0.3	0.8	V
I_{IX}	Input leakage current	GND $\leq V_I \leq V_{CC}$	Automotive-E	–20	+20	µA
I_{OZ}	Output leakage current	GND $\leq V_I \leq V_{CC}$, Output disabled	Automotive-E	–20	+20	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Automotive-E	–	130	mA
I_{SB1}	Automatic CE power down current – TTL Inputs	Max V_{CC}, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	Automotive-E	–	45	mA
I_{SB2}	Automatic CE power down current – CMOS inputs	Max V_{CC}, $\overline{CE} \geq V_{CC}$ – 0.3 V, $V_{IN} \geq V_{CC}$ – 0.3 V, or $V_{IN} \leq$ 0.3 V, f = 0	Automotive-E	–	15	mA

Note

2. V_{IL} (min) = –2.0 V for pulse durations of less than 20 ns.

Capacitance

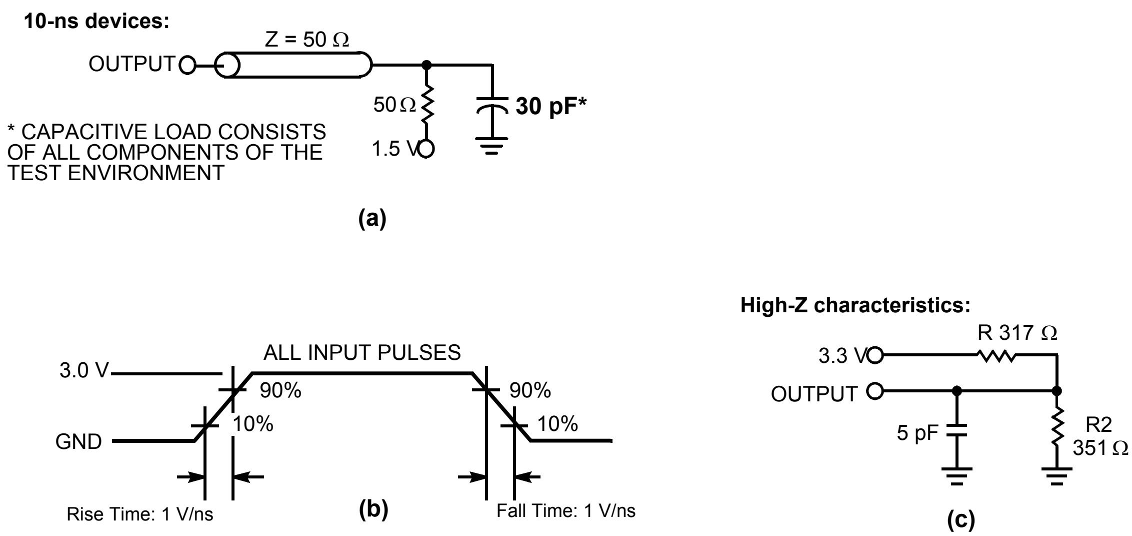
Parameter [3]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	8	pF
C_{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter [3]	Description	Test Conditions	48-ball BGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	38.15	°C/W
Θ_{JC}	Thermal resistance (junction to case)		9.15	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [4]



Notes
3. Tested initially and after any design or process changes that may affect these parameters.
4. AC characteristics (except High Z) for 10-ns parts are tested using the load conditions shown in Figure 2 (a). High Z characteristics are tested using the test load shown in Figure 2 (c).

Switching Characteristics

Over the Operating Range

Parameter [5]	Description	-10		Unit
		Min	Max	
Read Cycle				
t_{power}[6]	V_{CC} (typical) to the first access	100	–	µs
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	10	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [7]	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [7, 8]	–	5	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [7]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [7, 8]	–	5	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power down	–	10	ns
t_{DBE}	Byte enable to data valid	–	6	ns
t_{LZBE}	Byte enable to Low Z	0	–	ns
t_{HZBE}	Byte disable to High Z	–	6	ns
Write Cycle [9, 10]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	7	–	ns
t_{AW}	Address setup to write end	7	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	ns
t_{SD}	Data setup to write end	5	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [7]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [7, 8]	–	5	ns
t_{BW}	Byte enable to end of write	7	–	ns

Notes
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
6. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
7. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
8. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of Figure 2 on page 5. Transition is measured ±500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW, and $\overline{BHE}/\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$, and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a write. The transition of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [11, 12]

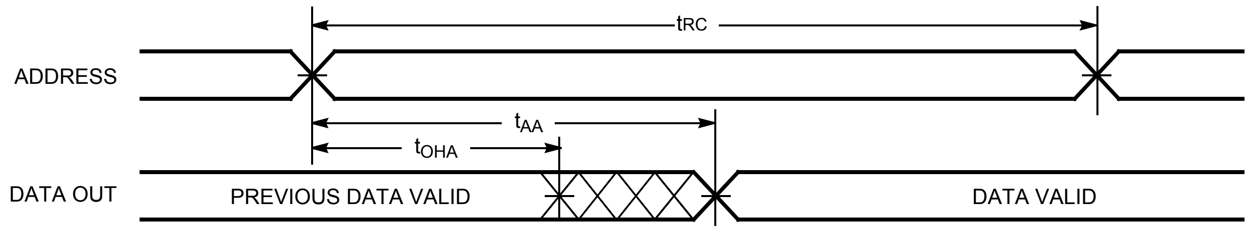
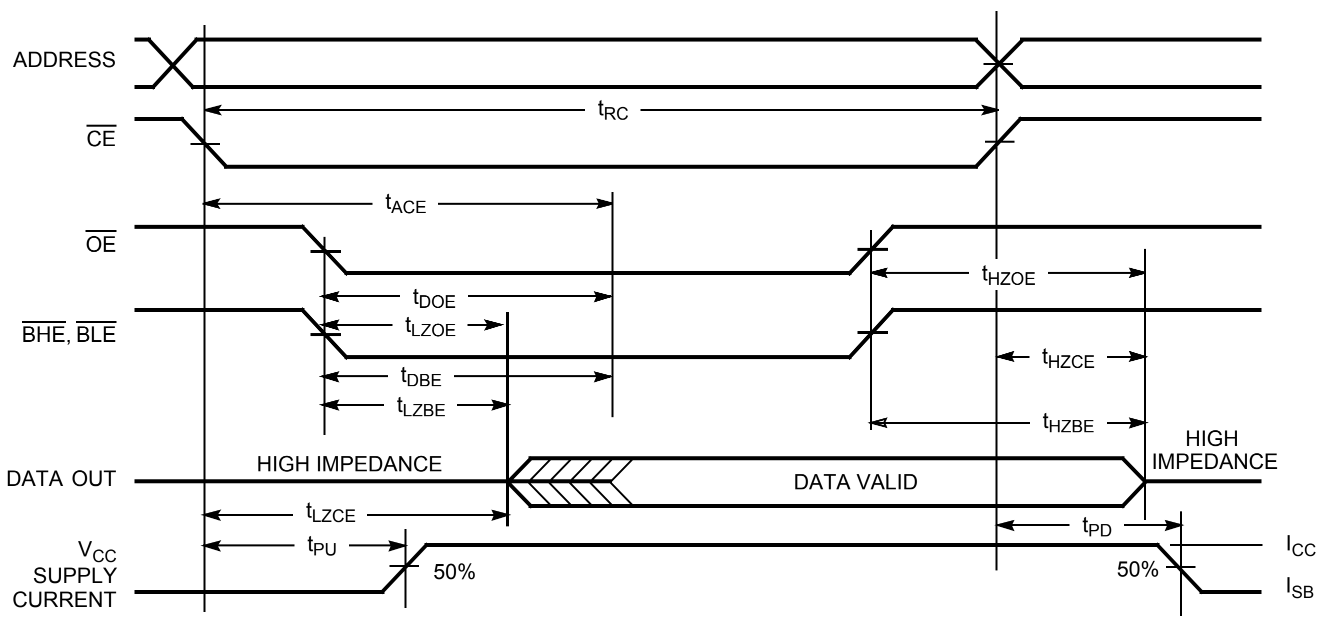


Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled) [12, 13]



Notes
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ($\overline{CE}$ Controlled) [14, 15]

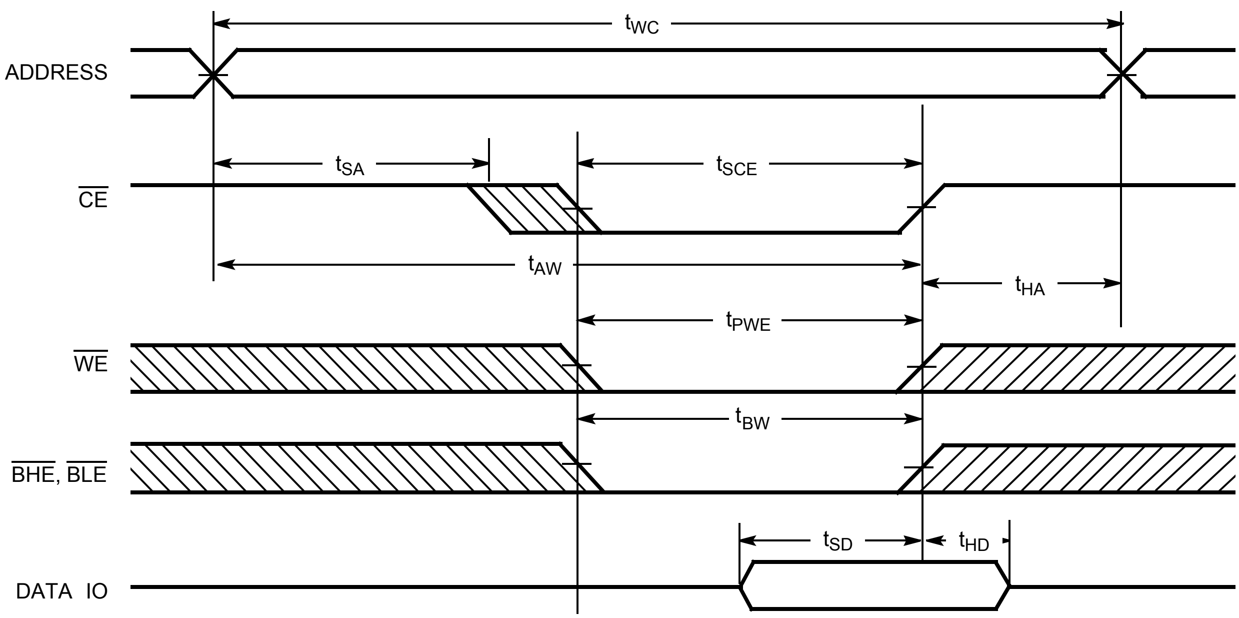
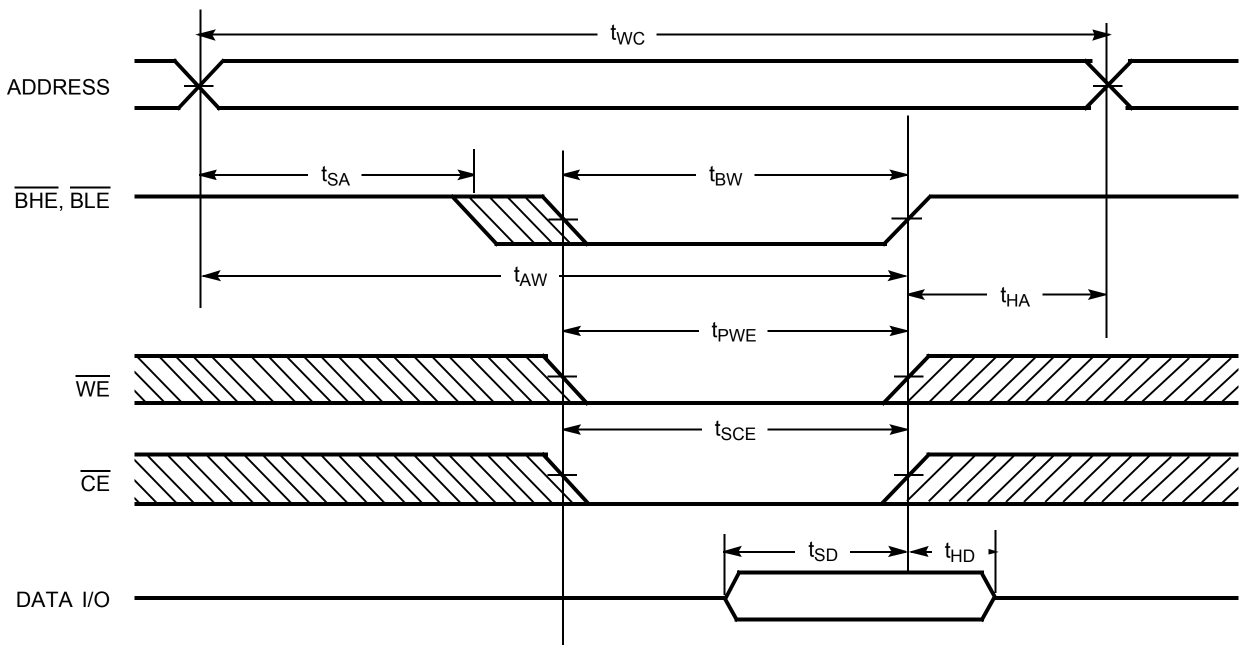


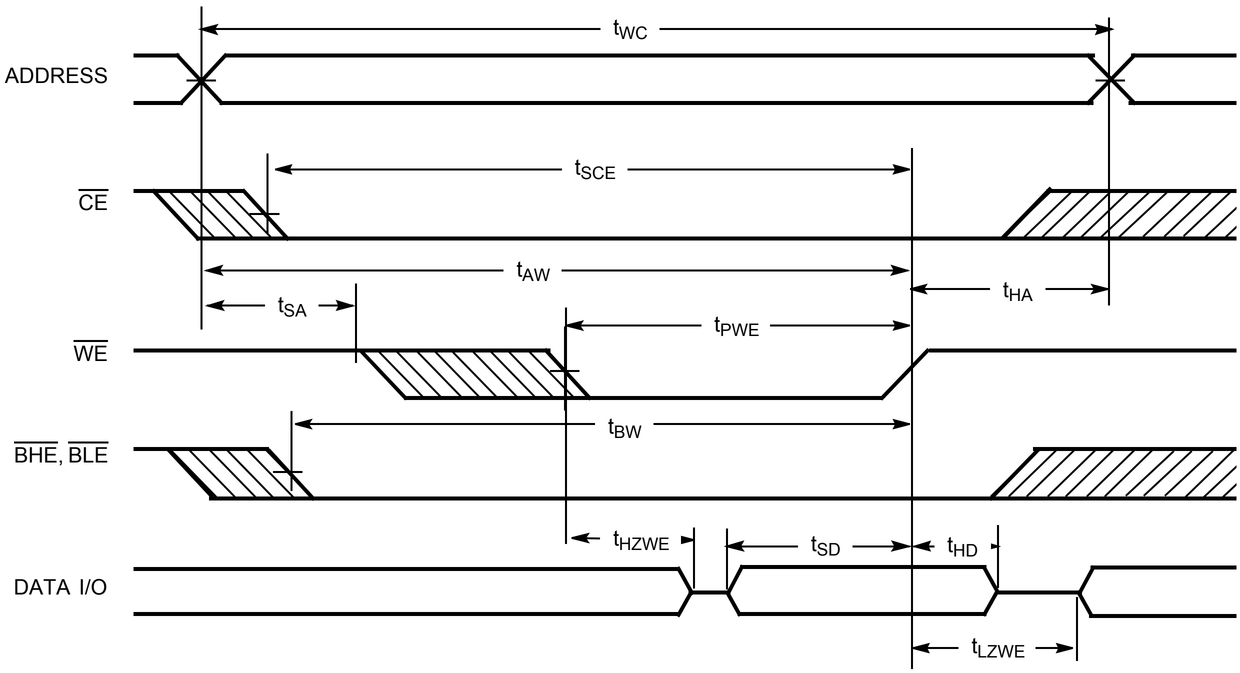
Figure 6. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes
14. Data I/O is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, LOW)



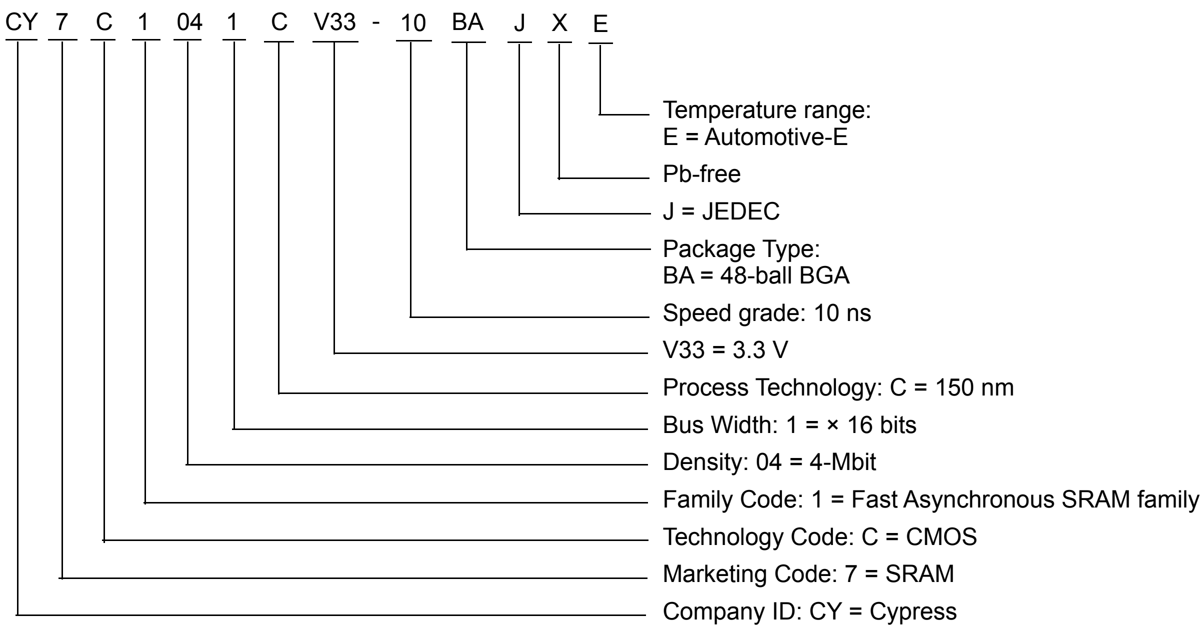
Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	X	X	X	X	High Z	High Z	Power down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – all bits	Active (I_{CC})
L	L	H	L	H	Data Out	High Z	Read – lower bits only	Active (I_{CC})
L	L	H	H	L	High Z	Data Out	Read – upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – all bits	Active (I_{CC})
L	X	L	L	H	Data In	High Z	Write – lower bits only	Active (I_{CC})
L	X	L	H	L	High Z	Data In	Write – upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I_{CC})

Ordering Information

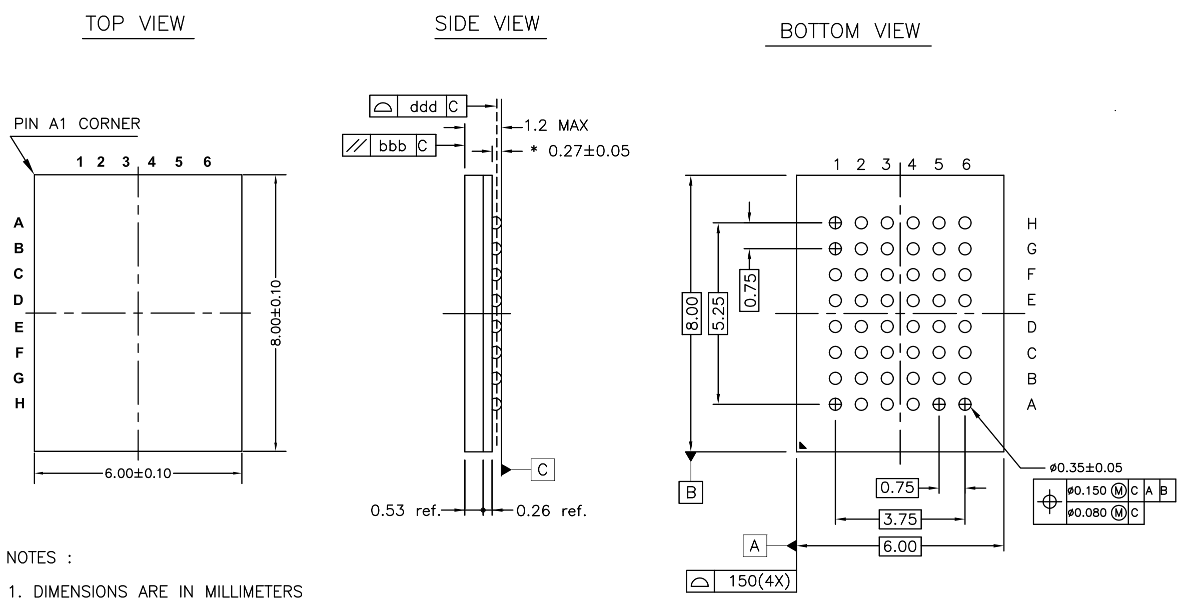
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1041CV33-10BAJXE	001-85259	48-ball BGA (Pb-free)	Automotive-E

Ordering Code Definitions



Package Diagrams

Figure 8. 48-ball FBGA (6 × 8 × 1.2 mm) BA48M/BK48M (0.35 mm Ball Diameter) Package Outline, 001-85259



NOTES :

1. DIMENSIONS ARE IN MILLIMETERS
2. REFERENCE JEDEC STD : MO–216
3. * 0.32±0.05 FOR RAMTRON DEVICES

001-85259 *A

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
mW	milliwatt
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Revision	ECN	Orig. of Change	Submission Date	Description of Change
Document Title: CY7C1041CV33 Automotive, 4-Mbit (256 K × 16) Static RAM **Document Number: 001-86495**				
**	3925192	TAVA	04/04/2013	New data sheet.
*A	4103029	MEMJ	08/23/2013	Changed status from Preliminary to Final. Updated Ordering Information: No change in part numbers. Replaced "51-85087" with "001-85259" in "Package Diagram" column. Updated Package Diagrams: spec 001-85259 – Changed revision from ** to *A. Updated in new template.
*B	4396000	VINI	06/02/2014	No technical updates. Completing Sunset Review.
*C	4724503	PSR	04/14/2015	Updated Functional Description: Added "For a complete list of related resources, click here." at the end. Updated to new template. Completing Sunset Review.
*D	6003585	AESATP12	12/22/2017	Updated logo and copyright.

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