PWM Buck Regulator, Synchronous, Voltage Mode, High Performance, 65 V, 8 A

FAN65005A

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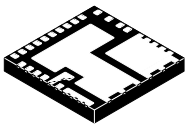
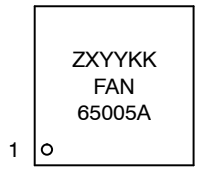


PQFN35 6x6
CASE 483BE

MARKING DIAGRAM



Z = Assembly Location
X = Year / Lead Free
YY = Week
KK = Lot
FAN65005A = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 23 of this data sheet.

Description

FAN65005A is a wide VIN highly efficient synchronous buck regulator, with integrated high side and low side power MOSFETs. The device incorporates a fixed frequency voltage mode PWM controller supporting a wide voltage range from 4.5 V to 65 V and can handle continuous currents up to 8 A.

FAN65005A includes a 0.67% accurate reference voltage to achieve tight regulation. The switching frequency can be programmed from 100 kHz to 1 MHz. To improve efficiency at light load condition, the device can be set to discontinuous conduction mode with pulse skipping operation.

FAN65005A has dual LDOs to minimize power loss and integrated current sense circuit that provides cycle−by−cycle current limiting. This single phase buck regulator offers complete protection features including Over current protection, Thermal shutdown, Under−voltage lockout, Over voltage protection, Under voltage protection and Short −circuit protection.

FAN65005A uses ON Semiconductor's high performance PowerTrench® MOSFETs that reduces ringing in switching applications. FAN65005A integrates the controller, driver, and power MOSFETs into a thermally enhanced, compact 6 x 6 mm PQFN package. With an integrated approach, the complete DC/DC converter is optimized from the controller and driver to MOSFET switching performance, delivering a high power density solution.

Features

- Wide Input Voltage Range: 4.5 V to 65 V
- Continuous Output Current: 8 A
- Fixed Frequency Voltage Mode PWM Control with Input Voltage Feed−forward
- 0.6 V Reference Voltage with 0.67% Accuracy
- Adjustable Switching Frequency: 100 kHz to 1 MHz
- Dual LDOs for Single Supply Operation and to Reduce Power Loss
- Selectable CCM PWM Mode or PFM Mode for Light Loads
- External Compensation for Wide Operation Range
- Adjustable Soft−Start & Pre−Bias Startup
- Enable Function with Adjustable Input Voltage Under−Voltage−Lock−Out (UVLO)
- Power Good Indicator
- Over Current Protection, Thermal Shutdown, Over Voltage Protection, Under Voltage Protection and Short−circuit Protection
- High Performance Low Profile 6 mm x 6 mm PQFN Package
- This Device is Pb−Free and RoHS Compliant

Applications

- High Voltage POL Module
- Telecommunications: Base Station Power Supplies
- Networking: Computing, Battery Management Systems, USB−PD
- Industrial Equipment: Automation, Power Tools, Slot Machines

TYPICAL APPLICATION

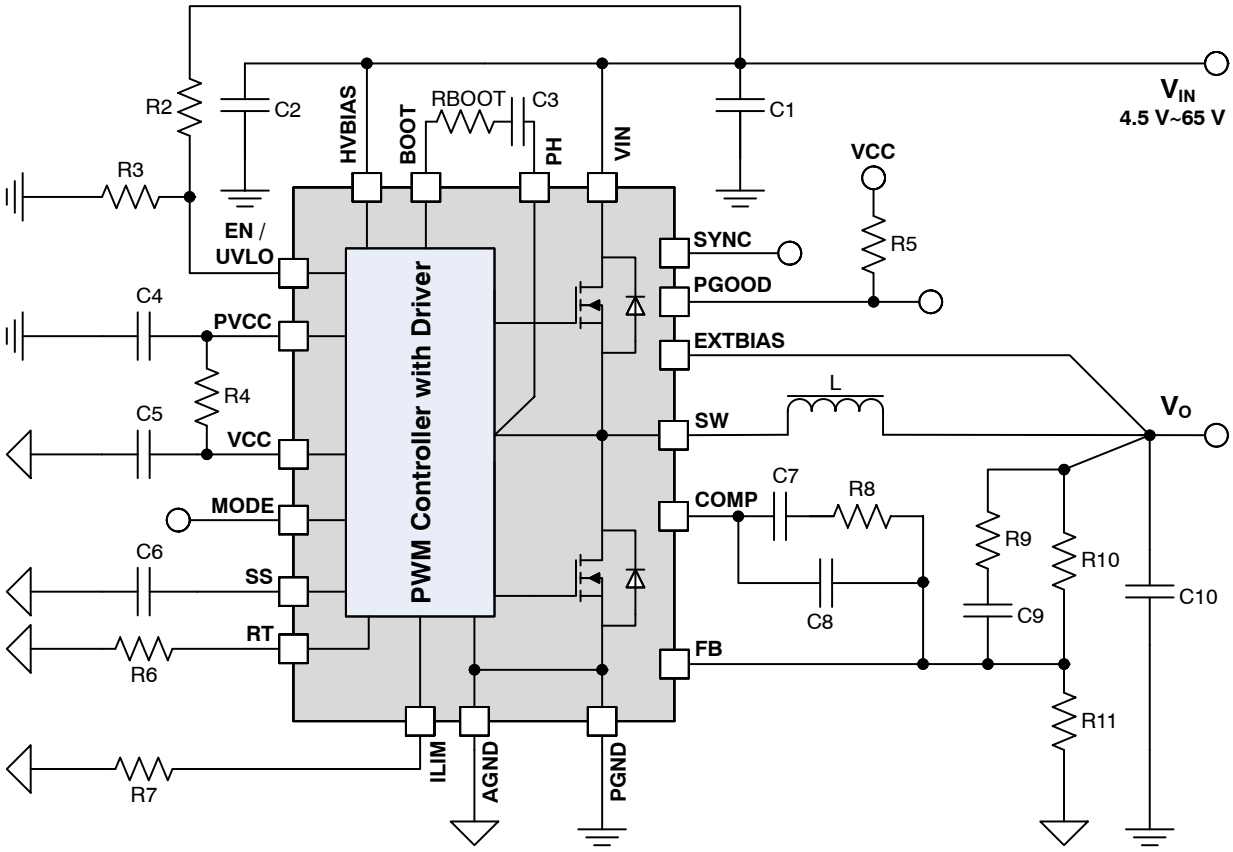


Figure 1. Typical Application

Table 1. APPLICATION DESIGN EXAMPLE

V_{IN} (V)	V_O (V)	L (µH)	L to be used (µH)	C_O from V_{O_RIPPLE} (µF)	C_O from V_{OS} (µF)	C_O from V_{US} (µF)	C_O to be used	R10 (Ω)	R11 (Ω)	R9 (Ω)	R8 (Ω)	C9 (F)	C7 (F)	C8 (F)	f_{CO} (Hz)	Phase margin (°)	RT (=R6) (Ω)
35	24	16.762		2.6	30.9	65.2			718.2						18.0k	69.4	
35	28	12.444		2.2	22.7	83.5			613.4						22.6k	67.5	
35	30	9.524		2.1	19.8	103.6			571.6						22.6k	67.5	
48	24	26.667		2.6	30.9	30.9			718.2								
48	28	25.926	22.00	2.2	22.7	31.4	75.2	28010	613.4	365	1.0k	2.7n	220n	470p			3.75E+04
48	30	25.000		2.1	19.8	32.3			571.6								
60	24	32.000		2.6	30.9	20.8			718.2								
60	28	33.185		2.2	22.7	19.9			613.4								
60	30	33.333		2.1	19.8	19.8			571.6								

NOTE: *Iout = 5 A, Fsw = 300 KHz

BLOCK DIAGRAM

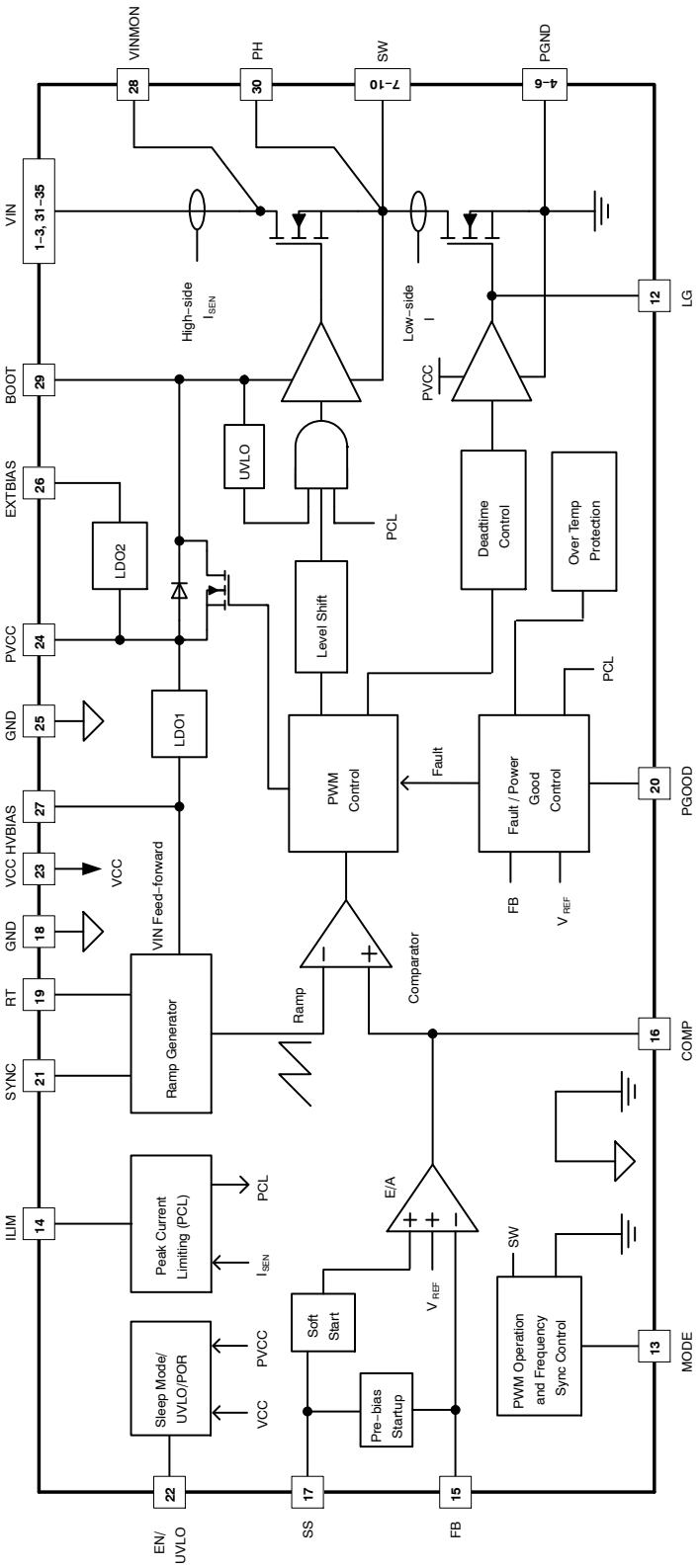


Figure 2. Block Diagram

PIN CONFIGURATION

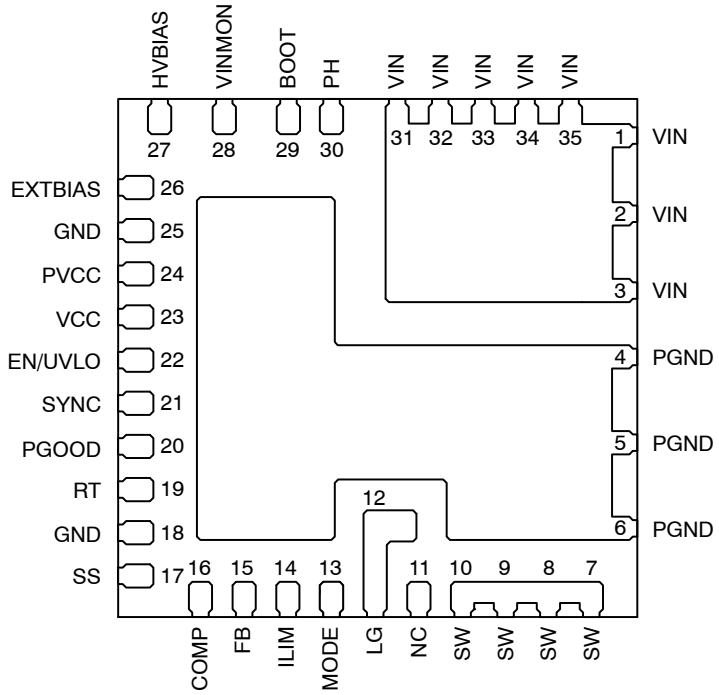


Figure 3. Pin Assignment (Bottom View)

Table 2. PIN DESCRIPTION

Name	Pin/Pad	Description
VIN	1–3, 31–35, VIN Pad	Input voltage to power stage
PGND	4–6, PGND Pad	Power ground for power stage and PVCC
SW	7–10	Switching node, junction of high- and low-side MOSFETs
NC	11	No Connection
LG	12	Gate of low side MOSFET
MODE	13	Configures pulse modulation/frequency synchronization modes. See MODE description for details
ILIM	14	Connect a resistor to GND to set the high-side MOSFET peak current limit
FB	15	Feedback Voltage Input
COMP	16	Output of internal error amplifier for external compensation
SS	17	Set up soft-start time. Connect a capacitor between SS and PGND to set the soft start time
GND	18, 25	Analog ground for VCC, RT, SYNC, MODE, etc.
RT	19	Connect a resistor to GND to set switching frequency
PGOOD	20	Power good indicator, open-drain output. Level HIGH indicates V_{OUT} is within set limits
SYNC	21	The pin is used to synchronize frequency in when in Non-Master mode or out when in master mode
EN/UVLO	22	Enable/VIN Under-Voltage-Lockout set pin. When used as enable function in-dependent of input voltage, connect this pin to a voltage > 1.22 V to enable or PGND to disable. When used as enable function at specific input voltage level, connect a resistor divider between input voltage and PGND to this pin
VCC	23	Bias power for internal analog circuits
PVCC	24	LDO output and the bias supply for gate driver circuit
EXTBIAS	26	Input voltage to the secondary LDO. Typically connect to V_O when $V_O \geq 5$ V
HVBIAS	27	Input voltage to the primary LDO. Also used for the feed-forward function. Connect it to power stage input with a small RC filter
VINMON	28	Current sense positive pin. Do NOT connect anything
BOOT	29	Bootstrap supply for high-side driver. Connect a low impedance capacitor between this pin and PH pin
PH	30	High-side source connection (SW node) for the bootstrap capacitor

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{IN}	VIN Pin Voltage (System Supply) with regard to PGND	−0.3	70	V
V_{HVBIAS}	HVBIAS Pin Voltage with regard to PGND	−0.3	70	
$V_{EXTBIAS}$	EXTBIAS Pin Voltage with regard to PGND	−0.3	70	
$V_{EN/UVLO}$	EN/UVLO Pin Voltage with regard to PGND	−0.3	8.4	
V_{PH}	PH Pin Voltage with regard to PGND	−0.3	70	
V_{SW}	SW Pin Voltage with regard to PGND	−0.3	70	
	SW Pin Voltage with regard to PGND (Pulse, 100 ns)	−5.0	75	
	SW Pin Voltage with regard to PGND (Pulse, 30 ns)	−7.5	75	
V_{BOOT}	BOOT Pin Voltage with regard to PGND	−0.3	75	
	BOOT Pin Voltage with regard to PH Pin	−0.3	6.5	
V_{ILIM}	ILIM Pin Voltage with regard to GND	−0.3	6.5	
V_{PVCC}	PVCC Pin Voltage with regard to PGND	−0.3	6.5	
V_{FB}	FB Pin Voltage with regard to GND	−0.3	V_{CC} + 0.3	
V_{COMP}	COMP Pin Voltage with regard to GND	−0.3	V_{CC} + 0.3	
V_{PGOOD}	PGOOD Pin Voltage with regard to GND	−0.3	V_{CC} + 0.3	
V_{LG}	LG Pin Voltage with regard to PGND	−0.3	V_{PVCC} + 0.3	
V_{MODE}	MODE Pin Voltage with regard to GND	−0.3	V_{CC} + 0.3	
V_{RT}	RT Pin Voltage with regard to GND	−0.3	V_{CC} + 0.3	
V_{SS}	SS Pin Voltage with regard to PGND	−0.3	V_{CC} + 0.3	
V_{SYNC}	SYNC Pin Voltage with regard to GND	−0.3	V_{CC} + 0.3	
V_{GND}	GND Pin Voltage with regard to PGND	−0.3	0.3	
ESD	Human Body Model, ANSI/ESDA/JEDEC JS−001−2012	−	1000	
	Charged Device Model, JESD22−C101	−	500	
T_{JN} (Note 1)	Thermal Calculation	−	$T_{jn} = k_{j1} \bullet Q_{LS} + k_{j2} \bullet Q_{Controller} + k_{j3} \bullet Q_{HS} + k_{Lead5} \bullet T_{Lead5} + k_{Lead25} \bullet T_{Lead25} + k_{Lead32} \bullet T_{Lead32} + k_{amb} \bullet T_a$	°C
T_J	Junction Operating Temperature	−55	150	°C
T_{STG}	Device Storage Temperature	−55	150	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Units, temperatures must be in degrees Celsius, power values (Q) must be in watts. Measured on 2s2p board, 80 x 80 mm^2 with 546 mm^2 top layer spreader. Use coefficients as per below table:

FAN65005A	k_{j1}	k_{j2}	k_{j3}	k_{Lead5}	k_{Lead25}	k_{Lead32}	k_{amb}
2s2p board, 80 mm x 80 mm with 546 mm^2 top layer spreader							
LS coefficients	6.8	4.1	2.4	0.46	0.09	0.21	0.24
LDO coefficients	4.0	45.8	1.9	0.26	0.29	0.17	0.28
HS coefficients	2.8	2.0	6.4	0.19	0.05	0.54	0.22

Table 4. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	VIN Pin Voltage (System Supply) with regard to PGND	4.5	–	65	V
V_{HVBIAS}	HVBIAS Pin Voltage with regard to PGND	4.5	–	65	
V_{SW}	SW Pin Voltage with regard to PGND (DC)	−0.3	–	V_{IN}	
$V_{EXTBIAS}$	EXTBIAS Pin Voltage with regard to PGND	4.5	–	65	
$V_{EN/UVLO}$	EN/UVLO Pin Voltage with regard to PGND	–	–	7.5	
V_{PG_SPLY}	PGOOD Pin Voltage with regard to GND	–	–	5.4	
T_A	Operating Ambient Temperature	−40	–	125	°C
T_J	Junction Operating Temperature	−40	–	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS

(Typical application circuit shown in Figure 1 is used. Unless otherwise noted, $V_{IN} = V_{HVBIAS} = 48$ V, $V_{OUT} = 5$ V, $V_{PVCC} = V_{CC} = 5$ V, $-40°C < T_J = T_A < +125°C$. $T_A = T_J = +25°C$ for typical values)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY						
$I_{HVBIAS\_Q\_PWM}$	Forced CCM Quiescent Current	V_{EN} = 2.0 V, MODE = 5 V through a 100 kΩ resistor, V_{FB} = 0.64 V	–	1.2	–	mA
$I_{HVBIAS\_Q\_PSM}$	DCM with Pulse Skipping Quiescent Current	V_{EN} = 2.0 V, MODE = 0 V through a 100 kΩ resistor, V_{FB} = 0.64 V	–	1.4	–	
I_{HVBIAS_SDN}	Shutdown Current	V_{EN} = 0 V	–	5	9	μA
V_{HVBIAS_TH}	HVBIAS UVLO Threshold	HVBIAS Rising	–	3.92	–	V
V_{HVBIAS_HYS}	HVBIAS UVLO Hysteresis	HVBIAS Falling	–	1.0	–	
LDOs						
V_{PVCC}	LDO Output Voltage	I_{PVCC} = 1 mA and EXTBIAS pin is open	4.75	5.00	5.25	V
		$V_{EXTBIAS}$ = 12 V, I_{PVCC} = 1 mA	4.75	5.00	5.25	
V_{HVBIAS_D}	LDO1 Dropout Voltage	V_{HVBIAS} = 5.0 V, LDO Output Current = 150 mA	–	1.0	2.0	
$V_{EXTBIAS\_D}$	LDO2 Dropout Voltage	$V_{EXTBIAS}$ = 5.0 V, LDO Output Current = 150 mA	–	0.33	0.66	
V_{LDOSWO}	Switchover Voltage above which LDO1 is Disabled and LDO2 is Enabled	$V_{EXTBIAS}$ is rising	–	4.7	–	
V_{LDOSWO_HYS}	Switchover Voltage Hysteresis	$V_{EXTBIAS}$ is falling	–	100	–	mV
$V_{SWTOLDO}$	Threshold Voltage above which the LDO is in LDO mode	V_{HVBIAS} or $V_{EXTBIAS}$ is rising	–	5.5	–	V
$V_{LDOTOSW}$	Threshold Voltage below which the LDO is in switch mode	V_{HVBIAS} or $V_{EXTBIAS}$ is falling	–	5.4	–	
VCC SUPPLY						
V_{CC_ON}	V_{CC} Start Voltage	V_{CC} Rising	3.8	4.0	4.4	V
V_{CC_UVLO}	V_{CC} UVLO Threshold	V_{CC} Falling	3.6	3.8	4.1	
$V_{CC\_UVLO\_HYS}$	V_{CC} UVLO Hysteresis		–	0.2	–	

Table 5. ELECTRICAL CHARACTERISTICS (continued)
(Typical application circuit shown in Figure 1 is used. Unless otherwise noted, $V_{IN} = V_{HVBIAS} = 48$ V, $V_{OUT} = 5$ V, $V_{PVCC} = V_{CC} = 5$ V, $-40°C < T_J = T_A < +125°C$. $T_A = T_J = +25°C$ for typical values)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage	$T_J = 25°C$, $V_{IN} = 4.5$ V to 65 V	0.596	0.600	0.604	V
		$T_J = -40°C$ to $125°C$ (Note 2)	0.594	–	0.606	
ENABLE AND UNDER VOLTAGE LOCK OUT						
V_{EN_TH}	EN/UVLO Threshold	EN/UVLO Rising	1.141	1.22	1.296	V
V_{EN_HYS}	EN/UVLO Hysteresis	EN/UVLO Falling	–	115	–	mV
R_{EN_PD}	EN/UVLO Internal Pull down Resistance		–	500	–	kΩ
V_{EN_CLP}	EN/UVLO Clamp Voltage	TBD	–	2.5	–	V
R_{EN_CLP}	EN/UVLO Clamp Resistance		–	200	–	kΩ
I_{EN_CLP}	EN/UVLO Clamp Current	$V_{EN} = 2.5$ V	–	22	–	μA
MODE						
R_{MASTER}	Resistor Connected to Mode Pin for Master Synchronization Mode		70	100	130	kΩ
R_{NON_MASTER}	Resistor Connected to Mode Pin for Non-Master Synchronization Mode		1	–	5	kΩ
OSCILLATOR						
f_{SW}	Frequency Range		100	–	1000	kHz
f_{SW1}	Switching Frequency Set by RT	$R_T = 199$ kΩ	85	100	125	
f_{SW2}		$R_T = 8.0$ kΩ	900	1000	1200	
f_{SW3}		RT Pin is Short-Circuited to VCC Pin	215	250	280	
f_{SW4}		RT Pin is Short-Circuited to GND Pin	425	500	575	
FREQUENCY SYNCHRONIZATION						
$V_{SYNC\_IN\_H}$	SYNC Input Logic HIGH		2	–	–	V
$V_{SYNC\_IN\_L}$	SYNC Input Logic LOW		–	–	0.8	
$t_{HIGH\_IN\_MIN}$	Input HIGH Level Pulse Width		150	–	–	ns
$t_{LOW\_IN\_MIN}$	Input LOW Level Pulse Width		150	–	–	
f_{SYNC}	Synchronizable Frequency	Percentage of frequency set by RT	70	–	130	%
$t_{RT\_SYNC\_DL}$	Transition Delay from RT Set Frequency to Sync Frequency	In Number of External Clock Cycles in 2 ms time period	–	64	–	Cycles
R_{SYNC_PD}	SYNC Pin Pull down Resistance		–	100	–	kΩ
$R_{SYNC\_DR\_PU}$	SYNC output Driver Pull-up Resistance		–	10	–	Ω
$R_{SYNC\_DR\_PD}$	SYNC output Driver Pull-down Resistance		–	13	–	
D_{SYNC_OUT}	SYNC Output Frequency Duty Cycle		–	50	–	%
C_{L_SYNC}	SYNC Pin Lead Capacitance		–	–	200	pF

Table 5. ELECTRICAL CHARACTERISTICS (continued)
(Typical application circuit shown in Figure 1 is used. Unless otherwise noted, $V_{IN} = V_{HVBIAS} = 48$ V, $V_{OUT} = 5$ V, $V_{PVCC} = V_{CC} = 5$ V, $-40°C < T_J = T_A < +125°C$. $T_A = T_J = +25°C$ for typical values)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RAMP AND PWM MODULATOR						
k_{PWM}	PWM Modulator Gain, $V_{IN}/\Delta V_{RAMP}$	$V_{IN} = V_{HVBIAS} = 4.5$ to 65 V	–	25	–	V/V
T_{ON_MIN}	PWM Minimum ON time		–	150	200	ns
T_{OFF_MIN}	PWM Minimum OFF time		–	150	200	
ERROR AMPLIFIER						
GBW	Unit Gain Bandwidth		–	10	–	MHz
G	DC Gain		–	80	–	dB
I_{FB}	FB Bias Current	$V_{FB} = 0.6$ V	–50	5	50	nA
I_{COMP_SOURCE}	COMP Source Current		2	7	–	mA
I_{COMP_SINK}	COMP Sink Current		2	8.5	–	mA
SOFT START						
t_{SS_DL}	Enable High to Soft Start Ramp Start Delay		–	1	3	ms
I_{SS}	Charging Current to SS Capacitor		4.3	5	5.9	μA
BOOT						
V_{BT_SWITCH}	Bootstrap Switch Voltage Drop	BOOT Current, $I_{BOOT} = 50$ mA	–	0.1	–	V
$V_{BT\_UVLO\_TH}$	BOOT UVLO Voltage with regard to PH	BOOT Falling	–	3.20	–	
$V_{BT\_UVLO\_HYS}$	BOOT UVLO Hysteresis with regard to PH	BOOT Rising	–	0.35	–	
CURRENT PROTECTION						
I_{LIM_S}	Current Source Creating Current Limit Reference Voltage on R_ILIM		–	8.5	–	μA
k_{ILIM_HS}	High-side MOSFET current limit scale factor ($I_{LIM\_HS} = k_{ILIM\_HS} \times R_{ILIM}$)		–	59.5	–	μA/Ω
k_{ILIM_LS}	Low-side MOSFET current limit scale factor ($I_{LIM\_LS} = k_{ILIM\_LS} \times R_{ILIM}$)		–	19.6	–	
n_{CYCLE_OCP}	Number of Switching Cycle(s) before Entering Hiccup Mode	$I_{LIM\_HS} \le I_{SEN\_PEAK} < 130\%\ I_{LIM\_HS}$	–	1024	–	Cycle
n_{CYCLE_SCP}		$I_{SEN\_PEAK} \ge 130\% I_{LIM\_HS}$	–	1	–	
POWER GOOD						
$V_{FB\_NPG\_TH}$	FB Pin Voltage for PGOOD to Be De-asserted When Down from Regulation	FB Falling	88	92	96	$\%V_{REF}$
	FB Pin Voltage for PGOOD to Be De-asserted When up into OVP1	FB Rising	110	115	120	
$V_{FB\_PG\_TH}$	FB Pin Voltage for PGOOD to Be Asserted When Down from OVP1	FB Falling	–	110	–	
	FB Pin Voltage for PGOOD to Be Asserted When up into Regulation	FB Rising	–	94	–	

Table 5. ELECTRICAL CHARACTERISTICS (continued)
(Typical application circuit shown in Figure 1 is used. Unless otherwise noted, V_{IN} = V_{HVBIAS} = 48 V, V_{OUT} = 5 V, V_{PVCC} = V_{CC} = 5 V, −40°C < T_J = T_A < +125°C. T_A = T_J = +25°C for typical values)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
POWER GOOD						
t_{PG_DL}	PGOOD Delay	Time from when FB Reaches $V_{FB\_PG\_TH}$ to when PGOOD becomes HIGH	–	500	–	μs
t_{PG_FLT}	PGOOD De-glitch Filter Duration		–	5	–	μs
V_{PG_L}	PGOOD Output LOW Voltage	V_{FB} = 70%V_{REF}, I_{PGOOD} = −1 mA	–	6	10	mV
VOLTAGE PROTECTION						
V_{FB_OVP1}	FB Pin Voltage for Level 1 Over Voltage Detection	FB Voltage Rising	110	115	120	%V_{REF}
V_{FB_OVP2}	FB Pin Voltage for Level 2 Over Voltage Detection		124	130	136	
$V_{FB\_UVP\_TH}$	FB Pin Voltage for Under Voltage Detection	FB Voltage Falling	–	35	–	
HICCUP						
t_{HICCUP}	Hiccup Time		–	1	–	s
THERMAL SHUTDOWN						
T_{J_SD}	Thermal Shutdown Threshold	Temperature Rising	–	150	–	°C
$T_{J\_SD\_HYS}$	Thermal Shutdown Hysteresis	Temperature Falling	–	20	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
2. Guaranteed by design

TYPICAL PERFORMANCE CHARACTERISTICS

(Test at T_A = 25°C, V_{HVBIAS} = V_{IN} = 48 V and V_O = 5 V unless otherwise specified)

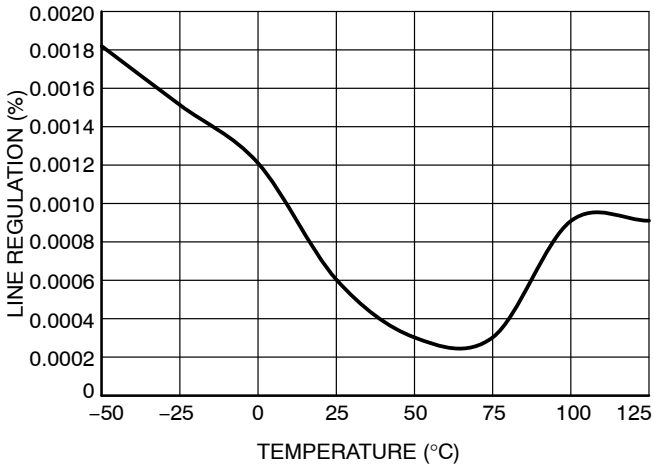


Figure 4. Line Regulation vs. Temperature

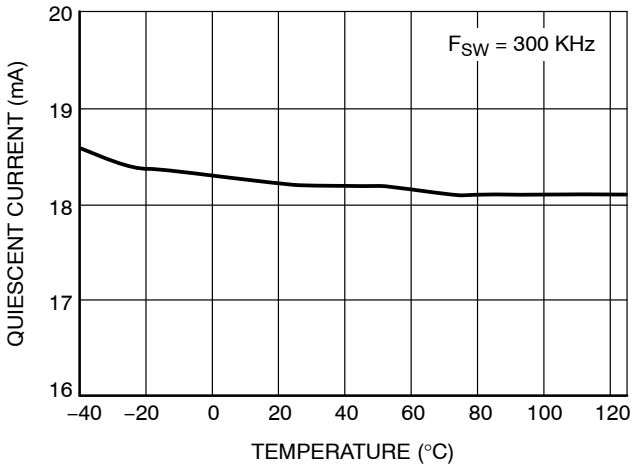


Figure 5. V_{IN} Quiescent Current vs. Temperature

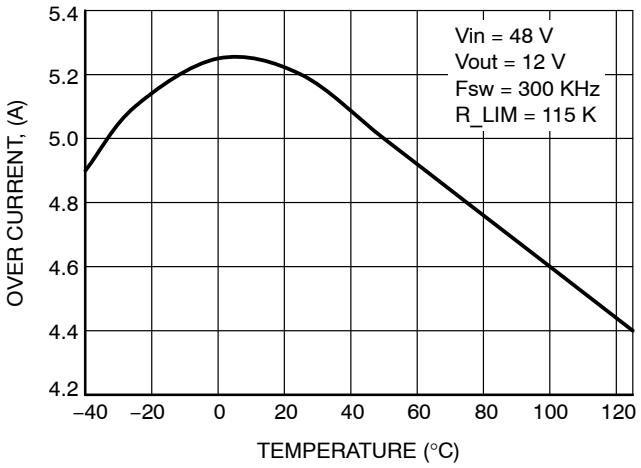


Figure 6. Over Current vs. Temperature

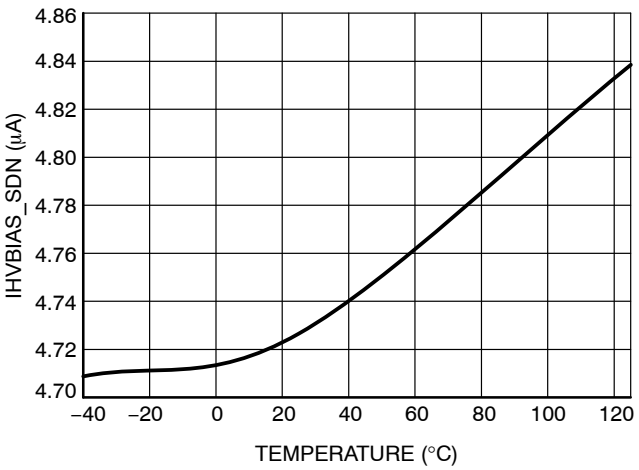


Figure 7. Shutdown Current vs. T at V_{HVBIA}S = 48 V

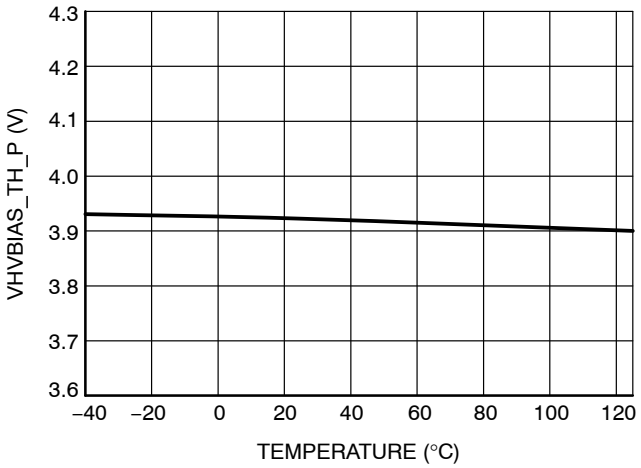


Figure 8. HVBIAS Rising Threshold vs. T

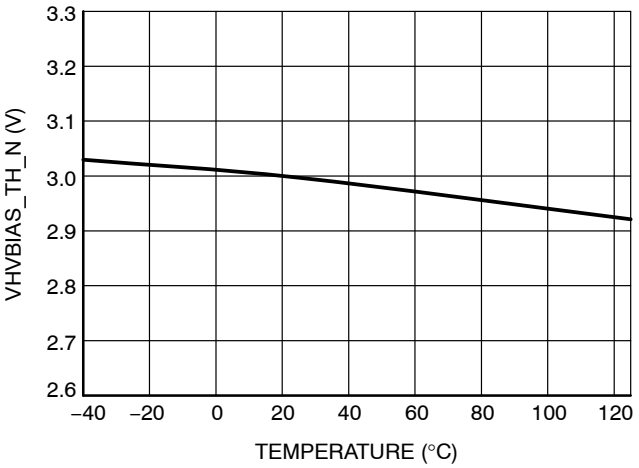


Figure 9. HVBIAS Falling Threshold vs. T

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

(Test at T_A = 25°C, V_{HVBIAS} = V_{IN} = 48 V and V_O = 5 V unless otherwise specified)

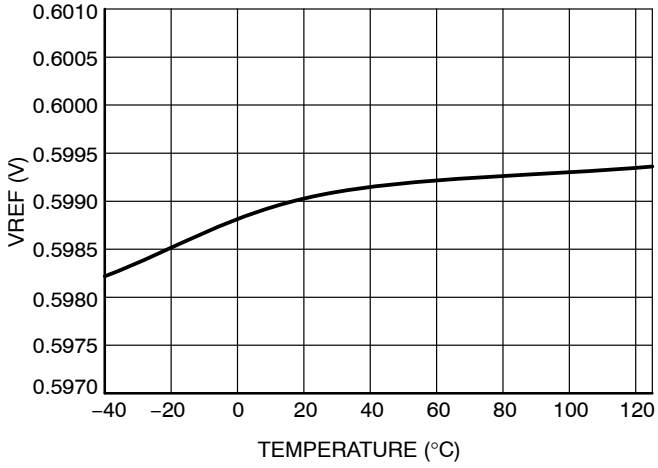


Figure 10. V_{REF} vs T at V_{HVBIAS} = 48 V

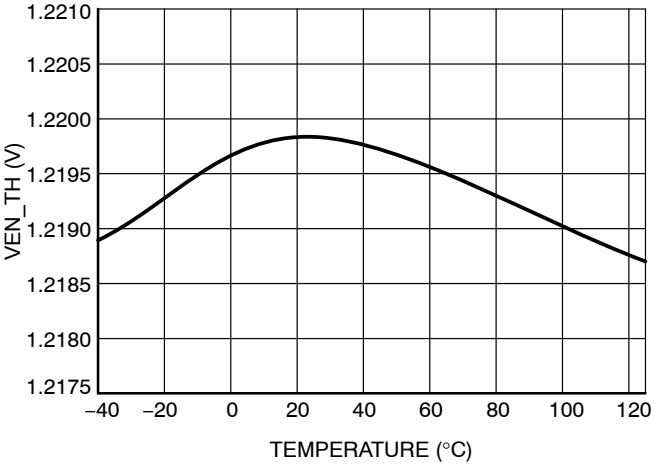


Figure 11. EN/UVLO Threshold Voltage vs. T at V_{HVBIAS} = 48 V

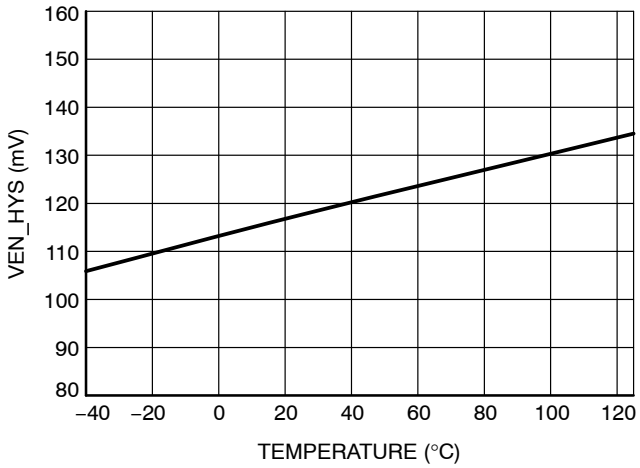


Figure 12. EN/UVLO Hysteresis Voltage vs. T at V_{HVBIAS} = 48 V

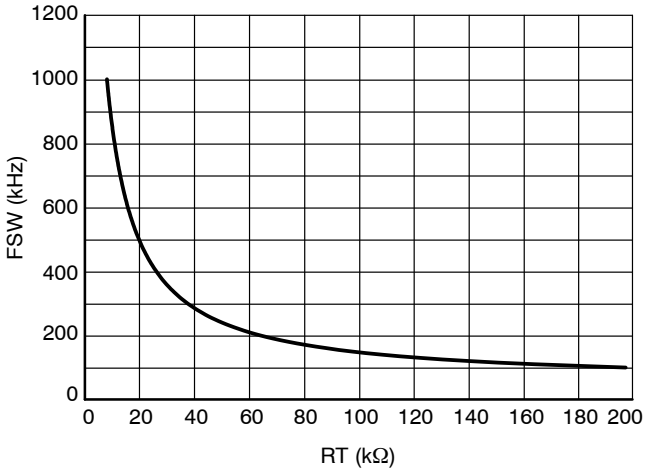


Figure 13. Switching Frequency vs. RT at V_{HVBIAS} = 48 V and T = 25°C

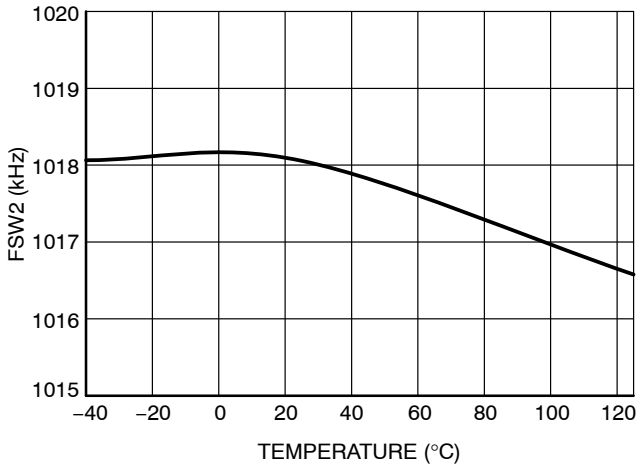


Figure 14. Switching Frequency vs. T at V_{HVBIAS} = 48 V and RT = 8.06 kΩ

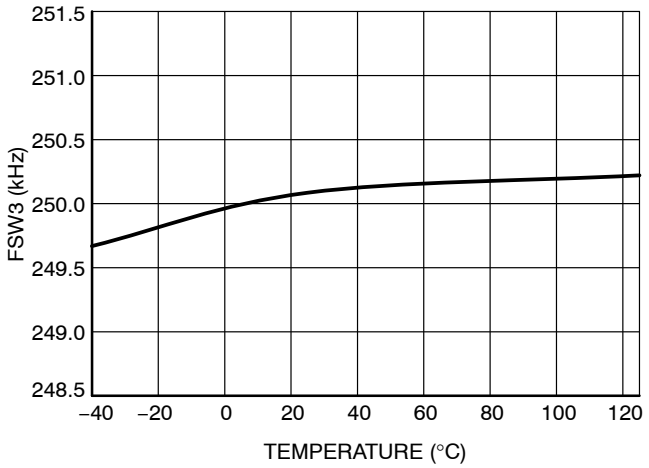


Figure 15. Switching Frequency vs. T at V_{HVBIAS} = 48 V and RT shorted to V_{CC}

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

(Test at T_A = 25°C, V_{HVBIAS} = V_{IN} = 48 V and V_O = 5 V unless otherwise specified)

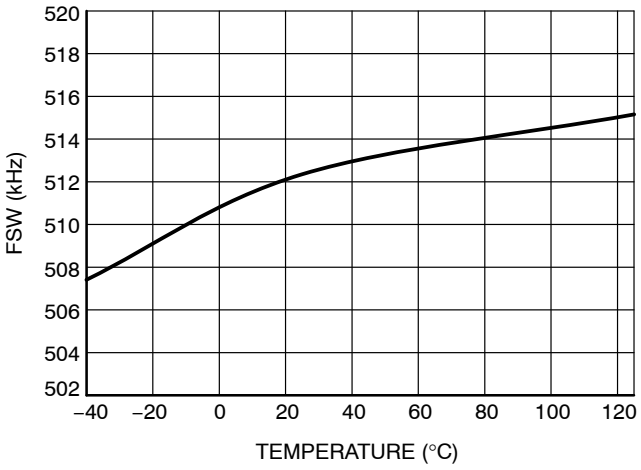


Figure 16. Switching Frequency vs. T at V_{HVBIAS} = 48 V and RT shorted to GND

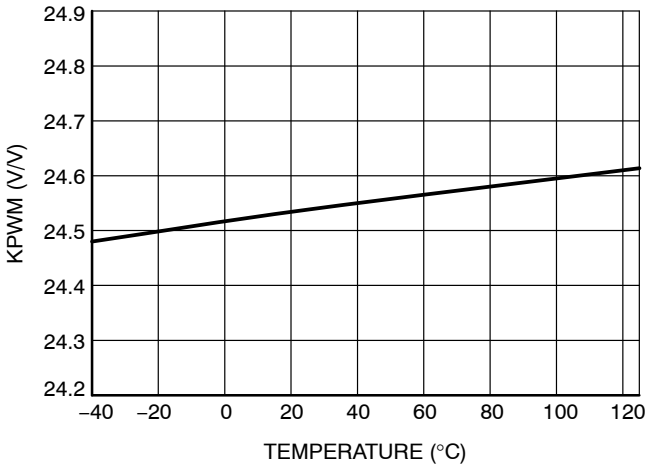


Figure 17. PWM Modulator Gain, V_{IN} / ΔV_{RAMP}, vs. T at V_{HVBIAS} = 48 V

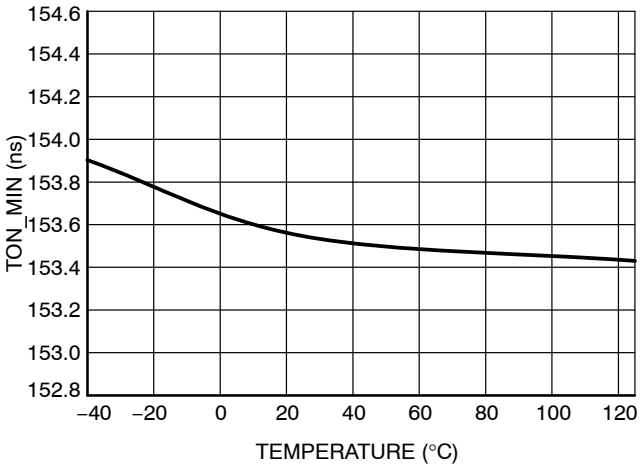


Figure 18. T_{ON_MIN} vs. T at V_{HVBIAS} = 48 V

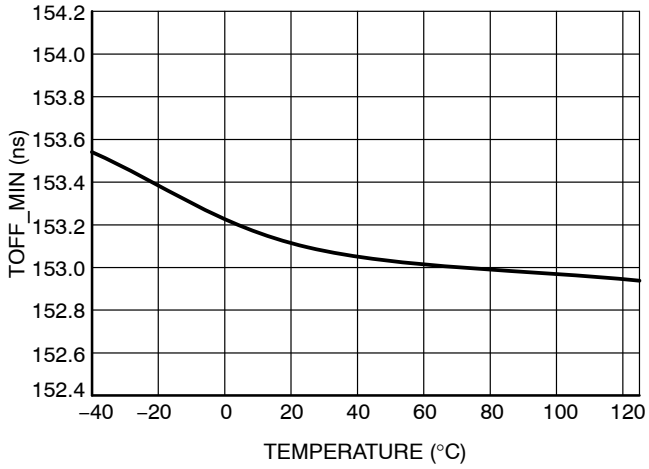


Figure 19. T_{OFF_MIN} vs. T at V_{HVBIAS} = 48 V

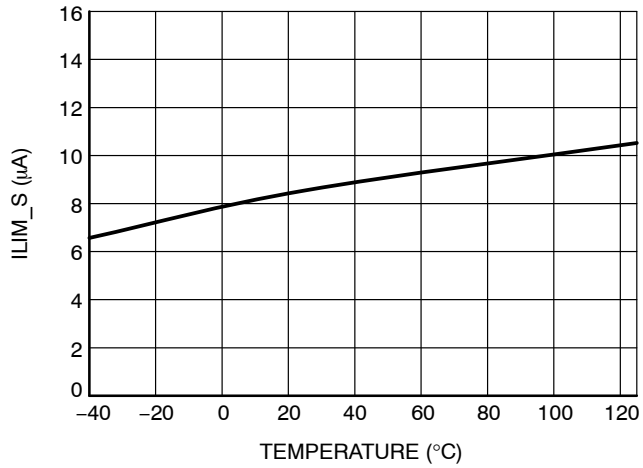


Figure 20. 8.5 μA Current Source for Current Limit Purpose vs. T at V_{HVBIAS} = 48 V

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

(Test at T_A = 25°C, V_{HVBIAS} = V_{IN} = 48 V and V_O = 5.0 V unless otherwise specified)

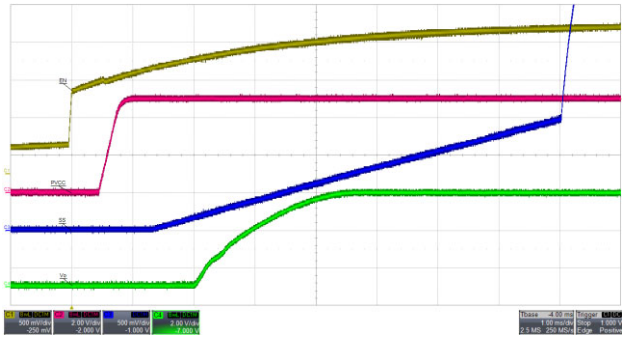


Figure 21. System Startup with No Load

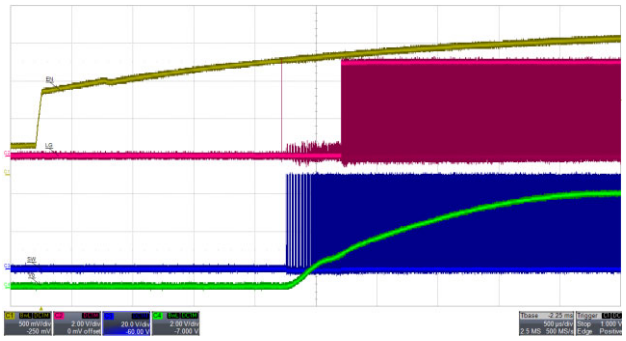


Figure 22. System Startup with No Load

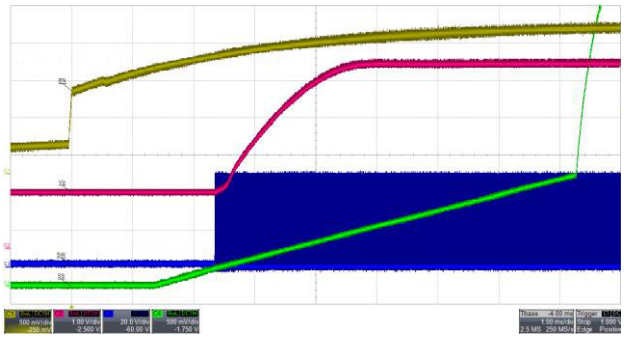


Figure 23. System Startup with 25% Pre-bias

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

(Test at T_A = 25°C, V_{HVBIAS} = V_{IN} = 48 V and V_O = 5.0 V unless otherwise specified)

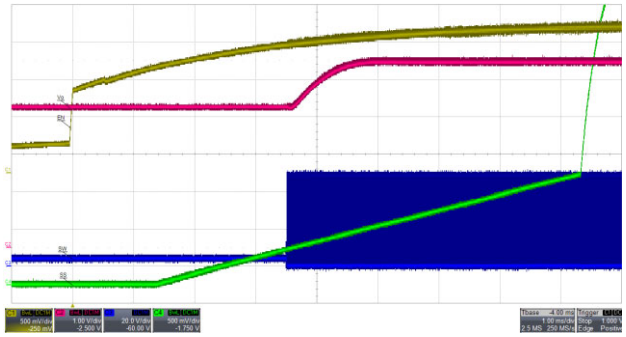


Figure 24. System Startup with 75% Pre-bias

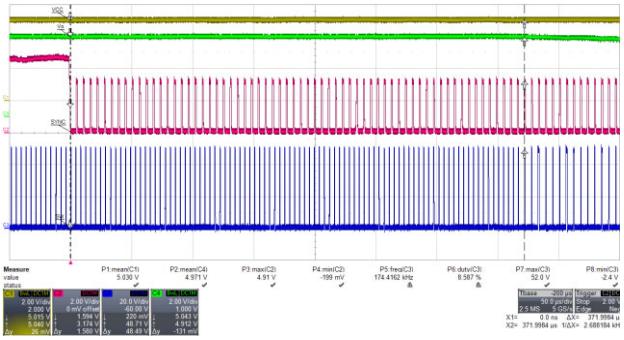


Figure 25. Show 64 Cycles of Transition Delay from RT Set Frequency to Sync Frequency

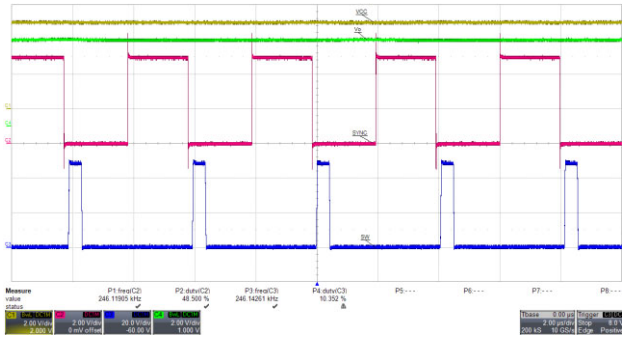


Figure 26. SYNC Output Frequency Duty Cycle in Master Mode

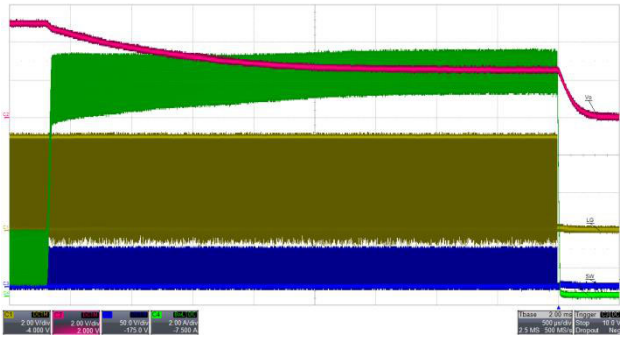


Figure 27. Over-current Protection with 250 kHz Switching Frequency

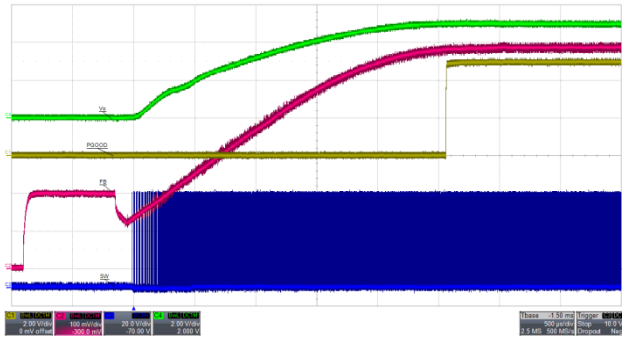


Figure 28. Power Good at Startup with No Load

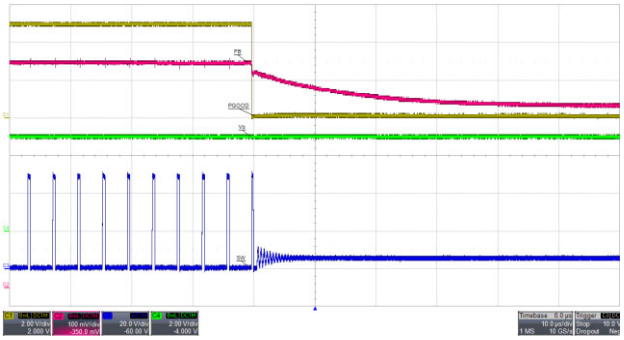


Figure 29. Power Good at Startup with No Load

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

(Test at T_A = 25°C, V_{HVBIAS} = V_{IN} = 48 V and V_O = 5.0 V unless otherwise specified)

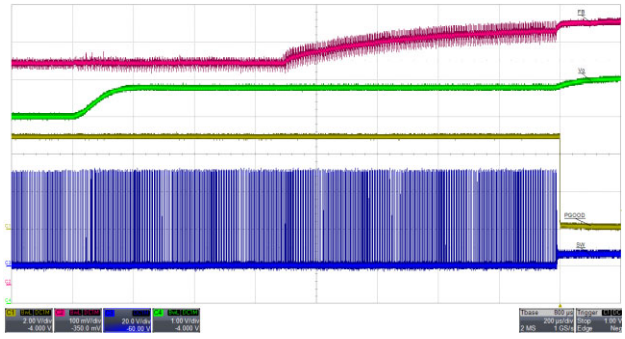


Figure 30. OVP1 at V_{FB} ≥ 115% V_{REF}

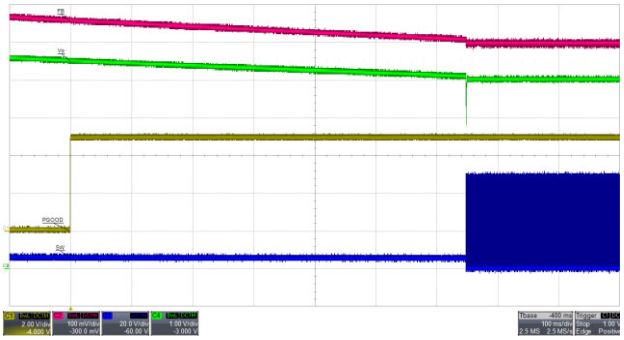


Figure 31. OVP1 Release at V_{FB} ≤ 110% V_{REF}

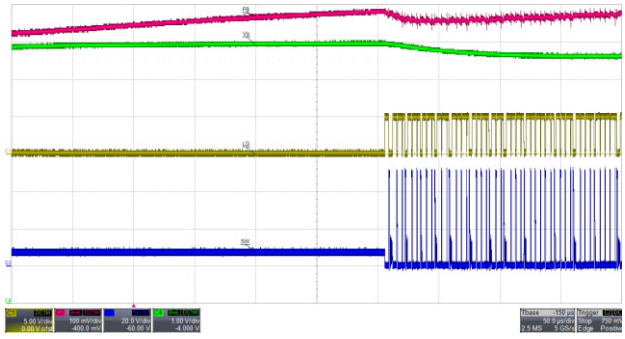


Figure 32. OVP2 at V_{FB} ≥ 130% V_{REF}

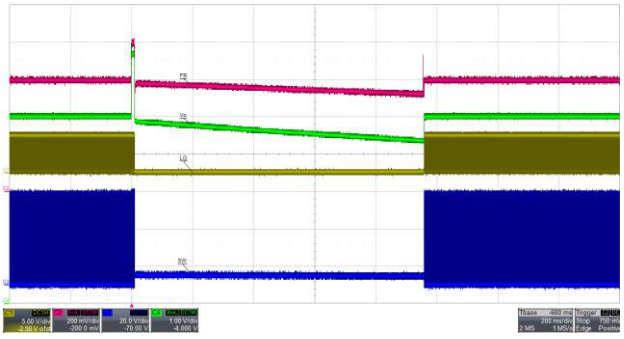


Figure 33. OVP2 Release at V_{FB} ≤ 100% V_{REF}

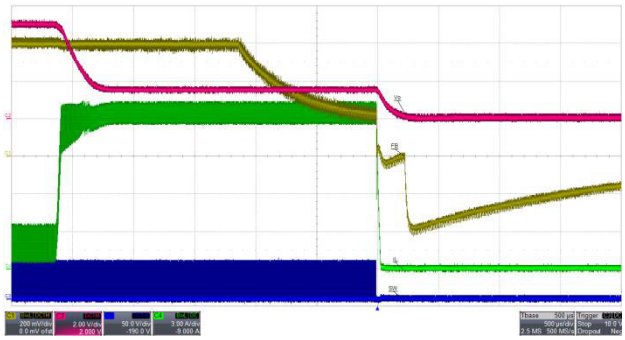


Figure 34. UVP due to Deep Over-current

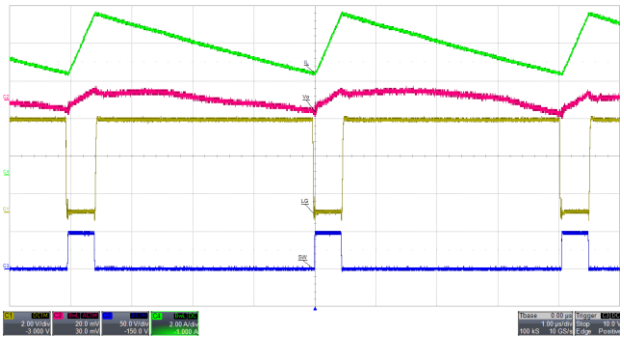


Figure 35. Switching and Voltage Ripple

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

(Test at T_A = 25°C, V_{HVBIAS} = V_{IN} = 48 V and V_O = 5.0 V unless otherwise specified)

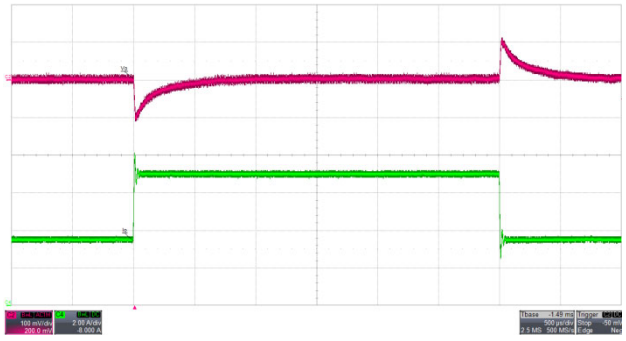


Figure 36. Load Step between 50% and 100% Load

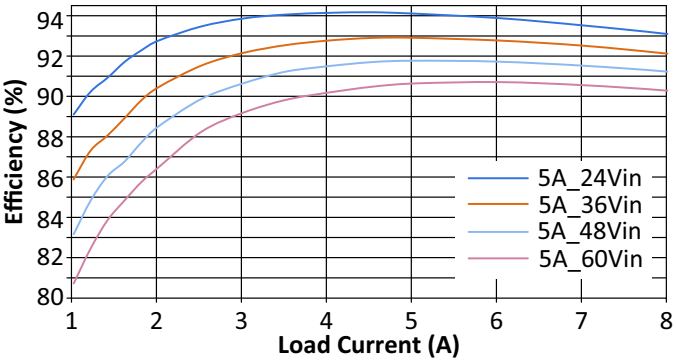


Figure 37. System Efficiency

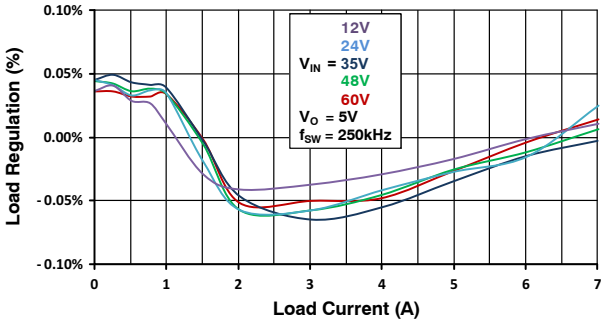


Figure 38. Load Regulation

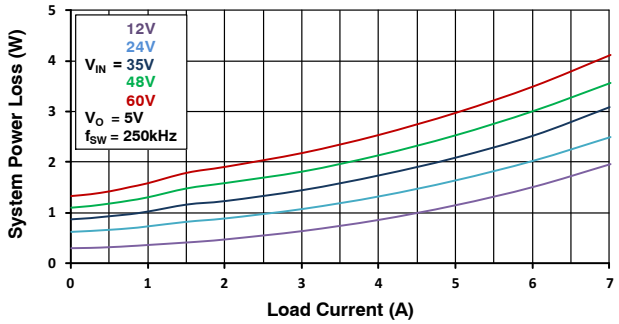


Figure 39. System Power Loss

NOTE: EXTBIAS is connected to V_O for Figures 21−39

Functional Description

FAN65005A is a high-efficiency synchronous buck converter with integrated controller, driver and two power MOSFETs. It can operate over a 4.5 V to 65 V input voltage range, and delivers 8 A load current. The internal reference voltage is 0.6 V ±1% over −40°C to 125°C temperature range.

FAN65005A uses voltage mode PWM control scheme with input voltage feed-forward feature for the wide input voltage range. The high bandwidth error amplifier monitors the output voltage and generates the control signal for the pulse width modulation block. By adjusting the external compensation network, the system performance can be optimized based on the application parameters.

The switching frequency is set by an external resistor and can be synchronized to an external clock signal. To improve light load efficiency (low I_Q mode), either low-side MOSFET is turned off when the inductor current drops to zero or pulse skipping is implemented when load current further decreases. The high-side MOSFET current sense circuit is adopted for the peak current limiting function and the output voltage will be reduced in current limiting condition. Other protection functions include over temperature shut-down and over-voltage protection.

At the beginning of each switching cycle, the clock signal initiates a PWM signal to turn on high-side MOSFET, and at the same time, the ramp signal starts to rise up. A reset pulse is generated by the comparator when the ramp signal intercepts the COMP signal. This reset pulse turns off high-side MOSFET and turns on low-side MOSFET until next clock cycle comes. In the case that current limit is hit, a peak current limiting (PCL) signal is generated to turn off the high-side MOSFET until the next PWM signal. This is cycle by cycle current limit protection. When certain faulty condition is met, the device enters hiccup mode to further protect itself.

LDOs

Two LDOs are included in FAN65005A to provide internal supply and to balance power loss from them. The LDO block diagram is shown below.

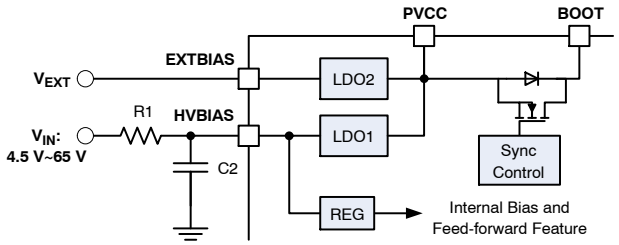


Figure 40. LDO Block Diagram

Since LDO1 input, HVBIAS, is also used for initial internal bias and for input voltage feed-forward compensation, system input voltage, VIN, should always be connected to HVBIAS pin and an RC filter is recommended between VIN and HVBIAS to filter any noise from high frequency switching. During power up, LDO1 is always selected. After the system finishes soft start, which LDO block is selected depends on voltages appearing on both HVBIAS and EXTBIAS pins. If there is a voltage at EXTBIAS pin and it is above 4.7 V, LDO2 will be selected, otherwise LDO1 will continue to supply power to the device. EXTBIAS can be left open for single LDO operation all the time. In the case that EXTBIAS is connected to a voltage, V_{EXT}, and V_{EXT} > 4.7 V and also $V_{EXT} > V_{HVBIAS}$, LDO2 will be selected. This makes power loss on LDO2 greater than that on LDO1 if LDO1 were selected. So it's the designer's responsibility to make sure $V_{EXT} < V_{HVBIAS}$ while V_{EXT} > 4.7 V. Both LDOs work in switch mode when their input voltages are lower than 5.4 V. This allows very low voltage drop on both LDOs and ensures high enough voltage level on PVCC for internal bias and MOSFET drive.

Assuming $V_{EXT} < V_{HVBIAS}$ while V_{EXT} > 4.7 V, Table 6 shows which LDO will be selected and the LDO work status. (• indicates which LDO and mode are selected and × means disabled)

Table 6. LDO SELECTION AND WORK MODE

Input		Work Mode			
		LDO1		LDO2	
HVBIAS (V)	EXTBIAS (V)	Switch	LDO	Switch	LDO
4.5–4.7	4.5–4.7	•	×	×	×
4.7–5.5	4.5–4.7	•	×	×	×
	4.7–5.5	×	×	•	×
5.5–65	4.5–4.7	×	•	×	×
	4.7–5.5	×	×	•	×
	5.5–50	×	×	×	•

Both LDOs are designed to deliver up to 150 mA current. A 4.7 μF ceramic capacitor between PVCC and PGND placed as close as possible to PVCC pin is recommended to decouple any noise from high frequency driver currents. A 1 Ω resistor can be used between PVCC and VCC together with a ceramic capacitor between VCC and AGND to form a filter for the VCC bias supply for the internal control circuits. When VCC voltage drops below its UVLO, the regulator control circuit blocks are disabled.

Enable and Under Voltage Lock-Out

EN/UVLO signal is used for device enable/disable when its voltage is higher/lower than the threshold, V_{EN_TH}, which is typical 1.22 V. The precision threshold voltage of this signal can also be used to set a system input voltage level, above which FAN65005A will be enabled and below which disabled. Figure 41 shows the EN/UVLO block diagram and application configuration.

A resistor divider (R2 and R3, as shown in Figure 1) can be used to set the level of input voltage, V_{IN_UVLO}, which enables the device. Selection of R3 is determined by Equation 1.

$$R3 = \frac{V_{EN\_TH} \times R2 \times R_{EN\_PD1}}{V_{IN\_UVLO} \times R_{EN\_PD1} - V_{EN\_TH} \times R2 - V_{EN\_TH} \times R_{EN\_PD1}} \quad \text{(eq. 1)}$$

R2 and R3 are both in kΩ.

Assuming *i*, in mA, is the current flowing through R2 when working input voltage is V_{IN}, then R2 is determined by Equation 2.

$$R2 = \frac{V_{IN\_UVLO} - V_{EN\_TH}}{V_{IN\_UVLO}} \times \frac{V_{IN}}{i} \quad \text{(eq. 2)}$$

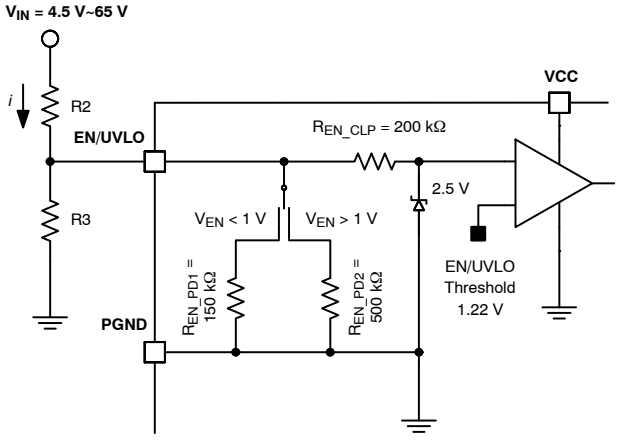


Figure 41. EN/UVLO Block Diagram

For example, a converter has nominal input voltage of V_{IN} = 48 V. It's desired that the device is enabled when input voltage is above 35 V, which makes V_{IN_UVLO} = 35 V. If 50 μA is chosen, then Equations 1 and 2 yield R2 and R3 in Equations 3 and 4 respectively:

$$R2 = \frac{48 \times (35 - 1.22)}{35 \times 50 \times 10^{-6} \times 10^{3}} = 926.5\ k\Omega \quad \text{(eq. 3)}$$

$$R3 = \frac{1.22 \times 926.5 \times 150}{35 \times 150 - 1.22 \times 926.5 - 1.22 \times 150} = 43.1\ k\Omega \quad \text{(eq. 4)}$$

Choose the closest standard 1% resistor values of R1 = 931 kΩ and R2 = 43.2 kΩ. What value is chosen for *i* is a power loss matter. The greater the *i* is, the greater the power loss will be, and vice versa. But if the current is too low, the EN/UVLO signal will be vulnerable to noise. Choose the highest possible current that only creates negligible power loss to the system. In the example shown above, the power loss in this EN/UVLO branch is $P = V_{IN} \times i = 48\ V \times 50\ \mu A = 2.4\ mW$.

When the device is disabled, only a few micro-ampere current is required to support essential blocks like bandgap. Only after the device is enabled, major functions like, LDO, oscillator, soft start, driver, logic control, start to run. The device is disabled if the EN/UVLO pin is floating.

Soft Start

The soft start block diagram is shown in Figure 42.

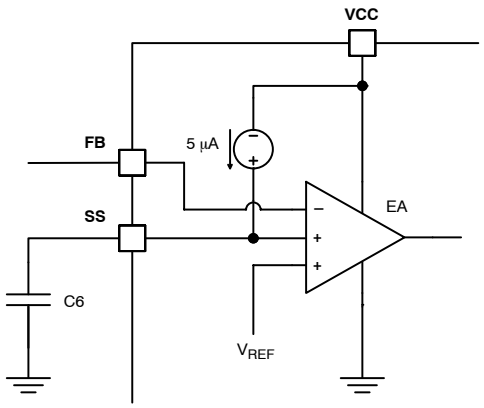


Figure 42. Soft Start Block Diagram

The soft start function is enabled with a delay of maximum 3 ms after EN is high. During the delay, the SS capacitor is discharged if there is any residual voltage. If SS voltage is still not 0 after this delay, a fault condition is created and the device enters hiccup mode, otherwise soft start process is initiated. A typical 5 μA constant current flows out of SS pin to charge the capacitor at SS pin. The error amplifier regulates the converter output voltage according to the lower value of SS pin voltage and the fixed 0.6 V reference voltage. With the constant current, SS voltage linearly ramps up from 0, and the regulator output voltage follows the SS voltage to ramp up. SS voltage continues to rise after it exceeds the 0.6 V reference voltage, at which point, the SS voltage is out of the loop and the converter output voltage is regulated to the reference voltage of 0.6 V. When SS capacitor is charged to 1.5 V, the SS timer stops counting and the device checks if FB has reached 94% V_{REF}. If not, the device enters hiccup mode, otherwise, the device considers the soft start successful and continues to charge SS capacitor until it reaches VCC.

If the SS pin is floating, device enters hiccup.

Pre-bias Startup

A pre-biased regulator is one that, before the regulator is powered, has output voltage above 0, and so for the FB pin. FAN65005A is able to start in such a case. When soft start is initiated, both high- and low-side MOSFETs are forced off until the SS pin is charged up to the pre-biased FB voltage. The following startup process will be a normal soft start process as stated in “Soft Start” section.

Switching Frequency

The internal clock generator can be programmed from 100 kHz to 1 MHz by a resistor connected between the R_T pin and the AGND pin. To set the desired switching frequency, the resistor can be calculated by Equation 5 as shown below:

$$f_{SW} = \min\left[\frac{10^4}{RT + 2.5} + 50,\ 1000\right] \qquad \text{(eq. 5)}$$

where f_{SW} is in kHz and RT is in kΩ.

The switching frequency vs. the external resistor curve is shown below.

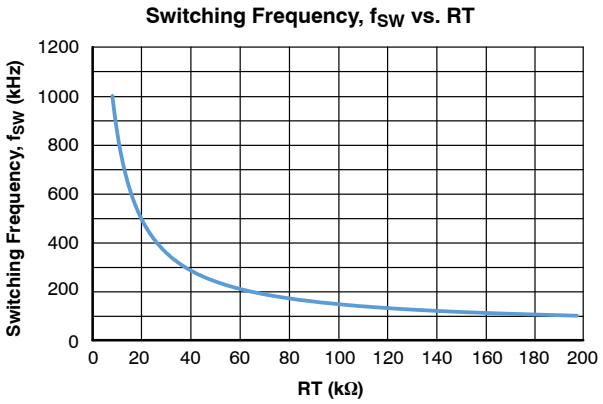


Figure 43. Relationship between RT and f_{SW}

As soon as the device is enabled, it will go through a set of routine to check the RT pin configuration to determine the switching frequency or if there is any fault. If RT is tied to VCC, the switching frequency is 250 kHz, and 500 kHz if short-circuited to AGND. If RT pin is floating initially or becomes open from any non-open state, the device enters hiccup mode.

Frequency Synchronization

FAN65005A can be set to work in either master mode or non-master mode. When in master mode, it sends out clock signal through SYNC pin; when in non-master mode, it either takes in clock signal from an external source on SYNC pin in ±30% of RT set frequency or uses RT to set its clock. Both modes are configured via MODE pin.

1. Master mode: A 100 kΩ resistor connected between MODE pin and either VCC or AGND

will enable master mode. In this mode, FAN65005A generates its ramp and PWM signal by its own and sends out PWM clock through SYNC pin with 180 degree phase shift and 50% duty cycle. If an external clock is detected on SYNC pin that is in conflict with the internal one, FAN65005A makes SYNC pin high impedance until fault is cleared.

2. Non-master mode: The MODE pin connected to either VCC or AGND through a 1 kΩ~5 kΩ resistor or left floating enables this mode. In this mode, the device keeps checking the SYNC pin for incoming clocks every 2 ms. If 64 cycles of clock are detected and the clock frequency is in ±30% of RT set frequency, the device is in sync with the clock appearing on SYNC pin. If no clocks are detected, the number of clocks in 2 ms does not reach 64, or the clock frequency is not within ±30% of RT set frequency, the device uses RT to set the clock. The synchronization block diagram is shown below.

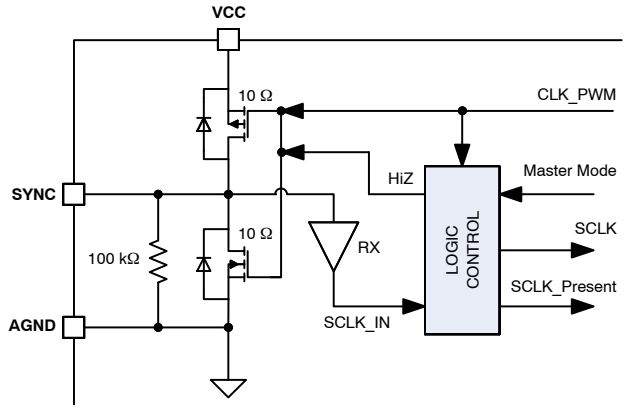


Figure 44. Frequency Synchronization Block Diagram

FAN65005A implements fault protection in case SYNC pin is short-circuited to either AGND or VCC. The logic checks voltage levels of both internal driving clock and SYNC pin except for a 100 ns time period at every clock transition, which is used to mask the transition glitches due to propagation delay. These 2 logic levels are expected to be the same when there is no pin fault. When SYNC pin fault is detected, the driver is disabled by using high impedance for 8 clock cycles, which makes worst case duty cycle of ~1.67% with 1 MHz frequency.

SYNC pin fault is only a local fault and doesn't trigger global hiccup or stop device operation. Figure 44 shows the frequency synchronization block diagram.

Operation Modes

The MODE pin controls 2 functions: pulse modulation and frequency synchronization.

Pulse modulation refers to continuous conduction fixed frequency pulse width modulation (short-formed Forced CCM) and discontinuous conduction with pulse skipping modulation (Short-formed DCM with Pulse Skipping). When in DCM with Pulse Skipping, device works in discontinuous conduction mode when inductor current hit 0 and may skip pulses when load becomes even lighter; device transits to fixed frequency operation and works in continuous conduction mode when inductor current valley is higher than 0. Frequency synchronization refers to master or non-master mode.

If low output voltage ripple is desired, Forced CCM PWM operation can be selected. In this mode, continuous conduction fixed switching frequency applies regardless of light load or heavy load and negative current appears at light load condition. This results in greater power loss at light load.

To reduce the power loss at light load, DCM with Pulse Skipping can be chosen. When at light load, the device works in discontinuous conduction mode and skips pulses, so that the power loss is reduced.

The relationship between the MODE configuration and the actual mode is illustrated in the following table:

Table 7. OPERATION MODES WITH MODE CONFIGURATION

MODE Pin Configuration	Operation Mode	
	Pulse Modulation	Freq Sync
VCC ← R = 1 kΩ~5 kΩ → MODE	Forced CCM	Non-master
VCC ← R = 100 kΩ ±30% → MODE	Forced CCM	Master
GND ← R = 1 kΩ~5 kΩ → MODE	DCM with Pulse Skipping	Non-master
GND ← R = 100 kΩ ±30% → MODE	DCM with Pulse Skipping	Master
Floating	Forced CCM	Non-master

Power Good

A comparator monitors the FB voltage and controls an open drain MOSFET. The PGOOD pin is connected to the Drain of this MOSFET. To correctly use the PGOOD signal, a pull-up resistor connected to an external voltage source is required. When FB voltage exceeds 94% of V_{REF} (typical 0.6 V), PGOOD signal is asserted after a delay, t_{PG_DL}, and when it's below 92% of V_{REF} it is de-asserted. PGOOD signal is valid only after device is enabled and soft start is completed (SS ramps above 0.6 V). When OVP1 is detected, PGOOD is de-asserted. PGOOD is re−asserted with 5% hysteresis. Figure 45 shows the internal circuitry connected to PGOOD pin.

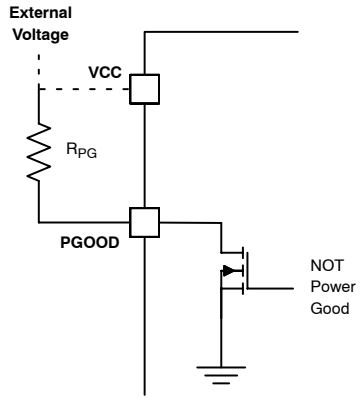


Figure 45. PGOOD Block Diagram

Setting Current Limit

A resistor, R_ILIM, connected between ILIM pin and GND is used to set the current limit for both high- and low-side MOSFETs. An 8.5 μA internal current source flows through R_ILIM, creating a reference voltage, and the voltage drops on R_{DSON} of both high- and low-side MOSFETs are used to compare with this reference voltage. This comparison generates an over current event. The high-side MOSFET current is monitored in forward direction, i.e. current flows from drain to source, while low-side MOSFET current is monitored in a reverse direction. When low-side MOSFET turns on in a normal condition, its current flows from ground to switching node. Current is NOT monitored in this case. If current flows from switching node to ground, it is considered abnormal and is monitored. The current limit for both high- and low-side MOSFETs is calculated the same way, $I_{LIM} = k_{ILIM} \times R_{ILIM}$, and k_{ILIM} parameters for both high- and low-side MOSFETs are shown in the Electrical Characteristic Table. If ILIM is tied to VCC, system is in standby mode, enabling all blocks except driver.

R_ILIM below 60 kΩ is defined as short-circuit, above 350 kΩ is considered to be open.

Over Current Protection (OCP) and Short Circuit Protection (SCP)

FAN65005A implements over current protection for high- and low-side MOSFETs in a different way.

For high-side MOSFET, FAN65005A sets two levels of over load protection according to the current limit setting: over current protection (OCP) and short circuit protection (SCP). OCP happens when the high-side MOSFET current, i_{DS_HS}, is in the range of $100\% I_{LIM\_HS} \le i_{DS\_HS} < 130\% I_{LIM\_HS}$, and SCP occurs when $i_{DS\_HS} \ge 130\% I_{LIM\_HS}$. FAN65005A monitors MOSFET current constantly and provides cycle by cycle peak current limit. The high-side MOSFET is turned off whenever its current exceeds the limit.

Once the current limit is hit, FAN65005A counts. If 1024 consecutive OCP events have reached, regardless of the FB voltage, the system enters hiccup mode.

The worst case of over current is such conditions as short-circuited output or saturated inductor, in which the current exceeds 130% of current limit. In this case, device initiates short circuit protection and enters hiccup mode immediately.

For low-side MOSFET, FAN65005A performs cycle by cycle protection if its current limit is hit. At each cycle of low-side MOSFET turn-on, its current is checked. If the current exceeds its current limit, I_{LIM_LS}, the low-side MOSFET will be turned off immediately and remains off until next switching cycle. This process repeats until the over current event is released (low-side MOSFET current becomes less than I_{LIM_LS}). Low-side MOSFET over current protection doesn't affect high-side MOSFET switching, i.e. high-side MOSFET remains normal switching if high-side MOSFET over current event does not occur.

Hiccup Mode

Hiccup mode is described as follows. When a fault condition is met, both high- and low-side MOSFETs turn off for a period of time, t_{HICCUP} (typical 1 s), and soft start capacitor is discharged. Then device enters soft start. After soft start, if the fault condition is met again, both high- and low-side MOSFETs turn off for t_{HICCUP} again and soft start capacitor is discharged…System returns to normal operation after the fault event is released.

Over Voltage Protection (OVP)

There are 2 levels of over voltage protection: over voltage protection 1 (OVP1) and over voltage protection 2 (OVP2), which are defined below respectively.

1. OVP1 is protection when FB voltage is above 115% but below 130% of V_{REF}. When OVP1 is triggered, both high- and low-side MOSFETs are turned off immediately. When FB falls to or below V_{REF}, the system returns to normal operation and initiates a new PWM signal at the next clock cycle.
2. OVP2 is protection when FB voltage is above 130% of V_{REF}. When OVP2 is triggered, the high-side MOSFET is turned off immediately while the low-side MOSFET is turned ON. If over current event occurs during the low-side MOSFET ON time, cycle by cycle protection will be performed as described in "Over Current Protection (OCP) and Short Circuit Protection (SCP)" section. As soon as over current event is released, the low-side MOSFET will be kept on again until FB voltage drops to or below V_{REF}. One hiccup cycle is initiated once output voltage reaches 100% level. After the hiccup, the part will go into a soft start sequence and try to regulate. If OVP2 happens during the hiccup timing period, nothing will happen.

In the case of OVP, power good signal is de-asserted and re-asserted after V_{FB} comes down to 110% V_{REF}.

Under Voltage Protection (UVP)

Under voltage is a condition when output voltage is below 35% of its regulated level (checked on FB pin). If $V_{FB} \leq 35\%$ is met, then under voltage protection (UVP) is initiated, where IC enters hiccup mode.

Over Temperature Protection (OTP)

The device keeps monitoring the junction temperature. When the sensed temperature is above the protection point, T_{J_SD}, over temperature protection (OTP) event occurred and the system shuts down. OTP is released when the sensed temperature is 20° lower than the trip point, T_{J_SD}, where the system resets through soft-start.

Output Inductor Selection

The output inductor is selected to meet the output ripple requirements. The inductor value determines the converter's ripple current ΔIL. Largest ripple current occurs at highest Vin voltage.

$$\Delta IL = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{F_{SW} \cdot L \cdot V_{IN}} \quad \text{(eq. 6)}$$

Lower ripple current reduced core losses in the inductor and output voltage ripple. Highest efficiency is obtained at low frequency with small ripple current, however with a disadvantage of using a large inductor. Inductor value can be chosen based on the equation below in order to not exceed a max ripple current (usually 30% to 70% of max inductor current)

$$L \geq \frac{(V_{IN} - V_{OUT})}{F_{SW} \cdot \Delta I_L} \cdot D \quad \text{(eq. 7)}$$

Output Capacitor Selection

In general, the output capacitors should be selected to meet the dynamic regulation requirements including ripple voltage and load transients.

1. For ripple voltage considerations; the output bulk maintains the DC output voltage. The use of ceramic capacitors is recommended to sustain a low output voltage ripple. At switching frequency the ceramic capacitors are capacitance dominante use the following equation for calculating C_{out} where the ripple output voltage is within 1% of Vout.

$$\Delta_{OUT} = \frac{V_{OUT} \cdot (1 - D)}{8 \cdot F_{SW}^2 \cdot L \cdot C_{OUT}} \quad \text{(eq. 8)}$$

And the RMS current through it is

$$I_{COUT(RMS)} = I_{OUT} \cdot \frac{\Delta I_L(pp)}{\sqrt{12}} \quad \text{(eq. 9)}$$

2. The maximum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor is shown

$$C_{MIN} = \frac{L \cdot I_{PK}^2}{(V_{OV} + V_{OUT})^2 - V_{OUT}^2} \quad \text{(eq. 10)}$$

where I_{PK} is defined as:

$$I_{PEAK} = I_{OUT,MAX} - \frac{\Delta I_L}{2} \quad \text{(eq. 11)}$$

Where CMIN is the minimum value of output capacitor required, L is the output inductor, IPK is the peak load current, VOV is the increase in output voltage during a load release, VOUT is output voltage.

Input Capacitor Selection

Voltage and RMS current rating of the input capacitors are critical factors. Typically input capacitor is designed based on input voltage ripple of 2%. Capacitor voltage rating must be at least 1.25x greater than max input voltage . Maximum RMS current supplied by the input capacitance occurs at 50% duty cycle and when Vin =2 x Vout.

RMS current varies with load as shown below:

$$I_{CIN(RMS)} = I_{OUT} \cdot \sqrt{D \cdot \left(1 - D + \frac{\Delta IL(pp)^2}{12}\right)} \quad \text{(eq. 12)}$$

Ceramic capacitors are best known for low ESR and are highly recommended.

Loop Compensation

Selecting External Compensation:

The FAN65004B is a voltage mode buck regulator with an error amplifier compensated by external components to achieve accurate output voltage regulation and to respond to fast transient events. The goal of the compensation network is to provide a loop gain function with the highest cross−over frequency at adequate phase and gain margins.

The output stage (LC) of the buck regulator is a double pole system. The resonance frequency of this lowpass filter is shown below:

$$f_{p0} = \frac{1}{2\pi \cdot \sqrt{LC_{OUT}}} \quad \text{(eq. 13)}$$

The output filter has a zero that is calculated from the output capacitance and output capacitor ESR:

$$f_{z0} = \frac{1}{2\pi \cdot ESR \cdot C_{OUT}} \quad \text{(eq. 14)}$$

The bode plot of the power stage, error amplifier and the desired loop gain are drawn in the figure below. The first zero (f_{z1}) compensates the phase lag of the pole located at the origin followed by a second zero (f_{z2}) to compensate for one of the poles of the LC filter in order to crossover (f_c) at −20 dB slope. The second pole (f_{p2}) is aimed to cancel the ESR zero and finally the third pole (f_{p3}) is to provide attenuation for frequencies above $f_{sw/2}$.

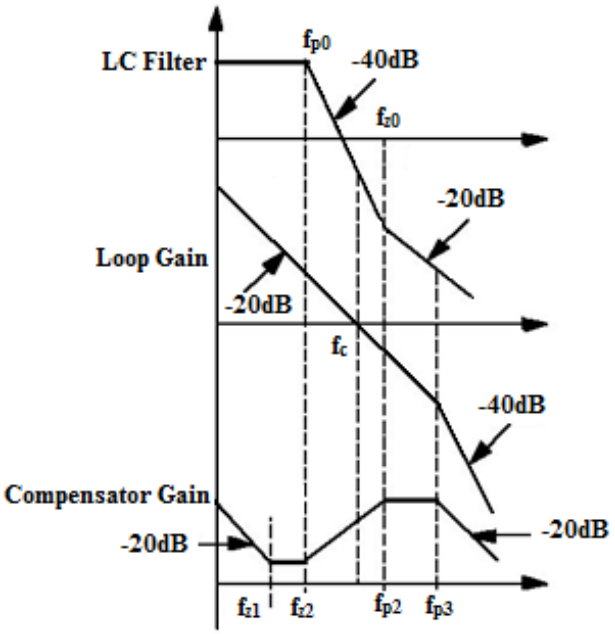


Figure 46. Power Stage, Loop Gain and Compensator Bode Plots

For ease of calculation, with C1 >> C3:

$$f_{z1} = \frac{1}{2\pi \cdot (R10 + R9) \cdot C9}$$

$$f_{z2} = \frac{1}{2\pi \cdot R8 \cdot C7}$$

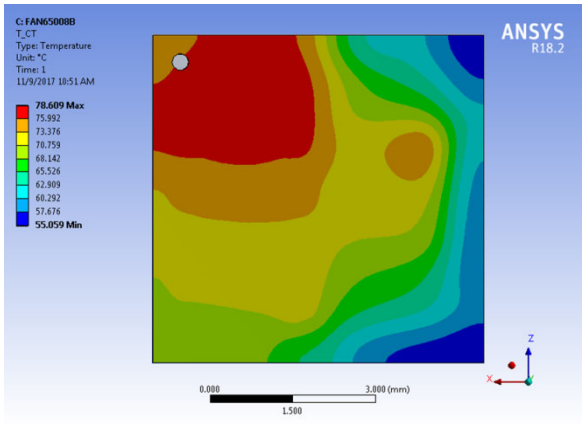
$$f_{p2} = \frac{1}{2\pi \cdot R9 \cdot C9}$$

$$f_{p3} = \frac{1}{2\pi \cdot R8 \cdot C8}$$

$$f_c = \frac{V_{IN}}{2\pi \cdot V_{Ramp} \cdot R10 \cdot C7}$$

Thermal Considerations

The temperature gradients on the FAN65004B are shown below. While measuring the thermal performance, place the thermocouple at the hottest spot of the IC (not at the center of the part).



Layout Guidelines

1. Place RT resistor and SS capacitor close to RT and SS pins.
2. Use a low impedance source such as a logic gate to drive the SYNC pin and keep the PCB trace as short as possible.
3. Components of digital signals like EN/UVLO, PGOOD and SYNC can be placed far away from device.
4. Place BOOT capacitor right next to BOOT and PH pins. If flexibility of high−side MOSFET driving strength is desired, place a resistor in series with this BOOT capacitor. **For Vin > 40 V, use Rboot = 2 ohm.**
5. Place inductor on top layer. Restrict the SW trace to only cover the inductor pin but keep its trace as wide as possible for thermal relief.
6. Avoid all the compensation components from passing through, above or underneath switching trace.
7. Keep the switching nodes away from sensitive small signal nodes (FB). Ideally the switch nodes printed circuit traces should be routed away and separated from the IC and especially the quiet side of the IC. Separate the high dv/dt traces from sensitive small−signal nodes with ground traces or ground planes.
8. Place decoupling caps right next to PVCC, VCC , HVBIAS and EXTBIAS.
9. The output capacitors should be placed as close to the load as possible. Use short wide copper regions to connect output capacitors to load to avoid inductance and resistances.

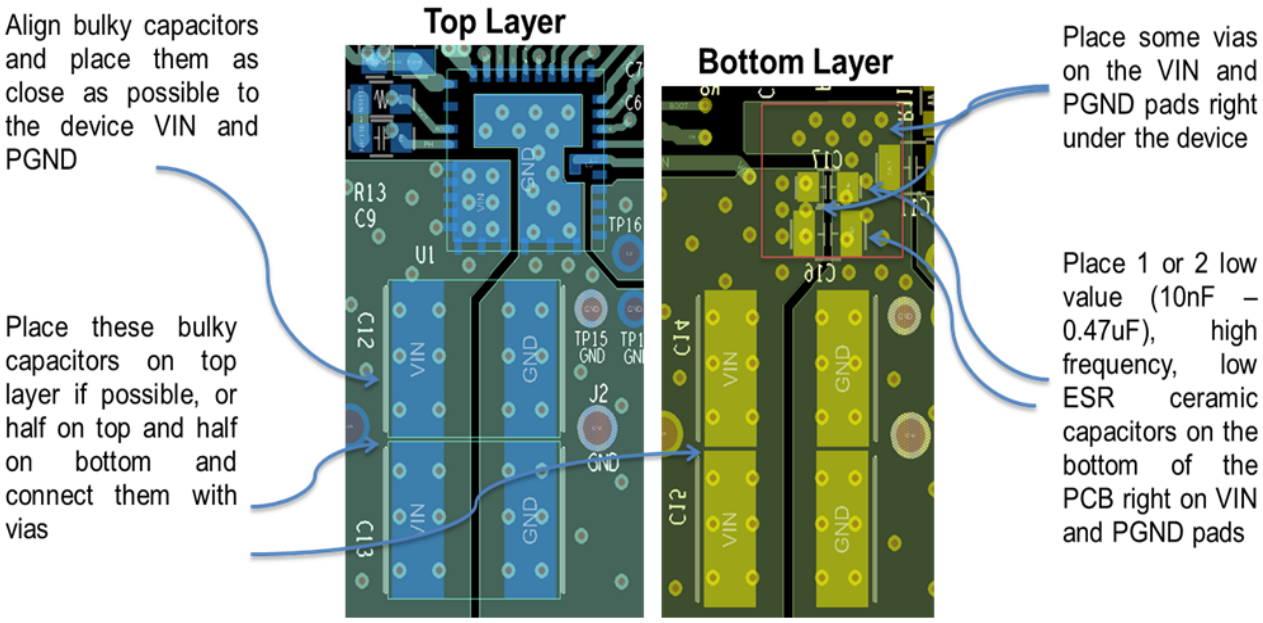
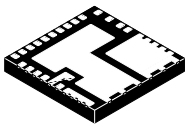


Table 8. ORDERING INFORMATION

Part Number	Current Rating (A)	Input Voltage Max. (V)	Frequency Max. (kHz)	Package
FAN65005A	8	65	1000	PQFN 6.0 × 6.0 mm

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

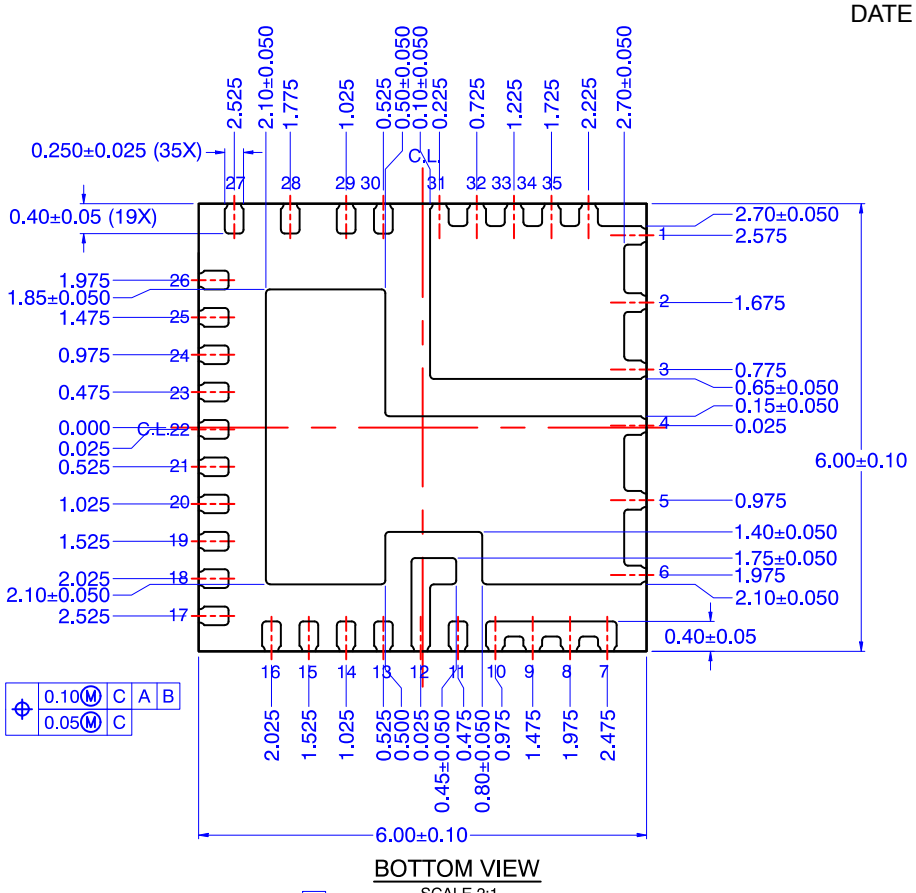
ON Semiconductor®



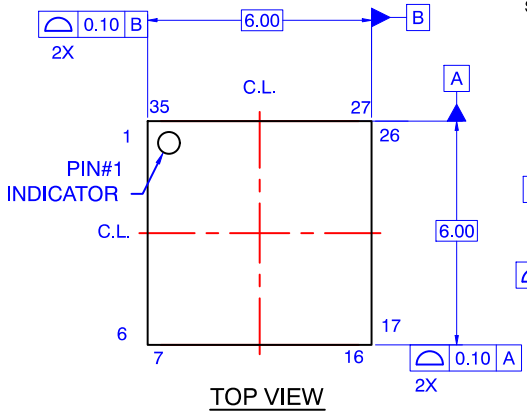
SCALE 2:1

PQFN35 6X6, 0.5P
CASE 483BE
ISSUE O

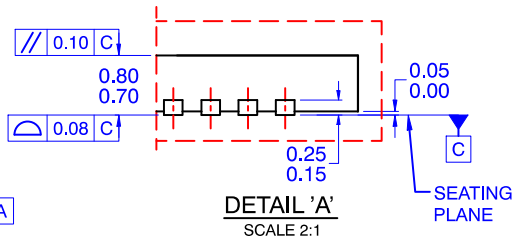
DATE 30 SEP 2016



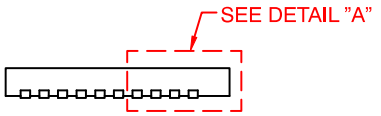
BOTTOM VIEW
SCALE 2:1



TOP VIEW



DETAIL 'A'
SCALE 2:1



FRONT VIEW

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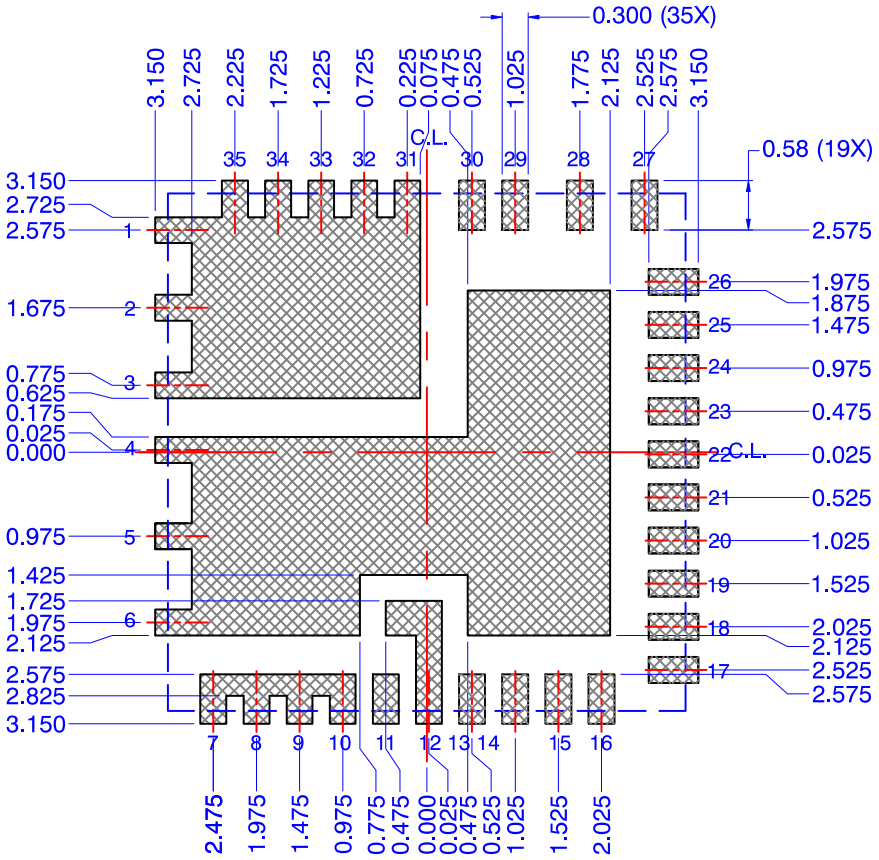
PQFN35 6X6, 0.5P
CASE 483BE
ISSUE O

DATE 30 SEP 2016



LAND PATTERN RECOMMENDATION
SCALE 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO−220, ISSUE K.01, DATED AUG 2011.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−2009.

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PUBLICATION ORDERING INFORMATION

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