PET750-12-050xD

DC-DC Front-End Power Supply

The PET750-12-050xD is a 750 Watt DC to DC power supply that converts -40 to -72 VDC voltage into an insulated main output of +12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches. The PET750-12-050xD utilizes digital control architecture for greater efficiency, control and functionality.

This power supply meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

Key Features & Benefits

- High Efficiency to 94% at 50% load
- Wide input voltage range: -40 to -72 VDC
- Always-On 5V/3A/15W standby output
- Hot-plug capable
- Parallel operation with active current sharing
- Digital controls for improved performance
- High Density Design 20.5 W/in^3
- Small Form Factor: 300 x 50.5 x 40 mm (11.81 x 1.99 x 1.57 in)
- Power Management Bus communications protocol for control, programming and monitoring
- Over temperature, output over voltage and over current protection
- Status LED with fault signaling

Applications

- Networking Switches
- High Performance Servers
- Routers

1. ORDERING INFORMATION

PET	750	-	12	-	050	x	D
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**
PET Front-Ends	750 W		12 V		50 mm	N: Normal R: Reverse*	D: DC

* Contact factory for availability.

2. OVERVIEW

The PET750-12-050ND DC/DC power supply is a DSP controlled, highly efficient front-end power supply. It incorporates state-of-the art technology and uses a forward converter topology with active clamp and synchronous rectification to reduce component stresses, thus providing increased system reliability and high efficiency.

With a wide input DC voltage range the PET750-12-050ND maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow path.

An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.

The always-on standby output provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.

Status information is provided with a front-panel LED. In addition, the power supply can be controlled and the fan speed set via the I^2C bus. The I^2C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures.

Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I^2C bus.

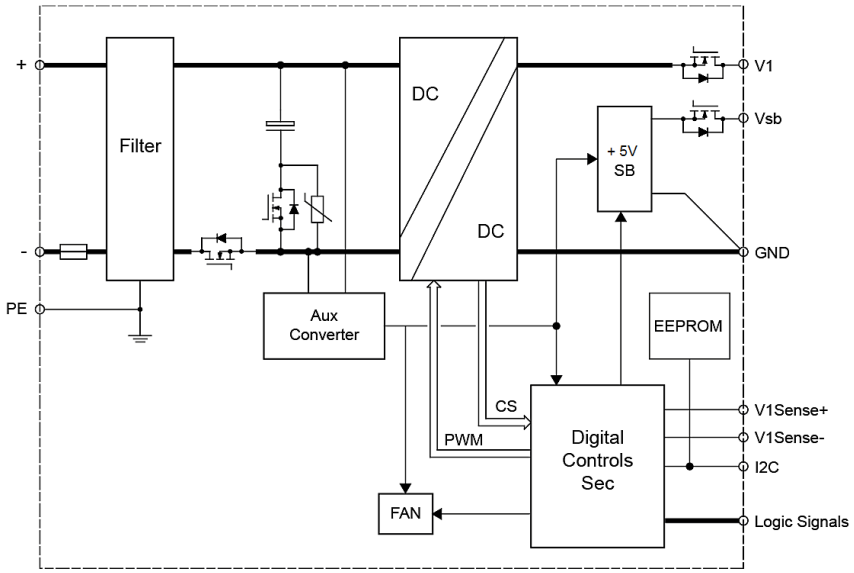


Figure 1. Block Diagram

3. ABSOLUTE MAXIMUM RATING

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Vi *maxc*	Maximum Input Voltage	Continuous			-75	VDC

4. INPUT

General Condition: T_A = 0… 50 °C unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Vi start	Minimum operating input voltage	Stand-by output available, DSP running	-30			VDC
Vi nom	Nominal input voltage			-54		VDC
Vi	Input voltage	Normal operation (from Vi min to Vi max)	-40		-72	VDC
Ii	Input current	Vi > Vi min			25	A
Ii pk	Inrush current limitation	From Vi min to Vi max, T_A = 25°C, turn on			50	A
Vi on	Turn-on standby input voltage	Ramping up	-30			VDC
Vi on	Turn-on input voltage	Ramping up	-39		-43	VDC
Vi off	Turn-off input voltage	Ramping down	-37		-41	VDC
η	Efficiency	Vi = -48 VDC; -54 VDC; -60 VDC; 20% load		90		%
		Vi = -48 VDC; -54 VDC; -60 VDC; 50% load		94		%
		Vi = -48 VDC; -54 VDC; -60 VDC; 100% load		91		%
Thold_V1	Hold-up time V1	62 A on V1, 3 A on Vsb with 11000 µF Load capacitance, Vi = -48 VDC	1			ms
Thold_sb	Hold-up time Vsb	62 A on V1, 3 A on Vsb with 350 µF Load capacitance, Vi = -48 VDC	2			ms

4.1 INPUT FUSE

A fast-acting 30 A input fuse in the negative voltage path inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

4.2 INRUSH CURRENT

Internal bulk capacitors will be charged through resistors connected from bulk cap minus pin to the DC rail minus, thus limiting the inrush current. After the inrush phase, NTC resistors are then shorted with MOSFETs connected in parallel. The Inrush control is managed by the digital controller (DSP).

4.3 INPUT UNDER-VOLTAGE

If the value of input DC voltage stays below the input under voltage lockout threshold Vi on, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

4.4 EFFICIENCY

The power supply module efficiency curve is measured at -48VDC and with external fan power as below.

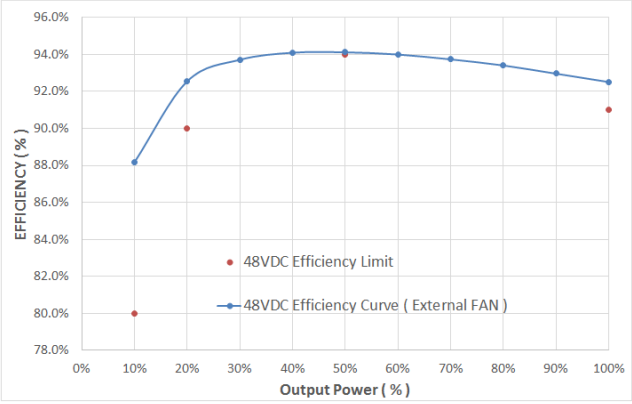


Figure 2. Efficiency Curve

5. OUTPUT

General Condition: T_A = 0…50 °C unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V_1						
$V_{1\ nom}$	Nominal Output Voltage	0.5 · $I_{1\ nom}$, T_A = 25°C		12.0		VDC
$V_{1\ set}$	Output Set Point Accuracy		-0.5		+0.5	%$V_{1\ nom}$
$dV_{1\ tot}$	Total Static Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, T_A = 0 to 40°C	-5		+5	%$V_{1\ nom}$
$P_{1\ nom}$	Nominal Output Power [1]	$V_{i\ min}$ to $V_{i\ max}$, T_A = 0 to 50°C		744		W
$I_{1\ nom}$	Output Current	$V_{i\ min}$ to $V_{i\ max}$,, T_A = 0 to 50°C		62		ADC
$V_{1\ pp}$	Output Ripple Voltage	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, 20Mhz Bandwidth			150	mVpp
$dV_{1\ load}$	Load Regulation	$V_{i\ nom}$, 0 to 100% $I_{1\ nom}$	-240		240	mV
$dV_{1\ line}$	Line Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0.5 · $I_{1\ nom}$	-120		120	mV
$dV_{1\ temp}$	Thermal Drift	$V_{i\ nom\ HL}$, 0.5 · $I_{1\ nom}$			0.1	%/°C
$dI_{1\ share}$	Current Sharing	Deviation from $I_{1\ tot}$ / N, I_1 > 10%	-5		+5	ADC
V_{ISHARE}	Current Share Bus Voltage	$I_{1\ peak}$		8		VDC
$dV_{1\ lt}$	Load Transient Response	ΔI_1 = 50% $I_{1\ nom}$, I_1 = 10 … 100% $I_{1\ nom}$, C_{ext} = 0mF, dI_1/dt = 1A/µs, recovery within 1% of $V_{1\ nom}$	-0.6		0.6	VDC
t_{rec}	Recovery Time				2	ms
$t_{V1\ on\ delay}$	Delay Time from DC Applied	V1 in regulation Vi = 0V to $V_{i\ min}$, $V_{i\ nom}$, $V_{i\ max}$			2.5	sec
$t_{V1\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom}$, 0 to 100% $I_{1\ nom}$			5	%$V_{1\ nom}$
$dV_{1\ sense}$	Remote Sense	Compensation for cable drop, 0 to 100% $I_{1\ nom}$			0.25	V
$C_{V1\ load}$	Capacitive Loading				11000	µF
Standby Output V_{SB}						
$V_{SB\ nom}$	Nominal Output Voltage	I_{SB} =1.5 A (50% of I_{SBnom}), T_A = 25°C		5		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		-0.5		+0.5	%V_{SBnom}
$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$	-3		+3	%V_{SBnom}
$P_{SB\ nom}$	Nominal Output Power	$V_{i\ min}$ to $V_{i\ max}$, T_A = 0 to 50°C		15		W
$I_{SB\ nom}$	Output Current	$V_{i\ min}$ to $V_{i\ max}$, T_A = 0 to 50°C			3	ADC
$dV_{sb\ load}$	Load Regulation	$V_{i\ nom}$, 0 to 100% $I_{sb\ nom}$	-75		75	mV
$dV_{sb\ line}$	Line Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0.5 · $I_{sb\ nom}$	-25		25	mV
dVSB	Droop	0 - 100 % $I_{SB\ nom}$		90		mV
$V_{SB\ pp}$	Output Ripple Voltage	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, C_{ext} = 0Mf, 20 MHz bandwidth			100	mVpp
$dI_{SB\ share}$	Current Sharing	Deviation from $I_{SB\ tot}$ / N, I_{SB} = 0.5 · $I_{SB\ nom}$	-1		+1	ADC
$t_{VSB\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom}$, 0 to 100% $I_{SB\ nom}$			5	%Vsb
dVSB	Load Transient Response	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 10… 100% $I_{SB\ nom}$, dI_{SB}/dt = 0.5 A/µs, recovery within regulation of $V_{SB\ nom}$	-3		+3	%Vsb
trec	Recovery Time				250	µs
$C_{VSB\ load}$	Capacitive Loading				350	µF

[1] See chapter *TEMPERATURE AND FAN CONTROL*

5.1 OUTPUT GROUND / CHASSIS CONNECTION

The output return path serves as power and signal ground. All output voltages and signals are referenced to these pins. To prevent a shift in signal and voltage levels due to ground wiring voltage drop a low impedance ground plane should be used as shown in *Figure 3*. Alternatively, separated ground signals can be used as shown in *Figure 4*. In this case the two ground planes should be connected together at the power supplies ground pins.

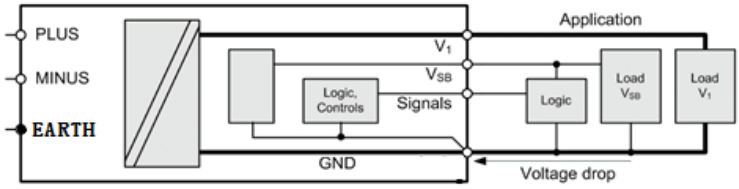


Figure 3. Common low impedance ground plane

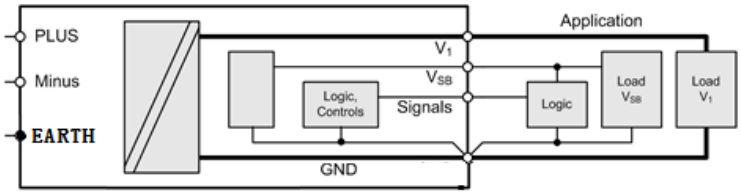


Figure 4. Separated power and signal ground

6. PROTECTION

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input fuse (L)	Not use accessible, fast acting		30		A
$V_{1\ OV}$	OV Threshold V_1	Over Voltage V_1 Protection, Latch-off Type, unlatch unit by disconnecting AC or by togging PS_ON signal	13.3		14.5	VDC
$V_{VSB\ OV}$	OV Threshold V_{SB}	Over Voltage Vsb Protection, unlatch unit by disconnecting AC or by togging PS_ON signal	5.75		6.5	VDC
$V_{1\ UV}$	UV Threshold V1	unlatch unit by disconnecting DC or by toggling the PS_ON signal		10.5		VDC
$I_{V1\ OC\ Slow}$	OC Limit V_1	Over Current Limitation, $V_{i\ min}$ to $V_{i\ max}$	65		71	ADC
$I_{VSB\ OC}$	OC Limit V_{SB}	Over Current Limit., Hiccup mode	3.5		4.5	A
T_{SD}	Over Temperature on Inlet	Automatic recovery with Hysteresis		60		°C
	Over Temperature Oring	Automatic recovery with Hysteresis		85		°C
	Over Temperature Secondary Rectifier	Automatic recovery with Hysteresis		105		°C

6.1 OVERVOLTAGE PROTECTION

The PET750-12-050ND front-end provides a fixed threshold overvoltage (OV) protection implemented with a HW comparator for both the main and the standby output. Once an OV condition has been triggered on the main output or VSB, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the DC supply or by toggling the PSON_L input.

6.2 UNDERVOLTAGE DETECTION

The main output will latch off when V1 drop to below the UV threshold. The latch can be unlatch by disconnecting the supply from the AC mains or by toggling the PS_ON input. The main output will shut down if the VSB voltage drop below 4 V and recover when VSB voltage higher than 4.3 V.

6.3 CURRENT LIMITATION

MAIN OUTPUT

The main output exhibits a substantially rectangular output characteristic controlled by a software feedback loop. If it runs in current limitation and its voltage drops below ~10.8 VDC for more than 10 ms, the output will latch off (standby remains on).

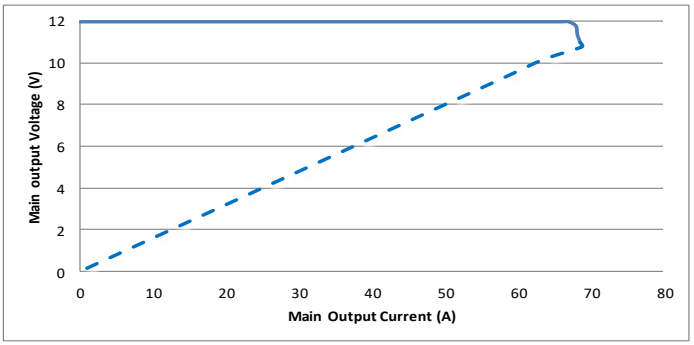


Figure 5. Current Limitation on V1 (Vi = -54 VDC)

A second current limitation circuit on V1 will immediately switch off the main output if the output current increases beyond the peak current trip point. The latch can be unlocked by disconnecting the supply from the DC mains or by toggling the PS_ON input.

STANDBY OUTPUT

The standby output exhibits a substantially rectangular output characteristic down to 0V (hiccup mode). If it runs in current Limitation and its output voltage drops below the UV threshold, then the main output will be inhibited.

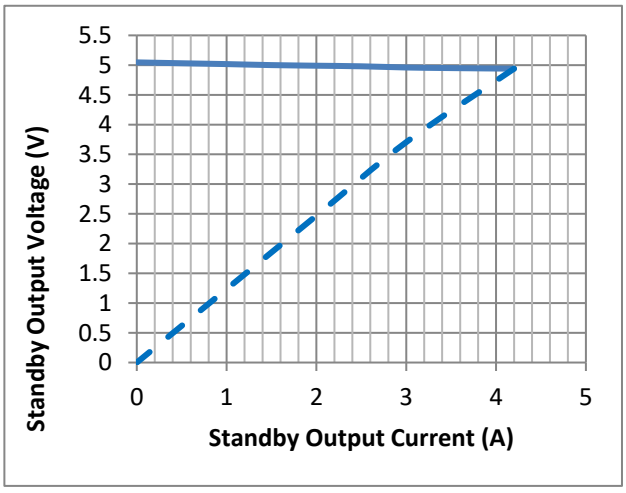


Figure 6. Current limitation on VSB

7. MONITORING

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ mon}$	Input Voltage	$V_{i\ min\ LL} \leq V_i \leq V_{i\ max}$	-2		+2	%
$I_{i\ mon}$	Input Current	I_i >7 A	-10		+10	%
$P_{i\ mon}$	True Input Power	P_i > 350 W	-10		+10	%
$V_{1\ mon}$	V_1 Voltage		-2		+2	%
$I_{1\ mon}$	V_1 Current	I_1 > 2 A	-5		+5	%
		I_1 ≤ 25 A	-2		+2	ADC
$P_{1\ nom}$	V_1 Output Power	P_1 > 300 W	-5		+5	%
		P_1 ≤ 300 W	-24		+24	W
$V_{SB\ mon}$	V_{SB} Voltage		-3		+3	%
$I_{SB\ mon}$	V_{SB} Current		-0.5		+0.5	ADC

8. SIGNALING AND CONTROL

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
PSON_H						
V_{IL}	Input Low Level Voltage	PSON_L: Main output enabled			0.5	V
V_{IH}	Input High Level Voltage	PSON_L: Main output disabled	2		3.5	V
$I_{IL,H}$	Maximum Input Sink or Source Current	V_I = -0.2 V to +3.5 V	-1		1	mA
$R_{pull\ up}$	Internal Pull up Resistor to internal 3.3 V			10		kΩ
R_{LOW}	Maximum external Pull down Resistance to GND to obtain Low Level				1	kΩ
R_{HIGH}	Minimum external Pull down Resistance to GND to obtain High Level		50			kΩ
PWOK_H						
V_{OL}	Output Low Level Voltage	$Vi < V_{i\ min\ LL}$, V_{Isink} < 4 mA			0.4	V
V_{OH}	Output High Level Voltage	$Vi > V_{i\ min\ LL}$, I_{source} < 0.5 mA	2.4		3.5	V
$R_{pull\ up}$	Internal Pull up Resistor to internal 3.3 V			1.6		kΩ
I_{OL}	Maximum Sink Current	V_O < 0.4 V			4	mA
DCOK_H						
V_{OL}	Output Low Level Voltage	I_{sink} < 4 mA			0.4	V
V_{OH}	Output High Level Voltage	I_{leak}< 50 µA	2.4		3.5	V
R_{puDC_OK}	Internal Pull Up Resistor on DC_OK			1.6		kΩ
SMB_ALERT						
V_{OL}	Output Low Level Voltage	I_{leak} < 4 mA			0.4	V
V_{OH}	Output High Level Voltage	I_{leak}< 100 µA	2.4		3.5	V
R_{puSMB_ALERT}	Internal Pull Up Resistor on SMB_ALERT			4.7		kΩ

8.2 SENSE INPUTS

The main output has sense lines implemented to compensate for voltage drop on load wires in both positive and negative path. The maximum allowed voltage drop is 200 mV on the positive rail and 100 mV on the GND rail.

With open sense inputs the main output voltage will rise by 270 mV. Therefore, if not used, these inputs should be connected to the power output and GND at the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.3 CURRENT SHARE

The PET front-ends have an active current share scheme implemented for V1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses an analog bus to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV.

The standby output uses a passive current share method (droop output voltage characteristic).

8.4 PSON_L INPUT

The PSON_L is an internally pulled-up (3.3 V) input signal to enable/disable the main output V1 of the front-end. With low level input the main output is enabled. This active-low pin is also used to clear any latched fault condition.
The PSON_L can be either controlled by an open collector device or by a voltage source.

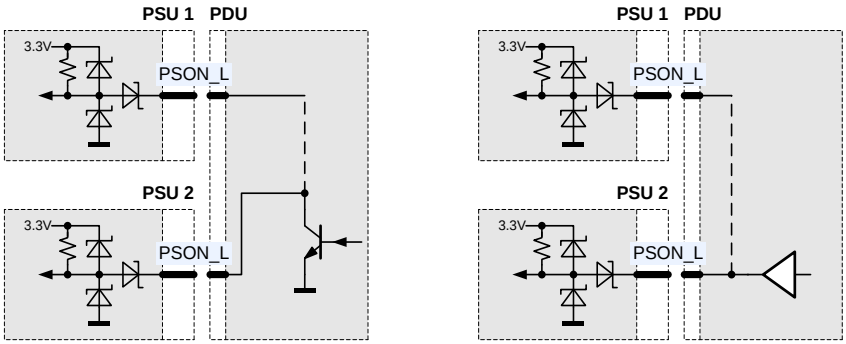


Figure 7. PSON_H connection

8.5 PWOK_H OUTPUT

The PWOK_H is an open drain output with an internal pull-up to 3.3 V indicating whether both VSB and V1 outputs are within regulation. This pin is active-high.

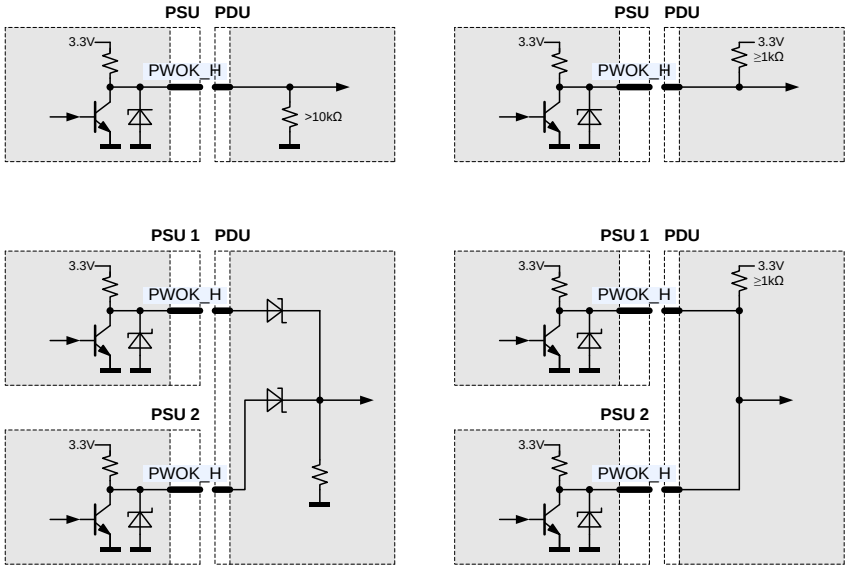


Figure 8. PWOK_H connection

8.6 PRESENT_L OUTPUT

The PRESENT_L pin is wired through a 100Ohms resistor to internal GND within the power supply. This pin does indicate that there is a power supply present in this system slot. An external pull-up resistor has to be added within the application. Current into PRESENT_L should not exceed 5mA to guarantee a low level voltage if power supply is seated.

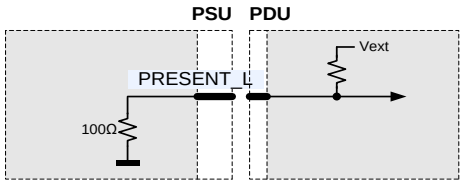


Figure 9. PRESENT_L connection

8.7 PDB_ALERT

The PDB_ALERT is received signal from system, if signal is pulled low, the unit internal fan will be forced to run at maximum speed, this signal is inactive at standby mode.

8.8 PDB_FAULT

The PDB_FAULT receive a signal from system, Power shall be shut down if this signal is high.

8.9 SIGNAL TIMING

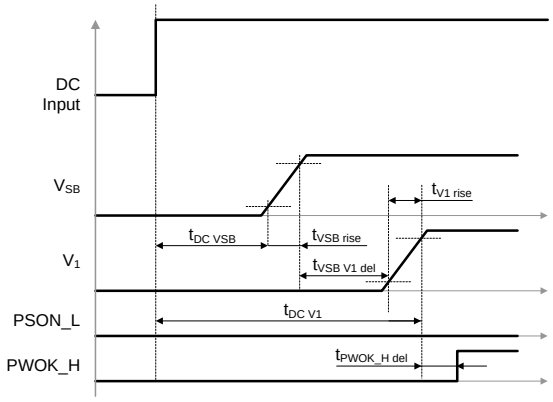


Figure 10. DC turn-on timing

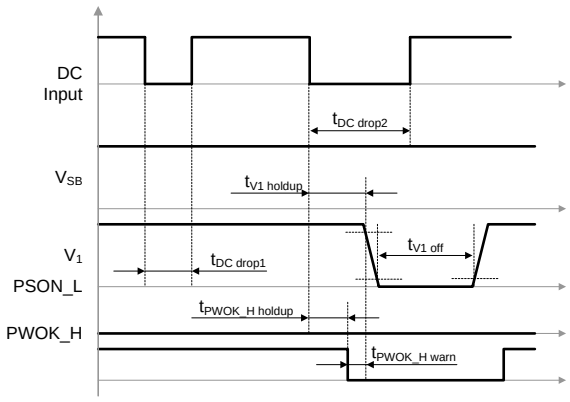


Figure 11. DC short dips

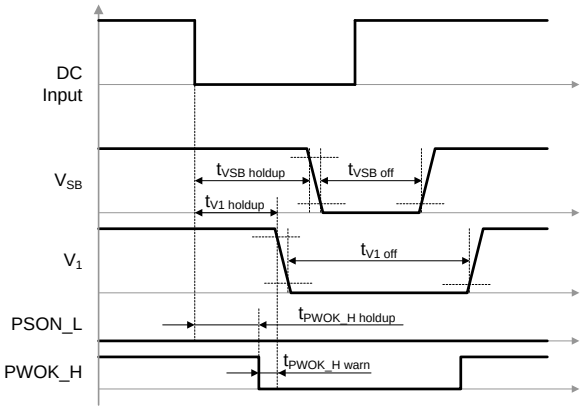


Figure 12. DC long dips

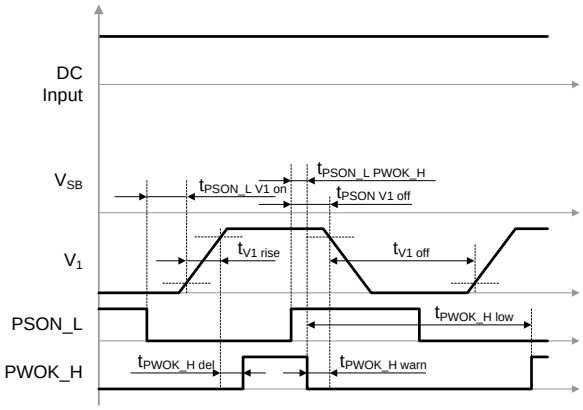


Figure 13. PSON_L turn-on/off timing

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$t_{DC\ VSB}$	DC Line to 90% V_{SB}				1500	ms
$t_{DC\ V1}$	DC Line to 90% V_1	PSON_L = Low			2500	ms
$t_{VSB\ V1\ del}$	V_{SB} to V_1 delay	PSON_L = Low	50		1000	ms
$t_{V1\ rise}$	V_1 rise time	See chapter OUTPUT	1		200	ms
$t_{VSB\ rise}$	V_{SB} rise time	See chapter OUTPUT	1		200	ms
$t_{DC\ drop1}$	DC drop without V_1 leaving regulation	$I_{1\ nom}$, $I_{SB\ nom}$			1	ms
$t_{DC\ drop2}$	DC drop without V_{SB} leaving regulation	$I_{1\ nom}$, $I_{SB\ nom}$			20	ms
$t_{V1\ holdup}$	Loss of DC to V_1 leaving regulation	See chapter INPUT	1			ms
$t_{VSB\ holdup}$	Loss of DC to Vsb leaving regulation	See chapter INPUT	10			ms
$t_{PWOK\_H\ del}$	Outputs in regulation to PWOK_H asserted		5		400	ms
$t_{PWOK\_H\ warn}$	Warning time from de-assertion of PWOK_H to V_1 leaving regulation		1			ms
$t_{PWOK\_H\ holdup}$	Loss of DC to PWOK_H de-asserted		4			ms
$t_{PWOK\_H\ low}$	Time PWOK_H is kept low after being de-asserted		100			ms
$t_{PSON\_L\ V1\ on}$	Delay PSON_L active to V_1 in regulation		5		400	ms
$t_{PSON\_L\ V1\ off}$	Delay PSON_L de-asserted to V_1 disabled				1	ms
$t_{PSON\_L\ PWOK\_H}$	Delay PSON_L de-asserted to PWOK_H de-asserted				4	ms
$t_{V1\ off}$	Time V_1 is kept off after leaving regulation			1		s
$t_{VSB\ off}$	Time V_{SB} is kept off after leaving regulation			1		s

8.10 LED INDICATOR

The front-end has one front LED showing the status of the supply. The LED is bi-colored: green and amber, and indicates DC input and DC output power presence and warning or fault conditions. *Table 1* lists the different LED status.

OPERATING CONDITION [1]	LED SIGNALING
No DC output or DC input in UV condition, V_{SB} not present from paralleled power supplies	Off
PSON_L High	Blinking Green 1 Hz
No DC output or DC input in UV condition, V_{SB} present from paralleled power supplies V_1 or V_{SB} out of regulation Over temperature shutdown Output over voltage shutdown (V_1 or V_{SB}) Output over current shutdown (V_1 or V_{SB}) Fan error (>15%)	Solid Amber
Over temperature warning Minor fan regulation error (>5%, <15%)	Blinking Amber 1Hz
Firmware bootloading in process	Blinking Green 2 Hz
Outputs V1 and VSB in regulation	Solid Green

[1] The order of the criteria in the table corresponds to the testing precedence in the controller.

Table 1. LED Status

9. I2C / POWER MANAGEMENT BUS COMMUNICATION

The PET front-end is a communication Slave device only; it never initiates messages on the I²C / SMBus by itself.

The communication bus voltage and timing is defined in *Table 2* further characterized through:

- The SDA/SCL IOs use 3.3 V logic levels
- External pull-up resistors on SDA/SCL required for correct signal edges
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

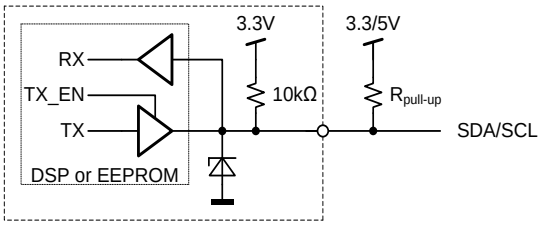


Figure 14. Physical layer of communication interface

Communication to the DSP or the EEPROM will be possible as long as the input DC voltage is provided. If no DC is present, communication to the unit is possible as long as it is connected to a life VSB output (provided e.g. by the redundant unit). If only V1 is provided, communication is not possible.

PARAMETER	DESCRIPTION	CONDITION	MIN	MAX	UNIT
SCL / SDA					
V_{iL}	Input low voltage		-0.5	1.0	V
V_{iH}	Input high voltage		2.3	3.5	V
V_{hys}	Input hysteresis		0.15		V
V_{oL}	Output low voltage	3 mA sink current	0	0.4	V
t_r	Rise time for SDA and SCL		$20+0.1C_b$[2]	1000	ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < C_b[2] < 400 pF	$20+0.1C_b$[2]	300	ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10	10	µA
C_i	Internal Capacitance for each SCL/SDA			50	pF
f_{SCL}	SCL clock frequency		0	100	kHz
$R_{pull-up}$	External pull-up resistor	f_{SCL} ≤ 100 kHz		1000 ns / C_b[2]	Ω
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0		µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0		µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0	3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250		ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0		µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	5		ms

[2] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

Table 2. I2C / SMBus Specification

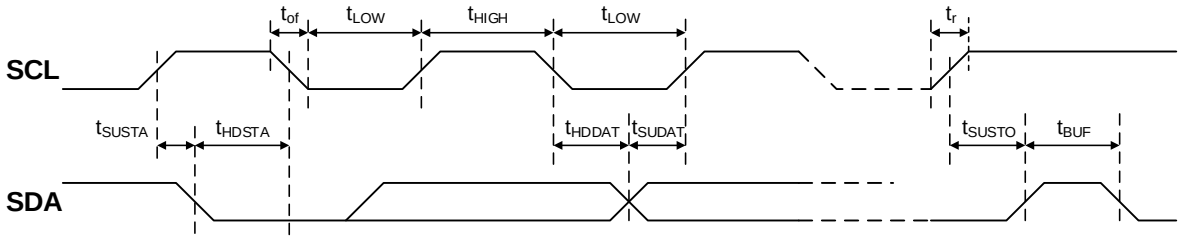


Figure 15. I²C / SMBus Timing

9.1 ADDRESS SELECTION

The address for I2C communication can be configured by pulling address input pins A1 and A0 either to GND (Logic Low) or leave them open (Logic High). An internal pull up resistor will cause the A1 / A0 pin to be in High Level if left open.
A fixed addressing offset exists between the Controller and the EEPROM.

A2[3]	A1	A0	I2C Address[4]	
			Controller	EEPROM
0	0	0	0xB0	0xA0
0	0	1	0xB2	0xA2
0	1	0	0xB4	0xA4
0	1	1	0xB6	0xA6
1	0	0	0xB8	0xA8
1	0	1	0xBA	0xAA
1	1	0	0xBC	0xAC
1	1	1	0xBE	0xAE

[3] A2 will be implemented in future
[4] The LSB of the address byte is the R/W bit.

Table 3. Address and protocol encoding

9.2 SMBALERT_L OUTPUT

The SMBALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. It is asserted (pulled Low) at Shutdown or Warning events such as reaching temperature warning/shutdown threshold of critical component, general failure, over-current, over-voltage, under-voltage or low-speed of failed fan. This signal may also indicate the power supply is operating in an environment exceeding the specified limits.
The SMBAlert signal is asserted simultaneously with the LED turning to solid amber or blinking amber.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
SMB_ALERT_L						
V_{ext}	Maximum External Pull up Voltage				12	V
I_{OH}	Maximum High Level Leakage Current	No Failure or Warning condition, V_O = 12 V			10	µA
V_{OL}	Output Low Level Voltage	Failure or Warning condition, I_{sink} < 4 mA	0		0.4	V
$R_{pull\ up}$	Internal Pull up Resistor to internal 3.3 V			4.7K		
I_{OL}	Maximum Sink Current	V_O < 0.4 V			4	mA

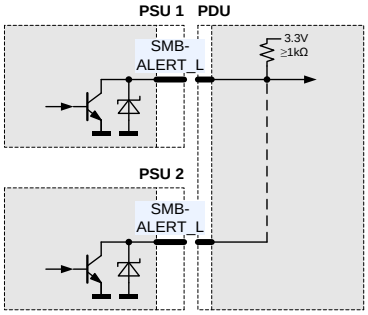


Figure 16. SMBALERT_L connection

9.3 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I²C bus physical layer (see *Figure 17*) and can be accessed under different addresses, see ADDRESS SELECTION. The SDA/SCL lines are connected directly to the controller and EEPROM which are supplied by internal 3.3 V.
The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

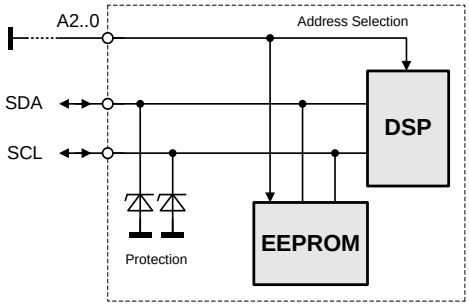


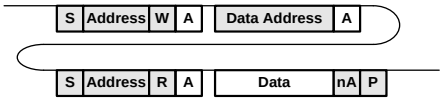
Figure 17. I2C Bus to DSP and EEPROM

9.4 EEPROM Protocol

The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE
The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

READ
The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



9.5 POWER MANAGEMENT BUS PROTOCOL

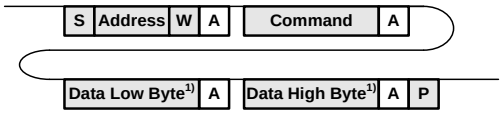
The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org.

Power Management Bus command codes are not register addresses. They describe a specific command to be executed. The PET750-12-050 supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

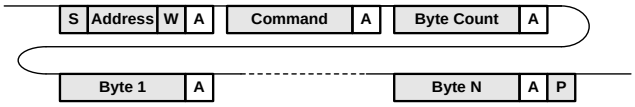
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



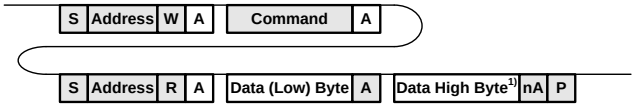
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes. See PET750-12-050ND Power Management Bus Communication Manual for further information.



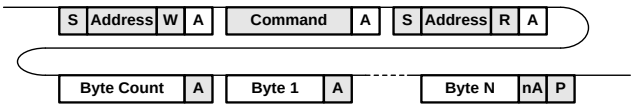
READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



1) Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes. See PET750-12-050ND Power Management Bus Communication Manual for further information.



9.6 GRAPHICAL USER INTERFACE

The Bel Power Solutions provides with its "I²C Utility" a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PET750-12-050ND Front-End.
The utility can be downloaded on: **belfuse.com/power-solutions** and supports both the PSMI and Power Management Bus protocols.
The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view, the power supply can be controlled and monitored.
If the GUI is used in conjunction with the VRA.00335.0 Evaluation Board it is also possible to control the PSON_L pin(s) of the power supply.
Further there is a button to disable the internal fan for approximately 10 seconds. This allows the user to take input power measurements without fan consumptions to check efficiency compliance to the Climate Saver Computing Platinum specification.

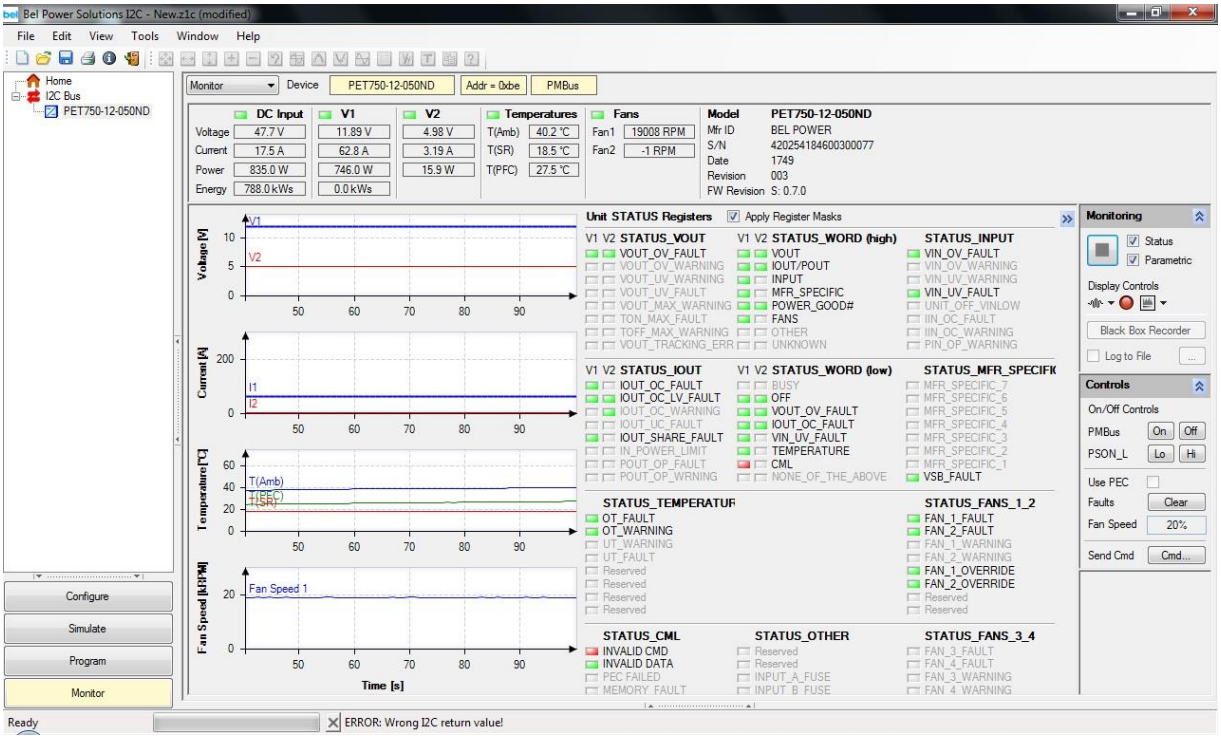


Figure 18. Monitoring dialog of the I2C Utility

10. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PET750-12-050ND is provided with a rear to front airflow, which means the air enters through the DC-output of the supply and leaves at the DC-inlet. The PET750-12-050ND power supply has been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

The PET750-12-050ND provides access via I^2C to the measured temperatures of in total 6 sensors within the power supply, see *Table 4*. The microprocessor is monitoring these temperatures and if warning threshold of one of these sensors is reached it will set fan to maximum speed. If temperatures continue to rise above shut down threshold the main output V_1 (or V_{SB} if auxiliary converter is affected) will be disabled. At the same time, the warning or fault condition is signalized accordingly through LED, PWOK_H and SMBALERT_L.

TEMPERATURE SENSOR	DESCRIPTION / CONDITION	POWER MANAGEMENT BUS REGISTER	WARNING THRESHOLD	SHUT DOWN THRESHOLD
Inlet air temperature	Sensor located on control board close to DC end of power supply	Ox8E	57°C	60°C
Synchronous rectifier	Sensor located on secondary side of DC/DC stage	0x8D	82°C	85°C

Table 4. Temperature sensor location and thresholds

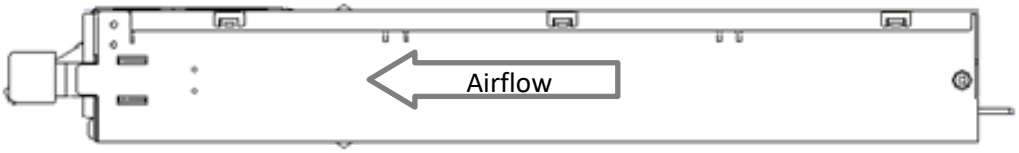


Figure 19. Airflow direction

11. ELECTROMAGNETIC COMPATIBILITY

11.1 IMMUNITY

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LED, connector body)	A
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	A
Radiated Electromagnetics Filed	IEC / EN 61000-4-3, 3 V/m, 1 kHz/80% Amplitude Modulation, 80 MHz ... 1 GHz	A
Burst	IEC / EN 61000-4-4, Level 3 DC input port ±1 kV, 1 minute DC output port ±0.5kV, 1 minute	B
Surge	IEC / EN 61000-4-5 Common mode: ±1 kV Differential mode ±1 kV	A
RF Conducted Immunity	IEC / EN 61000-4-6, 3 Vrms, CW, 0.15 … 80 MHz	A

11.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN 55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, single power supply	Class A
Radiated Emission	EN 55022 / CISPR 22: 30 MHz … 1 GHz, QP, single power supply	Class A

12. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	NOTE
Agency Approvals	UL 60950-1 2nd Edition CAN/CSA-C22.2 No. 60950-1-07 2nd Edition IEC 60950-1: 2005 EN 60950-1: 2006 NEMKO	
Isolation Strength	Input plus to chassis; 1414 V for 1 minute	Basic
	Input minus to chassis; 1414 V for 1 minute	Basic
	Output to chassis	Function
Creepage / Clearance	Primary to chassis (PE) Primary to secondary	>2 mm

13. ENVIRONMENTAL

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
TA	Ambient Temperature	Up to 1'000 m ASL	0		+50	°C
		Linear derating from 1'000 to 3'048 m ASL			+40	°C
TAext	Extended Temp. Range				65	°C
TS	Storage Temperature	Non-operational	-20		+70	°C
	Altitude	Operational, above Sea Level	-		3'048	m
		Non-operational, above Sea Level	-		10'600	m
	Shock	Per IPC9592B (CLASS 1)				
	Vibration	Per IPC9592B (CLASS 1)				
	Acoustical Noise	Distance 1 meter, 25°C, 50% Load			46	dBA

14. RELIABILITY

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
MTBF	Mean time to failure	According Telcordia SR-332; Ground Benign T_A = 25°C, Vi = -48 Vdc, 0.5 · I1 nom, ISB nom	300			kh
	Expected life time	T_A = 25°C, V_i = -48 Vdc, 0.7 · $I_{1\ nom}$, $I_{SB\ nom}$	5			years

15. MECHANICAL

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Dimensions	Width		50.5		mm
		Heigth		40		mm
		Depth		300		mm
m	Weight			900		g

Top and side view with the connector added

Dimensions in mm, tolerance unless otherwise stated: 0.5-30: ±0.3; 30-120: ±0.4; 120-400: ±0.5

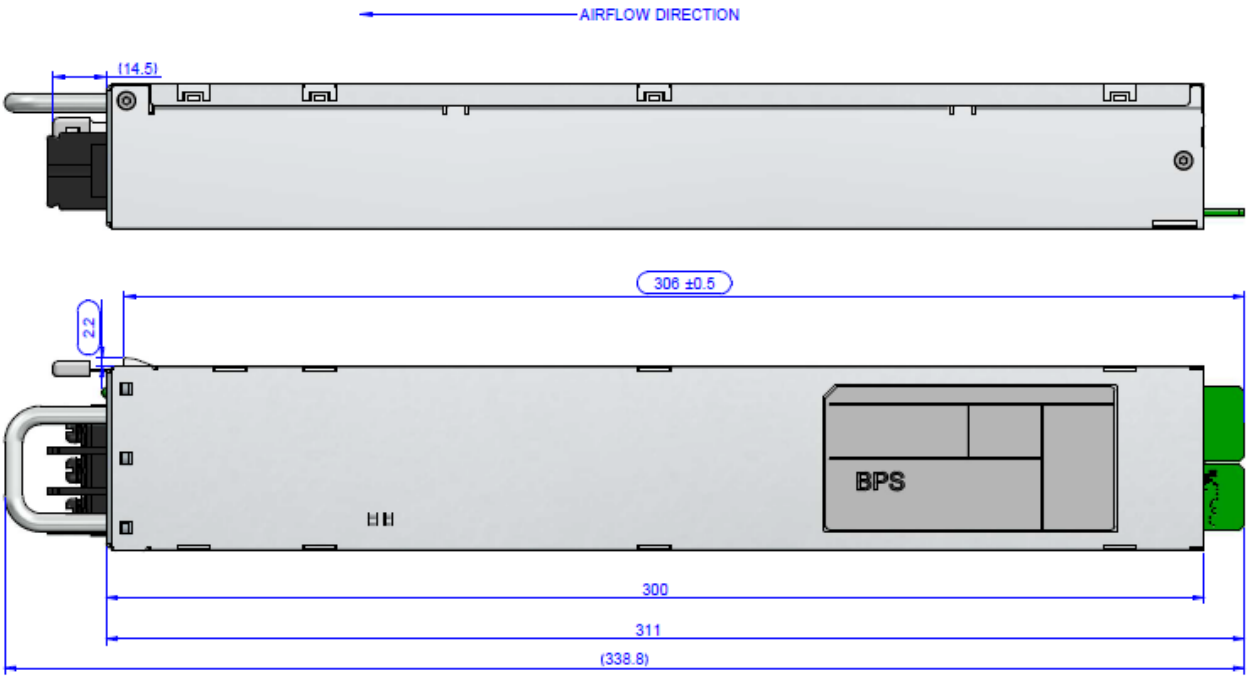


Figure 20. Mechanical Drawing-Side/Top View

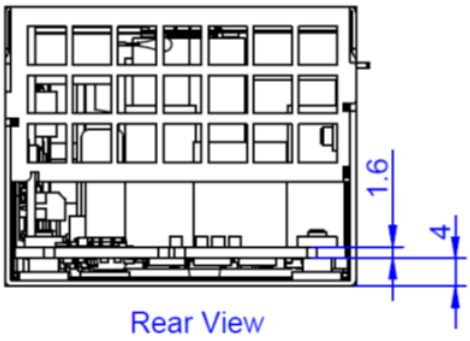


Figure 21. Front View

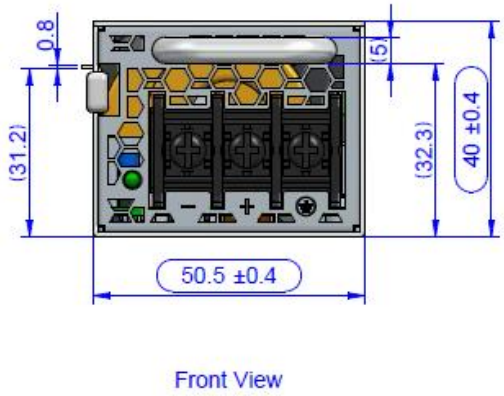


Figure 22. Rear View

16. CONNECTIONS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
DC input connector	Screw terminal block Supplier: DINKLE ENTERPRISE, MPN: DT-66-B11W-03				
DC input power cord requirement	Wire size		12		AWG
DC output connector	16 power contacts, 24 signal contacts Supplier FCI(Amphenol), MPN: 10118868-003LF				

For the pin assignment of DC output connector (PCB card edge), please refer to Figure 23 and Table 5.

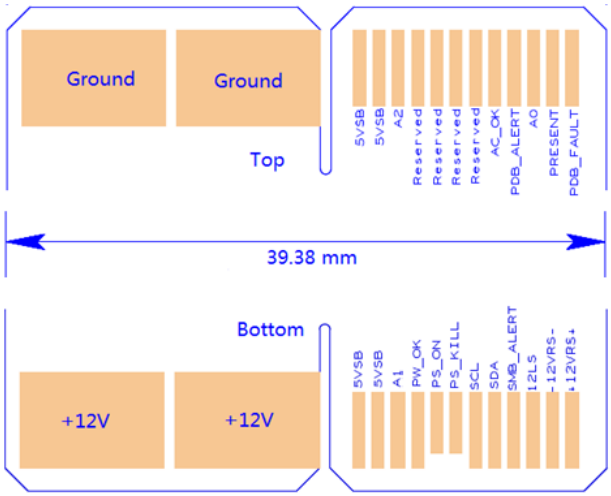
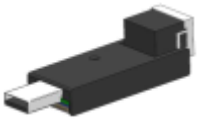
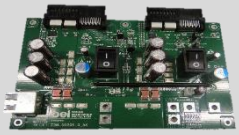


Figure 23. Pin Assignment of DC Output Connector (PCB card edge)

PIN	DESCRIPTION
+12V	12V power output
GND	Grounding
$5V_{SB}$	5V standby power
A0	I2C Address
A1	I2C Address
A2	I2C Address
PW_OK	Power Good Output. Signal is pulled HIGH to indicate all outputs ok.
PS_ON	Module PS_ON Remote control power On/Off (Pulled LOW=POWER ON)
PS_KILL	Activate PSU by hot-plug activity
SCL	I2C CLOCK
SDA	I2C DATA
PDB_ALERT	To receive ALERT signal from system, If signal is pulled LOW, the unit internal fan will be forced to run at maximum speed, This signal is inactive at standby mode.
SMB_ALERT	SMB Alert signal output: active-low
12LS	12V Load Share
PRESENT	This pin is grounded with a 47R resistor. To indicate a power has been plugged in.
12VRS+	12V Remote sense
12VRS-	12V Remote sense return
PDB_FAULT	To receive a FAULT signal. Power shall be shut down if this pin is pulled HIGH.
DC_OK	DC input OK signal: active-high

Table 5. Output Pin Assignment

17. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	**I²C Utility** Windows XP/Vista/7 compatible GUI to program, control and monitor PET750-12-050ND Front-Ends (and other I²C units)	TBD	belfuse.com/power-solutions
	**USB to I²C Converter** Master I²C device to program, control and monitor I²C units in conjunction with the *I²C Utility*	ZM-00056	belfuse.com/power-solutions
	**Evaluation Board** Connector board to operate PET750-12-050ND. Includes an on-board USB to I²C converter (use *I²C Utility* as desktop software).	VRA.00335.0	belfuse.com/power-solutions

18. REVISION HISTORY

DATE	REVISION	ISSUE	PREPARED BY	APPROVED BY
2017/02/24	Preliminary	First release	XF Yang	Mike Chen
2017/09/02	-001 Release for DVT	Update some parameters based on EVT test result	XF Yang	Mike Chen
2017/10/27	-002	1, update Radiated Electromagnetics Filed and RF Conducted Immunity 2, update vibration and shock specification	XF Yang	Mike Chen
2018/01/22	-003	1, update DC drop without V_{SB} leaving regulation from 10msecs to 20msecs 2, update Burst to change DC input port from +/-2Kv to +/-1Kv; add DC output port test of +/-0.5KV	Christian Cruz	Mike Chen
2018/04/11	AA	Release to AA	Christian	Mike Chen