AK9240

AFE with Dual 12-Bit 1MSPS SAR ADC

1. General Description

The AK9240 is an Analog Front End with 12-bit 1MSPS A/D converter. It integrates a programmable gain amplifier (PGA) that is able to select the input current and the input voltage realizing to control the input range. An LED driver and auto power control circuits are also integrated, making the device suitable for compact optical encoders. The AK9240 is housed in a space-saving 20-pin QFN package.

2. Features

- ☐ Simultaneous Sampling 12-bit SAR A/D Converter
- ☐ Sampling Rate: 1MSPS
- ☐ Differential Inputs
- ☐ Current Input or Voltage Input Selectable
- ☐ PGA Function
- ☐ LED driver
- ☐ Automatic Power Control Circuit
- ☐ Low Pass Filter
- ☐ S/(N+D): 71dB (Typ.) at 10kHz Input.
- ☐ INL: ±1.25LSB (Max.)
- ☐ DNL: ±1.0LSB (Max.)
- ☐ Power Consumption: 17 mA (fs= 1MSPS)
- ☐ Power Supply: 2.7 ~ 5.5V
- ☐ Operational Temperature Range (Ta): -40 ~ 105ºC
- ☐ Small Package: 20-pin QFN (3mm x 3mm)

3. Table of Contents

4. Block Diagram

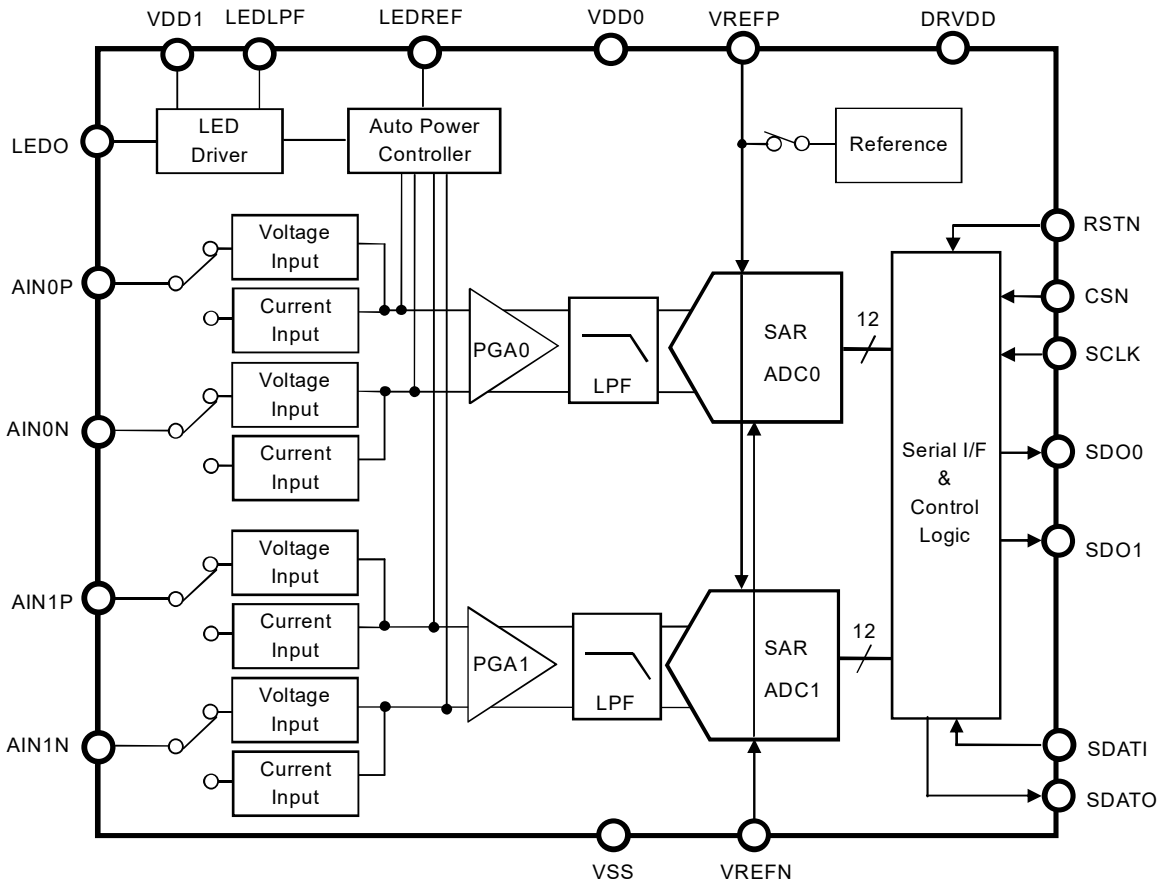
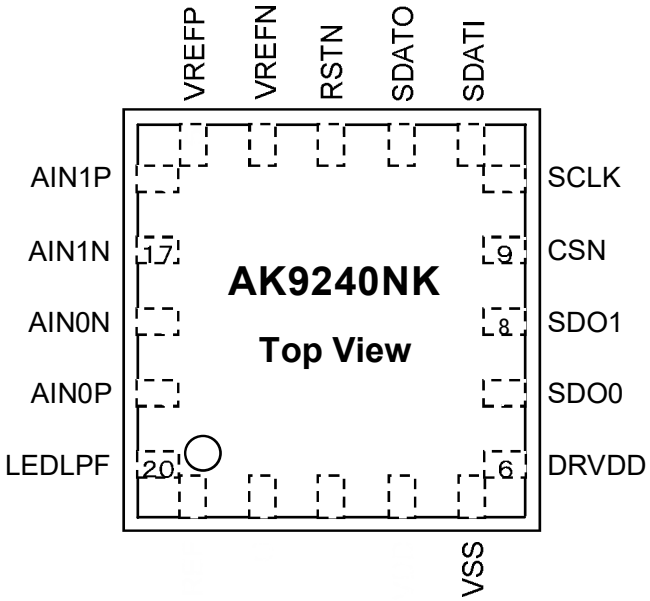


Figure 1. AK9240 Block Diagram

5. Pin Configurations and Functions

■ Pin Layout



■ Pin Functions

Pin No.	Pin Name	I/O	Function
1	LEDREF	I	Reference Voltage Input Pin at APC / LED mode.
2	LEDO	O	LED Drive Current Output Pin.
3	VDD1	-	Analog Power Supply Pin (3.0V/5.0V).
4	VDD0	-	Analog Power Supply Pin (3.0V/5.0V).
5	VSS	-	Ground Pin.
6	DRVDD	-	Digital Power Supply Pin (3.0V/5.0V).
7	SDO0	O	ADC0 Serial Data Output Pin.
8	SDO1	O	ADC1 Serial Data Output Pin.
9	CSN	I	Chip Select Pin.
10	SCLK	I	Clock Input Pin.
11	SDATI	I	Serial Data Input Pin. (* 2) Pin is connected to VSS by internal resistor.(typ. 100kΩ)
12	SDATO	O	Serial Data Output Pin. (* 2)
13	RSTN	I	Reset Pin. Pin is connected to VSS by internal resistor.(typ. 100kΩ)
14	VREFN	I	ADC Low level Voltage Reference Input. This pin must be connected to VSS. Pin is connected to VSS by internal resistor.(typ. 100kΩ)
15	VREFP	I/O	ADC High level Voltage Reference Input / Output. (* 3) Normally decoupled to VSS with a capacitor (1μF or more). When PMREF bit =”0”, VREFP pin has internal pull-down resistor, nominally 100kΩ.
16	AIN1P	I	ADC1 Positive Analog Input Pin.
17	AIN1N	I	ADC1 Negative Analog Input Pin.
18	AIN0N	I	ADC0 Negative Analog Input Pin.
19	AIN0P	I	ADC0 Positive Analog Input Pin.
20	LEDLPF	O	Capacitor connecting Pin for APC Loop Band Adjustment. When PMLED bit =”0”, LEDLPF pin has internal pull-down resistor, nominally 80kΩ. (* 4)(* 5)

Notes:
* 1. Do not open the digital input pins (CSN, SCLK, SDATI, RSTN).
* 2. The SDATI and the SDATO pins can be short-circuited. (Figure13)
* 3. The internal reference is designed for A/D conversion of AK9240, external circuit unable to drive directly.
* 4. A capacitor (0.1μF or more) must be connected to the LEDLPF pin when using the LED driver.
* 5. An over current may be output from the LEDO pin if an external voltage is input to the LEDLPF pin.

■ Handling of Unused Pin

Unused I/O pins must be connected appropriately.

Pin Name	Setting
AIN0P, AIN0N	(Open or VSS) & PMAD0 bit= “0”
AIN1P, AIN1N	(Open or VSS) & PMAD1 bit= “0”
LEDO	Open
LEDREF	VSS
LEDLPF	Open or VSS
VDD1	VDD0

■ Output Pin Statuses in Power-down Mode

Pin No.	Pin Name	I/O	RSTN = L or Individual Power Down Setting	State
1	LEDREF	I	-	-
2	LEDO	O	PMLED bit = “0”	Hi-Z
3	VDD1	-	-	-
4	VDD0	-	-	-
5	VSS	-	-	-
6	DRVDD	-	-	-
7	SDO0	O	PMAD0 bit = “0”	Hi-Z
8	SDO1	O	PMAD1 bit = “0”	Hi-Z
9	CSN	I	-	-
10	SCLK	I	-	-
11	SDATI	I	-	-
12	SDATO	O	-	Hi-Z
13	RSTN	I	-	-
14	VREFN	I	-	-
15	VREFP	I/O	PMREF bit = “0”	Connect to VSS via 100kΩ
16	AIN1P	I	-	-
17	AIN1N	I	-	-
18	AIN0N	I	-	-
19	AIN0P	I	-	-
20	LEDLPF	O	PMLED bit = “0”	Connect to VSS via 80kΩ

6. Absolute Maximum Ratings

(VSS = VREFN = 0V; * 6)

Parameter	Symbol	Min.	Max.	Unit
Power Supply1	VDD0	-0.3	+6.2	V
Power Supply2	VDD1	-0.3	+6.2	V
Power Supply3	DRVDD	-0.3	+6.2	V
Analog Input Current (AINxP, AINxN)	AIN	-	±10	mA
Digital Input Current	DIN	-	±10	mA
Analog Input Voltage	AVIN	-0.3	VDD0+0.3	V
Digital Input Voltage	DVIN	-0.3	DRVDD+0.3	V
Storage Temperature	Tstg	-65	150	ºC

Note:
* 6. All voltages are with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS=0V; * 7)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply1	VDD0	2.7	-	5.5	V
Power Supply2	VDD1	2.7	-	5.5	V
Power Supply3	DRVDD	2.7	-	5.5	V
Ambient Operating Temperature	Ta	-40	-	105	ºC

Note:
* 7. All voltages are for ground (VSS).
* 8. Connect the exposure tab on the back of the package to ground.

Caution: In normal mode, use VDD 0 = VDD 1 ≥ DRVDD.
Caution: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Analog Characteristics

(Ta = -40~105ºC; VDD0= VDD1= 5V, DRVDD= 3V; fs= 1MHz, VREFP= 2.5V(external); unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
Resolution		12	-	-	bit
No Missing Codes		12	-	-	bit
Sampling Dynamics					
Data Rate		-	-	1000	kSPS
Acquisition time		325	-	-	ns
Invalid conversions time after power up		-	-	5	ms
Low Pass Filter Characteristics					
Bandwidth at -3dB	FIL bit= “1”	50	100	150	kHz
	FIL bit= “0”	125	250	375	kHz
Reference Voltage Output					
Reference output voltage	VREFV bit= “0”	2.25	2.5	2.75	V
	VREFV bit= “1”	1.35	1.5	1.65	V
Reference output voltage drift		-	±70	-	ppm/°C
Invalid time after power up (* 1)		-	-	1	ms
Reference Voltage Input					
Reference input voltage		0.45 × VDD0	0.5 × VDD0	0.55 × VDD0	V
Input resistance		22.5	28	-	kΩ
Input Capacitance		-	35	-	pF
Input Current		-	90	135	μA
VDD0 Monitor Circuit					
Battery Backup Mode Switching Voltage: Vdet		0.3 ×VDD1	0.5 ×VDD1	0.7×VDD1	V
Hysteresis Width		100	-	-	mV
Power Supply Current (* 2)					
Normal Voltage mode Operation fin = 10kHz, fs = 1MSPS (* 3)	VDD0	-	16	21	mA
	VDD1	-	-	1	μA
	DRVDD	-	1	3	mA
Current mode Operation @APC fin = 1kHz, fs = 1MSPS (* 4)	VDD0	-	18.5	25	mA
	VDD1		3	8	mA
	DRVDD	-	1	3	mA
Current mode Operation @LED PD fin = 1kHz, fs = 1MSPS (* 5.)	VDD0	-	17.5	23.5	mA
	VDD1	-	-	1	μA
	DRVDD	-	1	3	mA
Power-Down State (* 6)	VDD0	-	-	1	μA
	VDD1	-	-	1	μA
	DRVDD	-	-	1	μA
Power-Down State (* 7)	VDD0	-	40	80	μA
	VDD1	-	-	1	μA
	DRVDD	-	6	20	μA
Battery Backup Mode (* 8)	VDD1	-	-	1	μA

Notes: * 1. VREFP pin decoupled to VSS with a 1μF capacitor.
* 2. VDD0=VDD1= 5V, DRVDD= 3V, Load Capacitance =30pF. except the LED driver output current:ILED.
* 3. MOD bit= “0”, PMREF bit= “1”, PMLED bit= “0”, PMAPC bit= “0”, PMAD1 bit= “1”, PMAD0 bit= “1”
* 4. MOD bit= “1”, PMREF bit= “1”, PMLED bit= “1”, PMAPC bit= “1”, PMAD1 bit= “1”, PMAD0 bit= “1” Gain bit =111”, LEDREF = 0.5V
* 5. MOD bit= “1”, PMREF bit= “1”, PMLED bit= “0”, PMAPC bit= “0”, PMAD1 bit= “1”, PMAD0 bit= “1”
* 6. RSTN= “L”
* 7. MOD bit= “0”, PMREF bit= “0”, PMLED bit= “0”, PMAPC bit= “0”, PMAD1 bit= “0”, PMAD0 bit= “0” RSTN= “H”, SDATI= “H”, SCLK= “H”, CSN= “L”
* 8. VDD0= 0V, DRVDD= 0V

■ **Voltage Input Mode: MODE bit= "0"**

(Ta = -40~105°C; VDD0= VDD1= 5V, DRVDD= 3V; fs=1MHz; Differntial Input;unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
Input Voltage Range (AINP,AINN) (* 9)	Differential Input	$VCM - \frac{VREFP}{2\times MAG}$	-	$VCM + \frac{VREFP}{2\times MAG}$	V
	Pseudo Differential Input	$VCM - \frac{VREFP}{MAG}$	-	$VCM + \frac{VREFP}{MAG}$	V
Common-Mode Voltage Range	VCM	0.45 × VDD0	-	0.55 × VDD0	V
Input Leakage Current		-	-	±1	μA
Input Capacitance		-	5	-	pF
Input Impedance		1	-	-	MΩ
Integral Nonlinearity (INL) Error (* 10)		-1.25	-	+1.25	LSB
Differential Nonlinearity (DNL) Error		-1	-	+1	LSB
Gain Error Channel Mismatch (ch0&ch1)		-	-	±2.5	%
Gain Error Temperature drift		-	±95	-	ppm/°C
Offset Error	AINxP=AINxN=VDD0/2	-	-	±10	mV
Offset Error Chanel Mismatch (ch0&ch1)	AINxP=AINxN=VDD0/2	-	-	±14	mV
Offset Error Temperature drift	AINxP=AINxN=VDD0/2	-	±8	-	μV/°C
PGA Characteristics					
Gain (* 9)	GAIN bit= "000"	13	14	15	dB
	GAIN bit= "001"	16	17	18	dB
	GAIN bit= "010"	19	20	21	dB
	GAIN bit= "011"	22	23	24	dB
	GAIN bit= "100"	25	26	27	dB
	GAIN bit= "101"	28	29	30	dB
	GAIN bit= "110"	31	32	33	dB
	GAIN bit= "111"	34	35	36	dB
Dynamic Characteristics VDD0= 5V (* 11)					
THD		-	-80	-	dB
S/N		67.5	72	-	dBFS
S/(N+D)		67	71	-	dBFS
SFDR		-	83	-	dB
CMRR		60	66	-	dB
Channel to Channel Isolation		-	-80	-	dB
Dynamic Characteristics VDD0= 3V (* 12)					
THD		-	-77	-	dB
S/N		65.5	70	-	dBFS
S/(N+D)		65	69	-	dBFS
SFDR		-	80	-	dB
CMRR		60	66	-	dB
Channel to Channel Isolation		-	-80	-	dB

Notes:

* 9. MAG = 10 ^ (Gain[dB] /20)
* 10. GAIN bit= "011", VREFP= 2.5V (external)
* 11. (AINxP – AINxN)x Gain= -1dBFS, fin= 10kHz, GAIN bit= "011", FIL bit= "0", VREFP= 2.5V(external)
* 12. (AINxP – AINxN)x Gain= -1dBFS, fin= 10kHz, GAIN bit= "011", FIL bit= "0", VREFP= 1.5V(external)

■ **Current Input Mode: MODE bit= "1"**

(Ta = -40~105°C; VDD0= VDD1= 5V, DRVDD= 3V; fs=1MHz; unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
Input Current Range		0	-	$+\frac{VREFP}{I\text{-}V\ Gain}$	μA
AINx pin External Input Load Capacitance		-	-	100	pF
AINx pin Bias Voltage	AINxP/AINxN=Open	-	0.6 × VDD0	-	V
AINxP-AINxN Input Resistance Mismatch		-	-	±1	%
Integral Nonlinearity (INL) Error (* 21.)		-1.25	-	+1.25	LSB
Differential Nonlinearity (DNL) Error		-1	-	+1	LSB
Gain Error Channel Mismatch (ch0 & ch1)		-	-	±2.5	%
Gain Error Temperature drift		-	±170	-	ppm/°C
Offset Error	AINxP/AINxN=Open	-	-	±0.8	μA
Offset Error Chanel Mismatch (ch0 & ch1)	AINxP/AINxN=Open	-	-	±1.1	μA
Offset Error Temperature drift	AINxP/AINxN=Open	-	±0.8	-	nA/°C
PGA Characteristics					
I-V Gain	GAIN bit= "000"	Typ. x 0.8	65	Typ. x 1.2	kΩ
	GAIN bit= "001"		91		kΩ
	GAIN bit= "010"		130		kΩ
	GAIN bit= "011"		183		kΩ
	GAIN bit= "100"		130		kΩ
	GAIN bit= "101"		183		kΩ
	GAIN bit= "110"		260		kΩ
	GAIN bit= "111"		365		kΩ
Dynamic Characteristics VDD0= 5V (* 22.)					
THD		-	-80	-	dB
S/N		65.5	70.5	-	dBFS
S/(N+D)		65	69.5	-	dBFS
SFDR		-	80	-	dB
Channel to Channel Isolation		-	-80	-	dB
Dynamic Characteristics VDD0= 3V (* 23)					
THD		-	-75	-	dB
S/N		62.5	67.5	-	dBFS
S/(N+D)		62	66.5	-	dBFS
SFDR		-	80	-	dB
Channel to Channel Isolation		-	-80	-	dB

Notes:

* 21. GAIN bit= "111", VREFP= 2.5V (external)
* 22. (AINxP/AINxN)x Gain= -1dBFS, fin= 10kHz, GAIN bit= "111", FIL bit= "0", VREFP= 2.5V (external)
* 23. (AINxP/AINxN)x Gain= -1dBFS, fin= 10kHz, GAIN bit= "111", FIL bit= "0", VREFP= 1.5V (external)
* 24. Outgoing current from the AK9240 is defined as "-" polarity, and incoming current to the AK9240 is defined as "+" polarity.

■ **Current input mode (RINモード) : MODE bit= "1"**

(Unless otherwise noted , Ta = -40 ~ 105°C; VDD0= VDD1= 5V, DRVDD= 3V, RIN=100kΩ; fs=1MHz)

Parameter		Min.	Typ.	Max.	Unit
Input Voltage Range (VINxP,VINxN)		$VCM - \frac{VREFP \times RIN}{2 \times I\text{-}V\ Gain}$	-	$VCM + \frac{VREFP \times RIN}{2 \times I\text{-}V\ Gain}$	V
Common-Mode Voltage Range	VCM	0.45 × VDD0	-	0.55 × VDD0	V
Dynamic Characteristics VDD0= 5.0V (* 13)					
THD		-	-80	-	dB
S/N		65.5	70.5	-	dBFS
S/(N+D)		63	69.5	-	dBFS
SFDR		-	80	-	dB
Dynamic Characteristics VDD0= 3.3V (* 14)					
THD		-	-75	-	dB
S/N		62.5	67.5	-	dBFS
S/(N+D)		60	66.5	-	dBFS
SFDR		-	80	-	dB

Notes:

* 13. (VINxP – VINxN) = 3.5Vdiffpp, fin= 1kHz, GAIN bit= "001", FIL bit= "0", VREFP= 2.5V (external)
* 14. (VINxP – VINxN) = 2.5Vdiffpp, fin= 1kHz, GAIN bit= "001", FIL bit= "0", VREFP= 1.5V (external)

Caution This mode must use the setting of GAIN[2:0]bit =001 only.

9. DC Characteristics

■ LED Normal Mode

(Ta = -40 ~105ºC, VDD0 = VDD1 = 2.7 ~ 5.5V, DRVDD = 2.7 ~ 5.5V)

Parameter		Symbol	Min.	Max.	Unit
High-Level Input Voltage	(* 27)	VIH1	0.7 × DRVDD	-	V
Low-Level Input Voltage	(* 27)	VIL1	-	0.3 × DRVDD	V
High-Level Output Voltage (Iout = -1mA)	(* 28)	VOH1	0.8 × DRVDD	-	V
Low-Level Output Voltage (Iout = 1mA)	(* 28)	VOL1	-	0.2 × DRVDD	V
Input Leakage Current	(* 29)	Iin	-	±1	μA

Notes:

* 27. CSN pin, SCLK pin, SDATI pin, RSTN pin
* 28. SDO1 pin, SDO2 pin, SDATO pin
* 29. CSN pin, SCLK pin
* 30. Outgoing current from the AK9240 is defined as “+” polarity, and incoming current to the AK9240 is defined as “-” polarity.

■ Battey Backup Mode

(Ta = -40 ~105ºC, VDD1 = 2.7 ~ 5.5V)

Parameter	Symbol	Min.	Max.	Unit
High-Level Input Voltage (RSTN pin)	VIH2	0.7 × VDD1	-	V
Low-Level Input Voltage (RSTN pin)	VIL2	-	0.3 × VDD1	V

Note:

*31. Serial I/F (CSN pin, SCLK pin, SDO1 pin, SDO2 pin, SDATO pin, SDATI pin) are not available in battery backup mode. The CSN pin, the SCLK pin and the SDATI pin must be fixed to “L” or “H”.

10. LED Driver Characteristics (Normal Mode)

■ APC Mode

(Ta = -40 ~105ºC, VDD0= VDD1= 5V, DRVDD= 3V, LEDO =1.5V)

Parameter		Min.	Typ.	Max.	Unit
LEDREF Input Voltage Range		0.2	-	1.0	V
Gain		98	104	110	dB
Bandwidth	LEDLPF pin= 0.1µF	10	20	30	Hz
Invalid time after power up	LEDLPF pin= 0.1µF	-	20	100	ms
Output Current: ILED		4	-	80	mA
Optical Gain (*32)		-	-	1 / 1500	A/A

Note:
* 32. Optical Gain = Input Current / ILED
Please do not use with Optical Gain higher than the specification value.

■ LED Mode

(Ta = -40 ~105ºC, VDD0= VDD1= 5V, DRVDD= 3V, LEDO =1.5V)

Parameter		Min.	Typ.	Max.	Unit
LEDREF Input Voltage Range		0.2	0.5	0.8	V
Output Current: ILED	LEDREF= 0.8V	45	61	76	mA
	LEDREF= 0.5V	27	39	49	mA
	LEDREF= 0.2V	9	15	21	mA
Maximum Output Current (* 33)		50	80	100	mA
Bandwidth	LEDLPF pin= 0.1µF	10	20	30	Hz
Invalid time after power up	LEDLPF pin= 0.1µF	-	50	150	ms

Note:
* 33. An over current may be output from the LEDO pin if an external voltage is input to the LEDLPF pin.

■ LED Backup Mode

(Ta = -40 ~105ºC, VDD0= VDD1= 5V, DRVDD= 3V, LEDO =1.5V)

Parameter	Min.	Typ.	Max.	Unit
Internal Resistance of LED Driver	60	85	110	Ω

11. LED Driver Characteristics (Battery Backup Mode)

(Ta = -40 ~105ºC, VDD1 = 5V, LEDO =1.5V)

Parameter	Min.	Typ.	Max.	Unit
Internal Resistance of LED Driver	60	85	110	Ω

12. Switching Characteristics

(Ta = -40 ~105°C, VDD0 = VDD1 = 2.7 ~ 5.5V, DRVDD = 2.7 ~ 5.5V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
CSN Clock Frequency		fCSN	-	-	1	MHz
SCLK Clock Frequency		fSCK	0.5	-	20	MHz
SCLK High Pulse Width	tSCK= 1/fSCK	tSCKH	0.4 ×tSCK	-	-	ns
SCLK Low Pulse Width	tSCK= 1/fSCK	tSCKL	0.4 ×tSCK	-	-	ns
CSN "↓" to First SCLK "↓"		tCSS	10	-	-	ns
CSN "↓" to SDOx "0" Delay		tCSD	-	-	30	ns
SCLK "↓" to SDATO Valid Delay		tDCD1	-	-	30	ns
SCLK "↓" to SDOx Valid Delay		tDCD2	-	-	30	ns
16th SCLK "↓" to SDOx "0" Delay		tDCD3	-	-	30	ns
SCLK "↓" to SDATO Valid Hold time		tDCH1	1	-	-	ns
SCLK "↓" to SDOx Valid Hold time		tDCH2	1	-	-	ns
CSN "↑" to SDATO Valid Hold time		tDCH3	1	-	-	ns
SCLK "↑" to SDATI Set Up time		tSU	20	-	-	ns
SCLK "↑" to SDATI Hold time		tHD	20	-	-	ns
Minimum CS pulse		tCS	50	-	-	ns
CSN "↑" to SDATO Hi-Z State		tCCZ1	-	-	50	ns
CSN "↑" to SDOx Hi-Z State		tCCZ2	-	-	50	ns
16th SCLK "↑" to CSN "↑"		tCHH	20	-	-	ns
Input RSTN Low Pulse Width	(* 34)	tRSTN	600	-	-	ns
LEDST "↓" (16th SCLK "↑") to LEDO "↑" Delay	(* 35)	tLR1	-	50	400	ns
LEDST "↑" (16th SCLK "↑") to LEDO "↓" Delay	(* 35)	tLF1	-	20	400	ns
RSTN "↑" to LEDO "↑" Delay	(* 36)	tLR2	-	30	80	ns
RSTN "↓" to LEDO "↓" Delay	(* 36)	tLF2	-	10	80	ns

Notes:
* 34. Normal Mode
* 35. LED Mode/LED Standby Mode
* 36. Battery Backup Mode

■ Timing Diagram

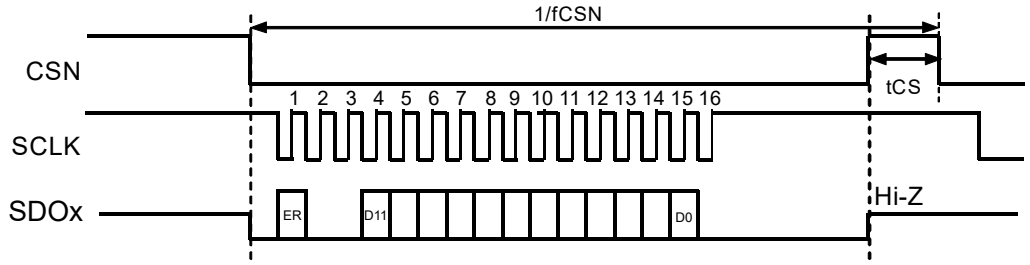


Figure 2. Data Output Timing 1 (SDOT bit = “0”)

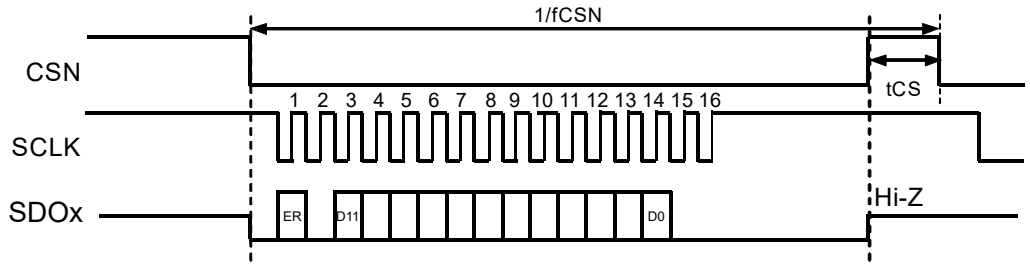


Figure 3. Data Output Timing 2 (SDOT bit = “1”)

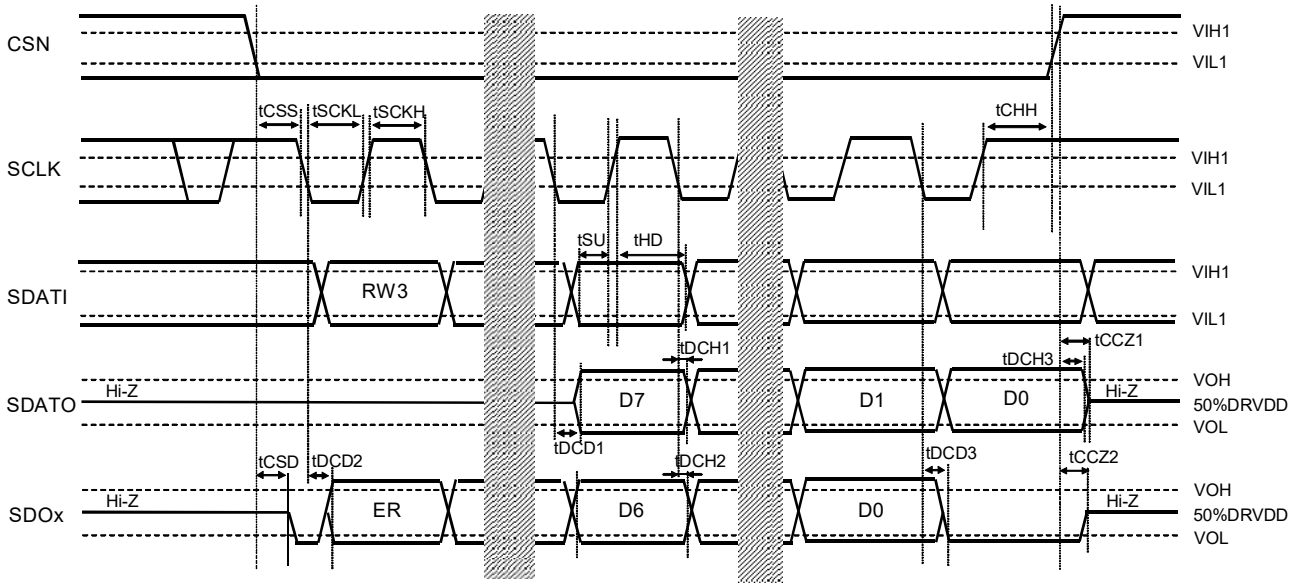


Figure 4. Data Output Timing3

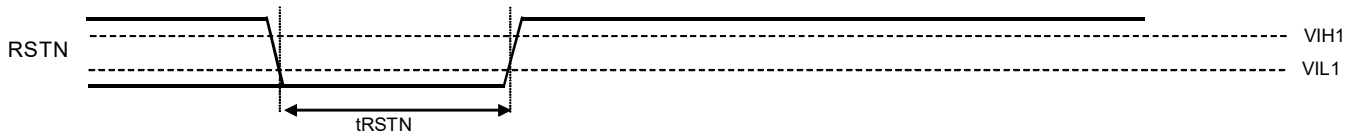


Figure 5. Reset Signal Timing

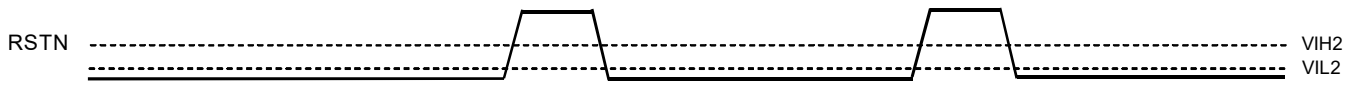


Figure 6. RSTN DC Characteristics in Battery Backup Mode

13. Functional Descriptions

■ Analog Input

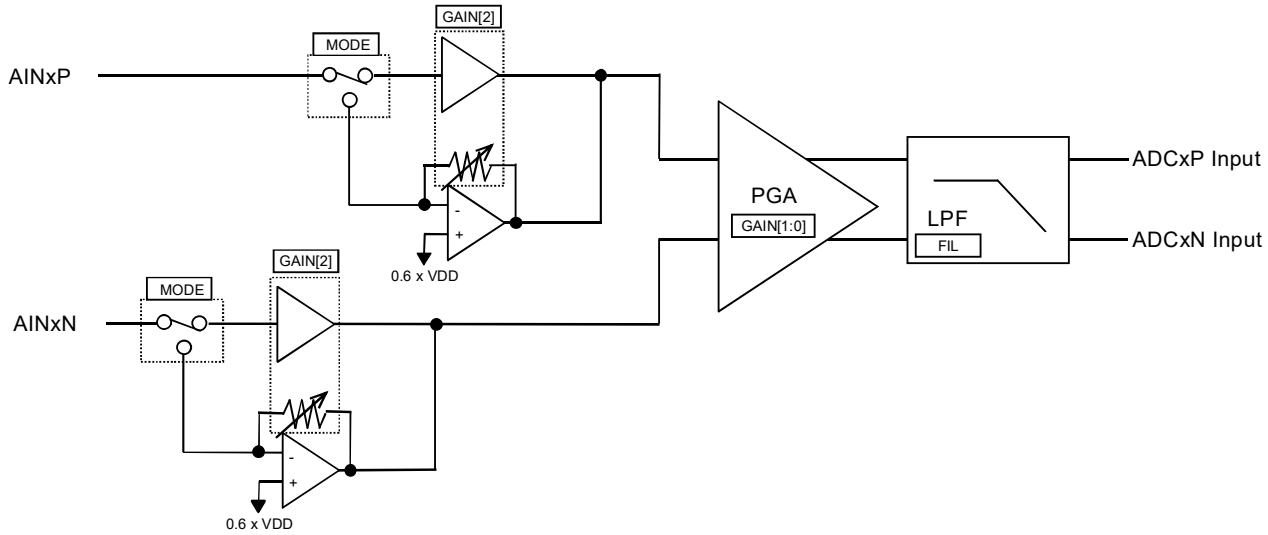


Figure 7. Analog Input

MODE bit selects Current or Voltage Input Mode of the AK9240. (AINxP/AINxN; x= 0 or 1)

Table 1. Mode Setting

MODE bit	Function
0	Voltage Mode
1	Current Mode

(1) Voltage Input Mode (MODE bit= "0")
Internal PGA gain is set by GAIN2-0 bits.

Table 2. PGA Gain Setting

GAIN2 bit	GAIN0 bit	GAIN0 bit	Gain(dB)
0	0	0	14
0	0	1	17
0	1	0	20
0	1	1	23
1	0	0	26
1	0	1	29
1	1	0	32
1	1	1	35

<Example> ADC differential input voltage is about 4Vdiffpp. (VDD0= 5.0V)

Table 3. Gain Setting Examples

MODE bit	GAIN2 bit	GAIN1 bit	GAIN0 bit	Differential Analog Input Range (AINxP/AINxN)
1	0	0	0	2.5V ± 200mV
1	0	0	1	2.5V ±140mV
1	0	1	0	2.5V ± 100mV
1	0	1	1	2.5V ± 70mV
1	1	0	0	2.5V ± 50mV
1	1	0	1	2.5V ± 35mV
1	1	1	0	2.5V ± 25mV
1	1	1	1	2.5V ± 18mV

<Example> ADC pseudo differential input voltage is about 4Vpp. (VDD0= 5.0V, AINxN= 2.5V)

Table 4. Gain Setting Examples

MODE bit	GAIN2 bit	GAIN1 bit	GAIN0 bit	Pseudo Differential Analog Input Range (AINxP)
1	0	0	0	2.5V ±400mV
1	0	0	1	2.5V ± 280mV
1	0	1	0	2.5V ± 200mV
1	0	1	1	2.5V ± 140mV
1	1	0	0	2.5V ± 100mV
1	1	0	1	2.5V ± 70mV
1	1	1	0	2.5V ± 50mV
1	1	1	1	2.5V ± 35mV

(2) Current Input Mode (MODE bit = “1”)

Figure 8 shows an usage example in Current Input Mode.

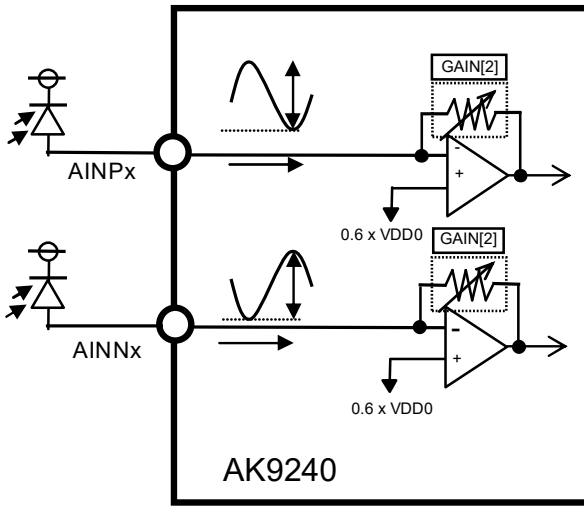


Figure 8. Current Mode Example

Note:

* 37. The current direction should only be incoming to the AK9240 as shown in Figure 8 in Current Input Mode.

I-V gain is set by GAIN2-0 bits

Table 5. PGA Gain Setting

GAIN2 bit	GAIN1 bit	GAIN0 bit	Gain(kΩ)
0	0	0	65
0	0	1	91
1	0	0	130
1	0	1	183
1	1	0	260
1	1	1	365

<Example> ADC differential input voltage is about 4Vdiffpp. (VDD0= 5.0V)

Table 6. Gain Setting Examples

MODE bit	GAIN2 bit	GAIN1 bit	GAIN0 bit	Differential Analog Input Range (AINxP/AINxN)
0	0	0	0	60μAdiffpp
0	0	0	1	44μAdiffpp
0	0	1	0	30μAdiffpp
0	0	1	1	22μAdiffpp
0	1	1	0	15μAdiffpp
0	1	1	1	11μAdiffpp

(3) Current input Mode (RIN MODE) (MODE bit = “1”)

An example of use in current mode (RIN mode) is shown in Figure 9.

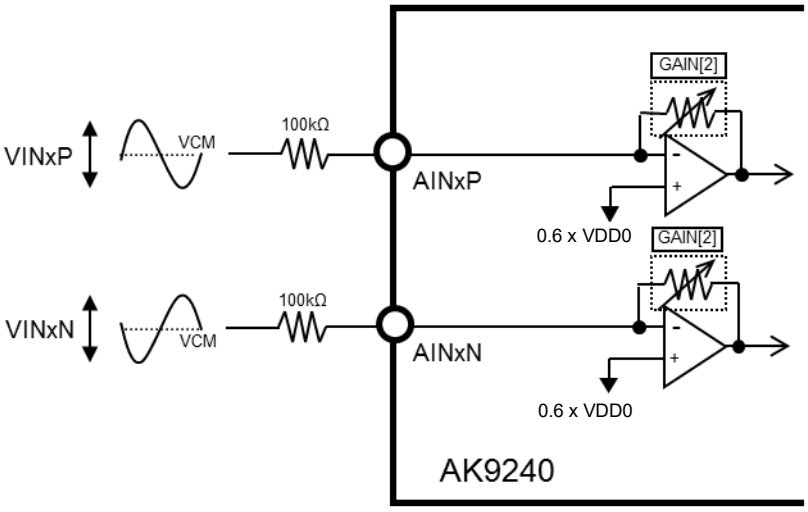


Figure 9. An example of use in current mode (RIN mode)

By connecting an external resistor 100 kΩ in series with the input pins (AINxP, AINxN)
It is possible to input a signal amplitude larger than the voltage input mode.

Caution This mode must use the setting of GAIN[2:0]bit =001 only.

■ Filter Band

The AK9240 has a first order low-pass filter at PGAx block. The cut-off frequency of the low-pass filter is selected by FIL bit.

Table 7. Filter Setting

FIL0 bit	Cut-off Frequency (Typ.)
0	250kHz
1	100kHz

■ ADC Output Code

ADC output format is 2's compliment. The size of LSB is dependent on the gain setting.
The expression of LSB size is shown below.

Full Scale = 2 * (VREFP – VREFN)

1LSB = Full Scale / 4096 [V]

■ Reference Voltage

Table 8. Reference Voltage Setting

VRMOD bit	Function	VREFP In/Output	Note
0	Internal Reference	Output	
1	External Reference	Input	

Table 9. Reference Voltage Setting

VREFV bit	Reference Voltage	VREFP In/Output	Note
0	2.5V	Output	VDD0= 4.5 ~ 5.5V
1	1.5V	Output	VDD0= 2.7 ~ 3.6V

Caution : The internal reference (circuit) is designed for A/D conversion of the AK9240, it can not drive an external circuit directly.

■ Serial Control Interface1 (A/D Conversion Result Output)

The AK9240 starts sampling the input signal by a falling edge of the CSN pin, and the AD conversion starts. Converted data is output from the SDOx pin during the conversion (x= 0 or 1). After a falling edge of the CSN pin, 1-bit ER data is output in synchronization with a falling edge of the SCLK pin. Then, 12-bit A/D conversion data is output in MSB first following 2-bit(SDO bit =”0”) or 1-bit(SDO bit =”1”) “0” data output. The SDO pin data becomes “0” and A/D conversion result output stops on the 16th(SDO bit =”0”) or 15th(SDO bit =”1”) falling edge “↓” of SCLK.
When SCLK of 12 MHz or more is input, it is recommended to capture the ADC output data on a falling edge of SCLK.

The AK9240 transitions to acquisition phase on the first rising edge after the 13th falling edge of SCLK clock.The CSN pin must be set to “H” after the 16th falling edge of SCLK. Normally, the CSN pin should not be set to “H” until “b” timing in Figure10.

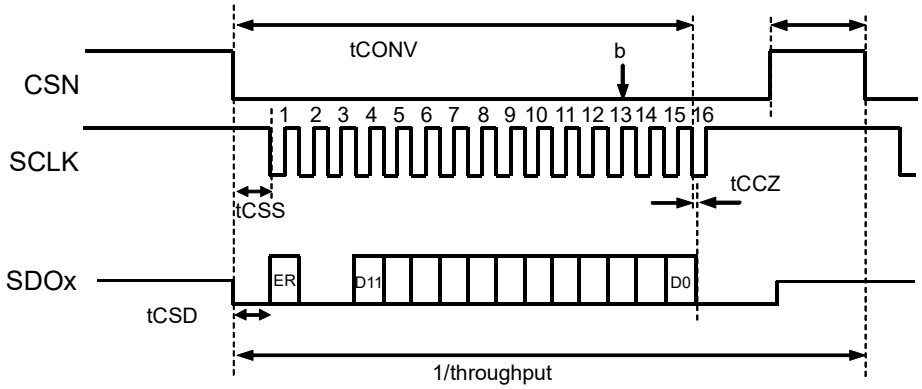


Figure 10. Digital I/F1

AD conversion is stopped and SDO data becomes Hi-Z if the CSN pin is put to “H” during the conversion. At the same time, the AK9240 transitions to acquisition phase. The CSN pin should be set to “L” after waiting the acquisition time (minimum 325nsec) when re-starting sampling.

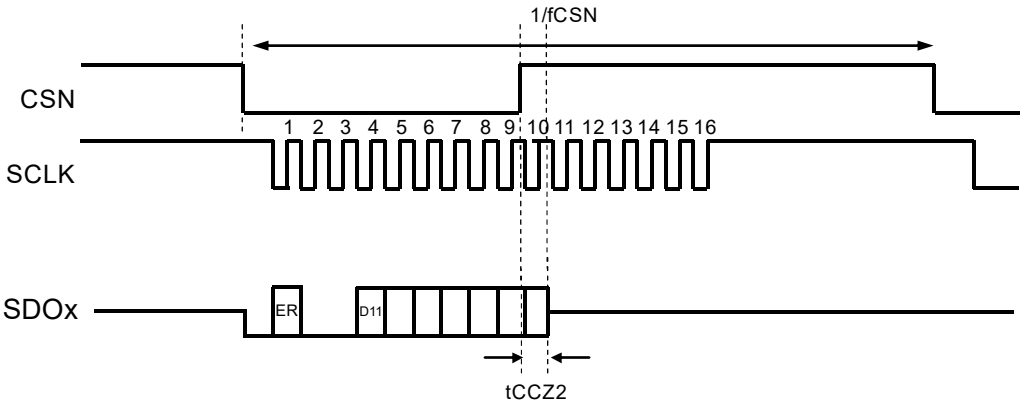


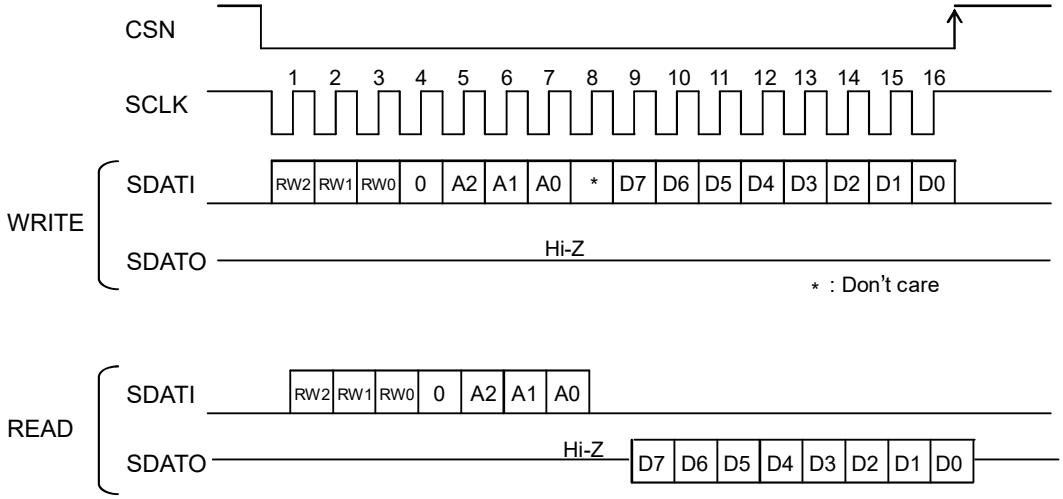
Figure 11. When CSN Pin Is Put to “H” During Conversion

■ Serial Control Interface2 (Register Write/Read)

Internal registers may be written by using 4-wire serial interface pins (CSN, SCLK, SDATI and SDATO). The data on this interface consists of Op code (3bits), Read/Write, Register address (MSB first, 3bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of SCLK and data is clocked out on the falling edge. Data writings become available on the 16th rising edge of SCLK. When reading the data, the SDATO pin changes to output mode at the falling edge of 8th SCLK and outputs data in D7-D0. The data output finishes on the rising edge of CSN. The SDATA is placed in a Hi-Z state except when outputting the data at read operation mode. Clock speed of SCLK is 20MHz (max).

When the clock speed of SCLK is over 12MHz, it is recommended to read register data on a falling edge of SCLK. In the case of reading data by a falling edge of SCLK, D0 bit must be read on the 17th falling edge of SCLK or a rising edge of CSN after the 16th rising edge of SCLK.

Register read must be executed after writing to registers to confirm if the register write is executed correctly since an AD conversion will not processed properly if the register setting above does not set correctly.

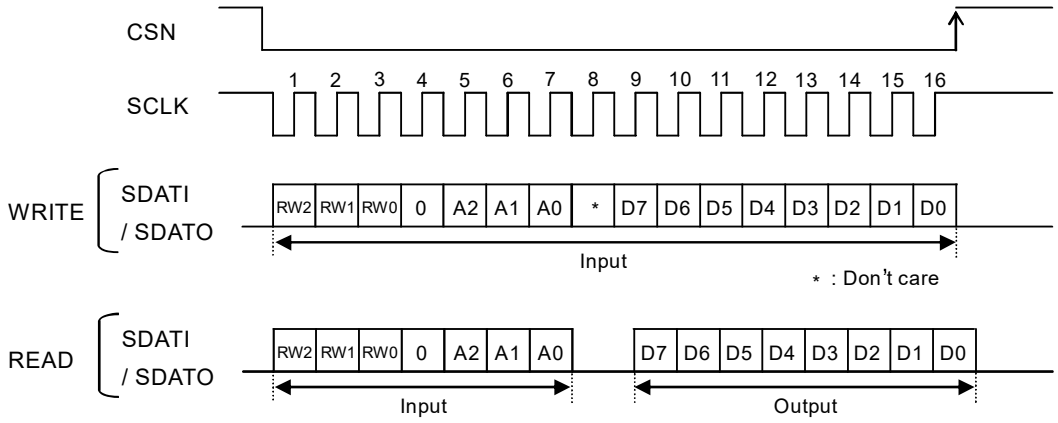


RW2-RW0: Op code
"110" = WRITE
"101" = READ
A2-A0: Register Address
D7-D0: Control data

Figure 12. Digital I/F2

■ Serial Control Interface3 (Register Write/Read)

A register read and write can be executed via 3-wire serial I/F pins (CSN, SCLK, SDATI/SDATO) if the SDATI and the SDATO pins are short-circuited.



RW2-RW0: Op code
"110" = WRITE
"101" = READ
A2-A0: Register Address
D7-D0: Control data

Figure 13. Digital I/F3

■ Register Self-Diagnosis Function

(1) Self-Diagnosis Function

The AK9240 has self-diagnosis function for unexpected data change of registers. When the AK9240 detects a data change of registers comparing to the written setting, ER bit value that is output from the SDOx pin is changed to “1”. When this alarm is output, execute all register writings again to return to normal operation.

(2) Detail

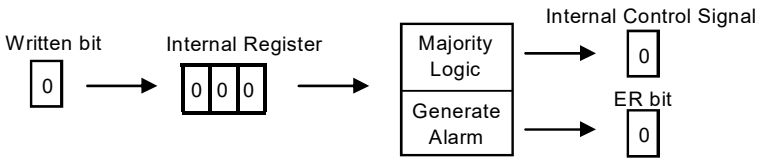


Figure 14. Register Self-Diagnosis Function

The AK9240 stores write data in three multiple internal registers.

Table 10. Register Data three multiplex Storage

Written bit	Internal Register
0	000
1	111

ER bit of the AK9240 works as alarm signal. ER bit is set to “0” when all internal three multiplex registers have the same values. When all internal three multiplex registers do not have the same values, ER bit is set to “1”. ER bit keeps this “1” value until the mismatched address is written again and all three internal registers have the same value.
The AK9240 uses majority logic for three multiplex registers to determine the internal control signal. Therefore, the internal operation of the AK9240 will not be changed when only 1 bit data is changed unexpectedly.

Table 11. Majority Logic / Alarm Output

Internal Register	ER bit	Internal Control Signal
000	0	0
001	1	0
010	1	0
100	1	0
111	0	1
110	1	1
101	1	1
011	1	1

Note:
* 38. It is recommended that all register writings should be executed again when the alarm (ER bit= “1”) is detected.

■ LED Driver Normal Operation Mode

The AK9240 has a LED driver that has following five operation modes.

Table 12. LED Driver Normal Mode

Mode		Block			Addr: 0H		Addr: 1H	
		APC	LED	LED Backup	PMAPC	PMLED	LEDST	LEDBU
1	APC	ON	ON	OFF	1	1	0	0
2	LED	OFF	ON	OFF	0	1	0	0
3	LED ST	OFF	Standby	OFF	0	1	1	0
4	LED BU	OFF	OFF	ON	0	0	0	1
5	LED PD	OFF	OFF	OFF	0	0	0	0

(1) APC : Auto Power Control mode
The AK9240 has an Auto Power Control (APC) circuit. The APC circuit adjusts the LED driver current according to an increase or decrease of the LEDREF pin voltage and analog input average voltage.

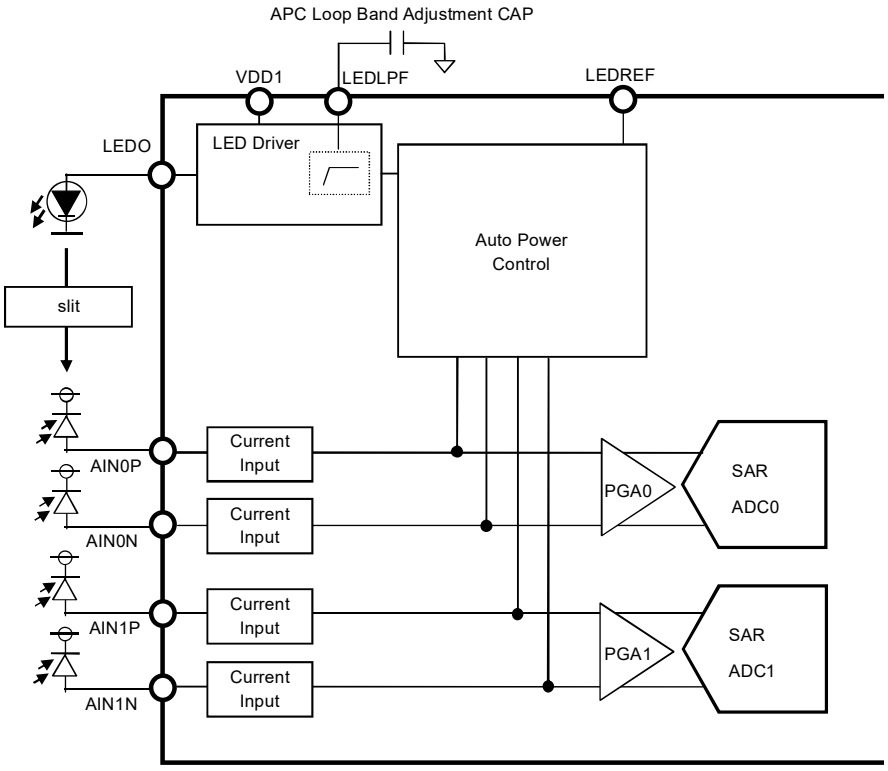


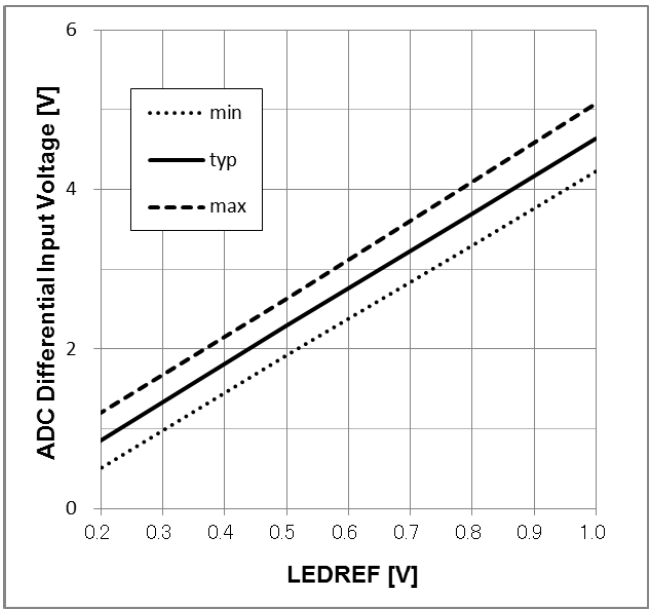
Figure 15. APC Circuit Diagram

Caution : APC mode can be used only in current input mode.
(Can not be used in voltage input mode.)
Caution : APC mode is available only when 2 channels are input.
(Can not be used when 1 channel is input.)
Caution : Do not use with optical gain higher than specification value.

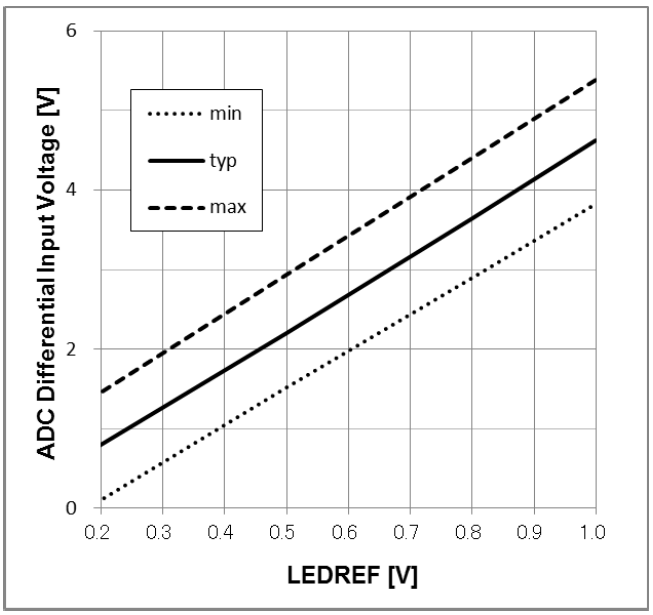
<Example>
In the case of 20mA LED Driver Current, (AINxP – AINxN) = 10μAdiffpp, Offset Current =0μA

Table 13. APC Example

Parameter			Min.	Typ.	Max.	Unit
Differential Input Voltage to ADC	Gain bit =”X00”	LEDREF=0.8V	3.3	3.7	4.1	Vdiffpp
		LEDREF=0.5V	1.92	2.3	2.63	Vdiffpp
		LEDREF=0.2V	0.5	0.85	1.2	Vdiffpp
	Gain bit =”X01”	LEDREF=0.8V	3.2	3.7	4.2	Vdiffpp
		LEDREF=0.5V	1.82	2.3	2.73	Vdiffpp
		LEDREF=0.2V	0.4	0.85	1.3	Vdiffpp
	Gain bit =”X10”	LEDREF=0.8V	3.1	3.7	4.25	Vdiffpp
		LEDREF=0.5V	1.67	2.25	2.83	Vdiffpp
		LEDREF=0.2V	0.3	0.8	1.35	Vdiffpp
	Gain bit =”X11”	LEDREF=0.8V	2.9	3.65	4.4	Vdiffpp
		LEDREF=0.5V	1.52	2.2	2.93	Vdiffpp
		LEDREF=0.2V	0.1	0.8	1.45	Vdiffpp



(a) Gain bit =”X00”



(b) Gain bit =”X11”

Figure 16. APC Example

APC loop band can be adjusted by the external capacitance of the LEDLPF pin.

<Example> 20mA LED driver current, (AINxP – AINxN) = 10μAdiffpp

Table 14. APC Loop Band Adjusting Example1

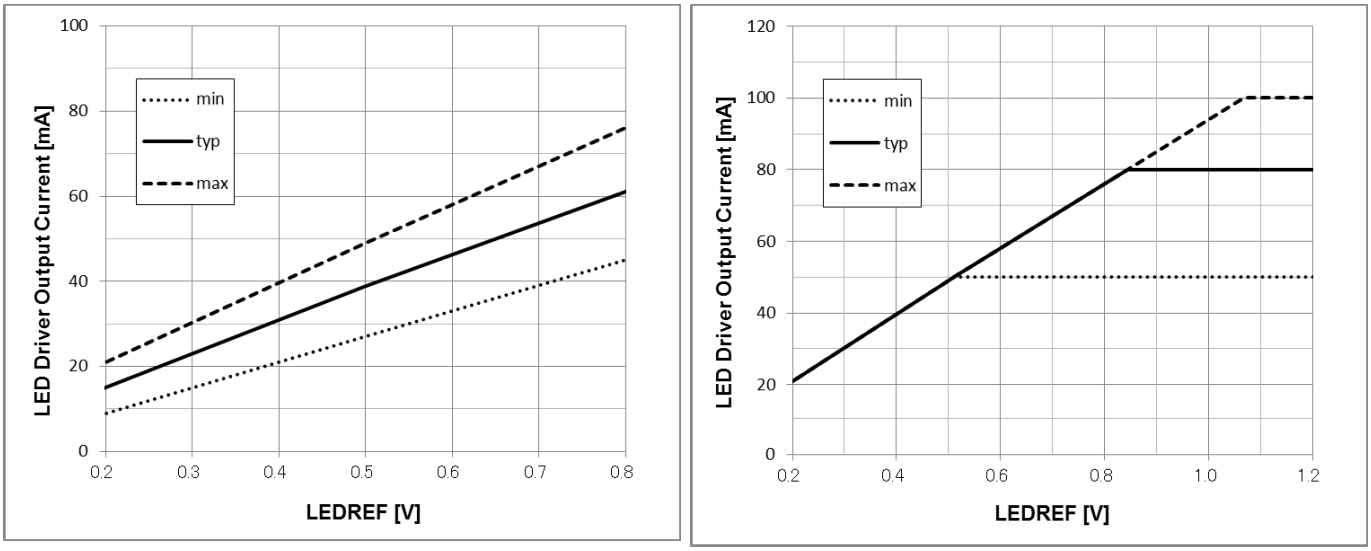
LEDLPF External Capacitance	APC Loop Band
0.1μF	400Hz
1μF	40Hz

<Example> 40mA LED driver current, (AINxP – AINxN) = 10μAdiffpp

Table 15. APC Loop Band Adjusting Example2

LEDLPF External Capacitance	APC Loop Band
0.1μF	200Hz
1μF	20Hz

(2) LED : LED mode
The LED driver current (ILED) is determined by the voltage input to the LEDREF pin.



(a) LED Driver Output Current Slope (b) LED Driver Maximum Output Current (Slope: max)

Figure 17. LED Driver Example (LED Mode: VDD0= 5.0V, VDD1= 5.0V)

(3) LED ST : LED Standby mode
The AK9240 has LED standby mode. LEDST bit switches LED mode and LED standby mode, realizing intermittent operation of the LED driver. The average current can be controlled by this intermittent operation cycle.

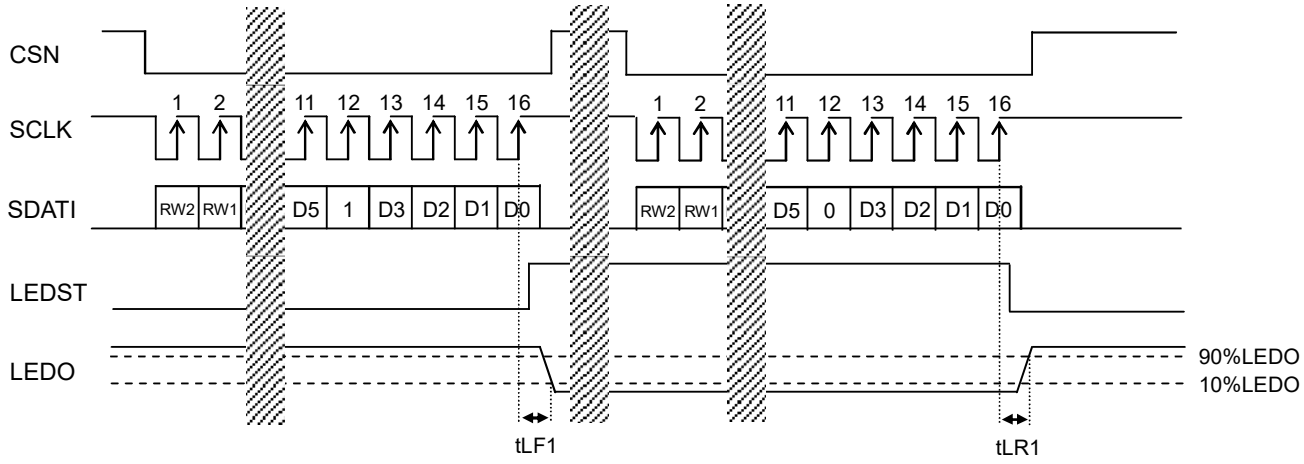


Figure 18. LED Driver Intermittent Operation

<Example> 20msec average drive current is targeted.

Table 16. Intermittent Operation Cycle Setting Example (LED Mode)

ILED	LEDST Low Period	Intermittent Operation Cycle	Average Drive Current
40mA	25µsec	20kHz	20mA
80mA		10kHz	

Note:
* 39. It does not include drive currents at power-up and power-down periods.

(4) LED BU : LED Backup mode
The AK9240 has LED backup mode.

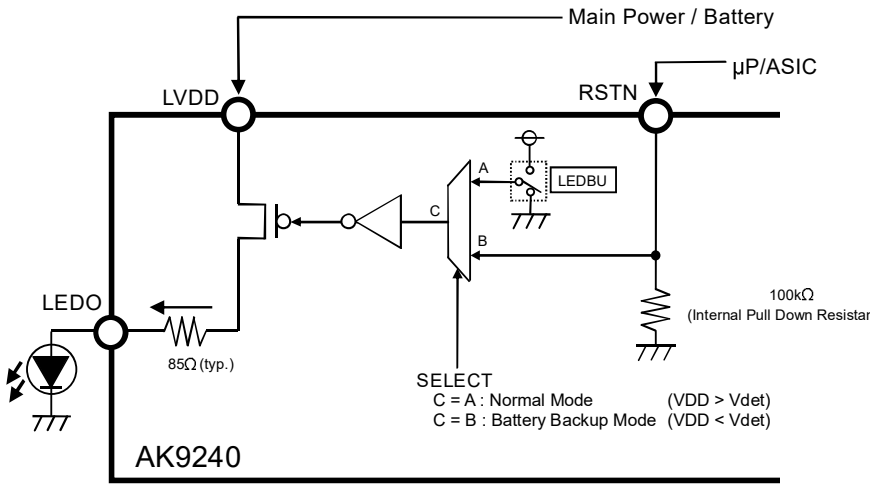


Figure 19. LED Driver Composition (Backup Mode)

In LED backup mode, the LED driver output current (ILED) is detemined by input voltage of VDD1 and LEDO voltage. The LED driver can be operated intermittently by controlling with LEDBU bit in LED backup mnode. In battery backup modde, it can be operated intermittently by controlling the RSTN pin.

<Example> LEDO Voltage 1.3V

Table 17. LED Driver Current (Backup Mode)

VDD1	ILED (Typ.)
3.0V	20mA
5.0V	44mA

(5) LED PD : LED Power Down mode
AK9240 has an LED driver / APC circuit . By powering down these blocks at this mode setting,
It is possible to use only PGA and ADC with current input and voltage input.

■ Battery Backup Mode

The AK9240 has Battery Backup Mode that is able to drive LEDs even if the VDD0 is in open state. The AK9240 enters battery backup mode when VDD0 voltage drops under Vdet (Typ. 0.5 x VDD1).

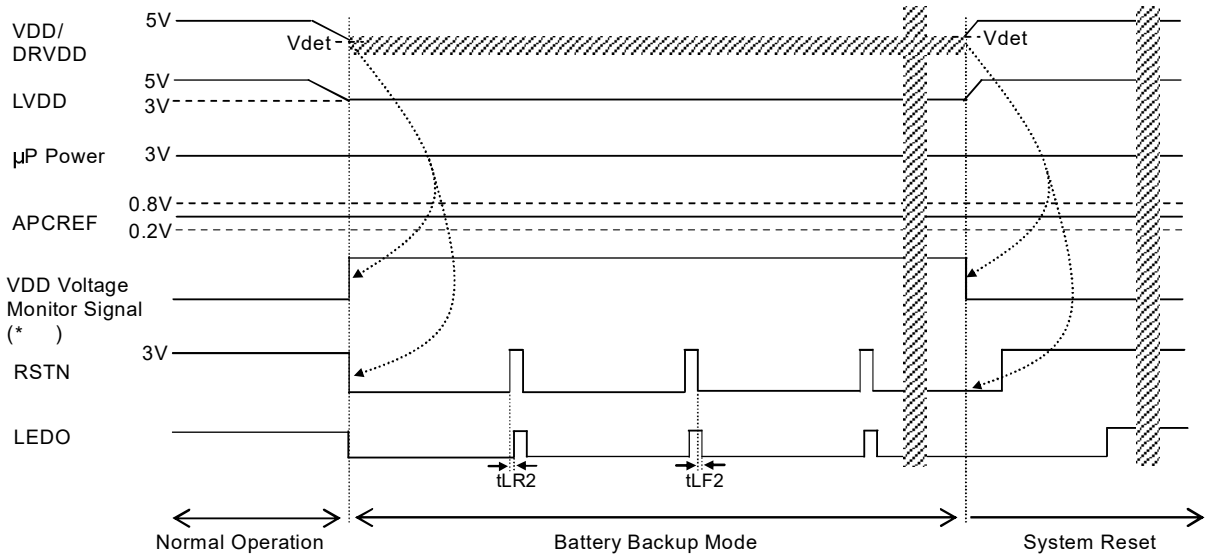


Figure 20. Battery Backup Mode Example1

Note:
* 40. VDD0 Voltage Monitor Signal: Signal that is generated by the system.

The LED driver can be operated in intermittent operation by controlling the RSTN pin in backup mode.

Table 18.RSTN pin Function (Battery Backup Mode)

RSTN pin	Battery Backup Mode Operation Status
L	Power Down
H	Power Up

<Example> 1µsec or less Average Consumption Current is Target (LED Driver Current Including ILED)

Table 19. Intermittent Operation Cycle Setting Example (Battery Backup Mode)

ILED	AK9240 Consumption Current	RSTN High Period	Intermittent Cycle	Average Consumption Current
20mA	< 1µA	200nsec	< 250Hz	< 1µA

Notes:
* 41. It does not include consumption currents at power-up and power-down periods.
* 42. It does not include the current that flows to pull-down resistor of the RSTN pin.

<Normal Operation → Battery Backup Mode>
ILED flows when the RSTN pin= “H”.

<Battery Backup Mode → Normal Operation>
There is a possibility that ILED flows when the RSTN pin= “H”.

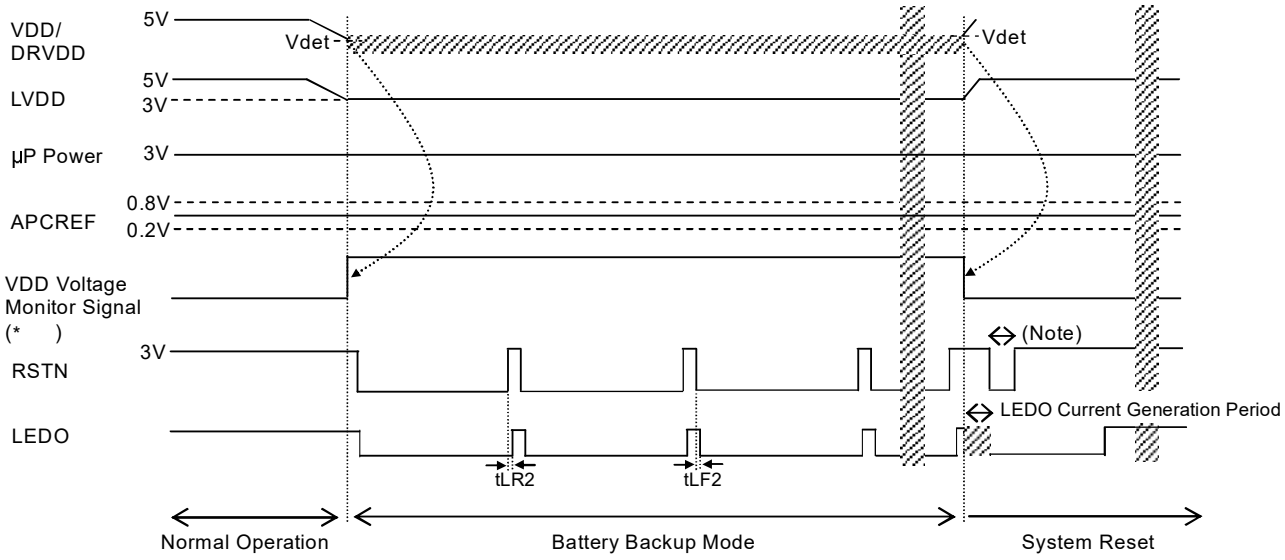


Figure 21. Battery Backup Mode Example 2

Notes:

* 43. If the power is switched while the RSTN pin= “H”, the RSTN pin must be set to “L” after power-up the AK9240.
* 44. **There is a possibility that a current flows to the LEDO pin while the RESTN pin = “H” when power up the AK9240.**

■ System Reset

The RSTN pin should be set to "L" upon power up the AK9240.
Set the RSTN pin to "H" after power supply is risen up and write register settings.
Power-up timing of the AK9240 is shown below.

(1) APC Mode
* LED Driver Current 20mA, (AINxP – AINxN) = 10μAdiffpp, LEDLPF pin= 0.1μF

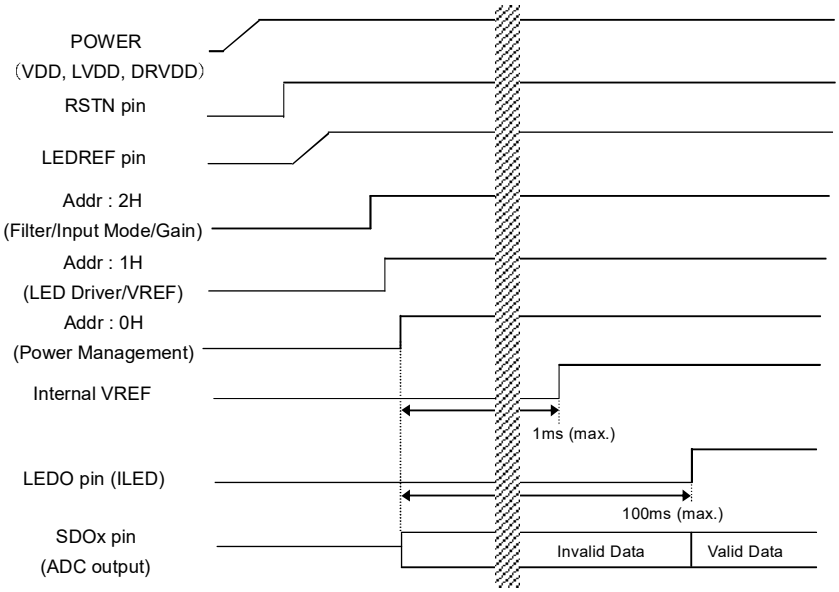


Figure 22. Power-Up Timing1

(2) LED Mode
* LEDLPF pin= 0.1μF

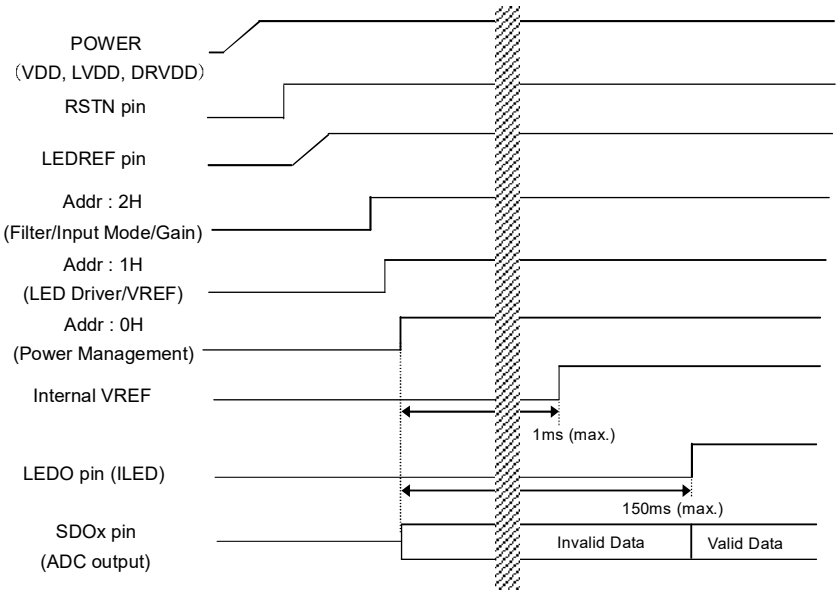


Figure 23. Power-Up Timing2

Notes:
* 45. The RSTN pin must be set to "L" after power is supplied if power up the AK9240 while the RSTN pin= "H".
* 46. **There is a possibility that a current flows to the LEDO pin while the RESTN pin = "H" when power up the AK9240.**
* 47. Resister read should be executed after writing resister settings to confirm the data.

(4) LED Power Down Mode
※VREFP pin =1μF

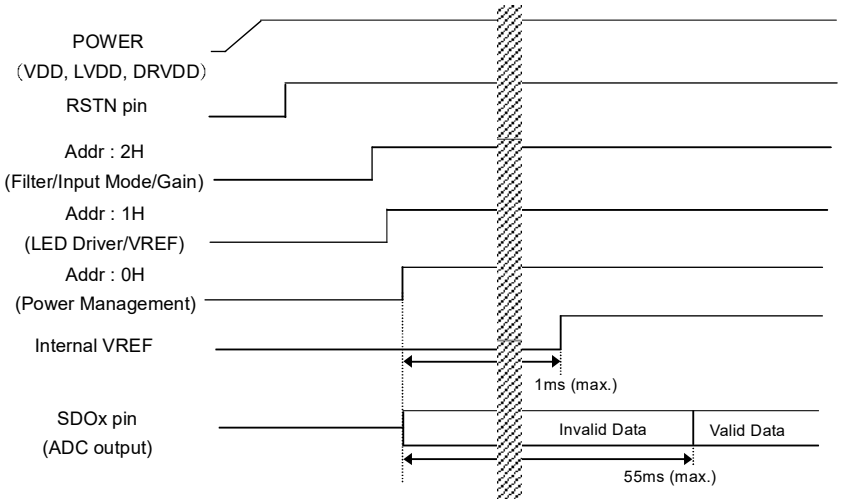


Figure 10. Power-Up Timing3

Notes:
* 48. Resister read should be executed after writing resister settings to confirm the data.

(4) LED Backup Mode Example

The AK9240 can shorten the time that LED is not emitting by being power up in LED backup mode.

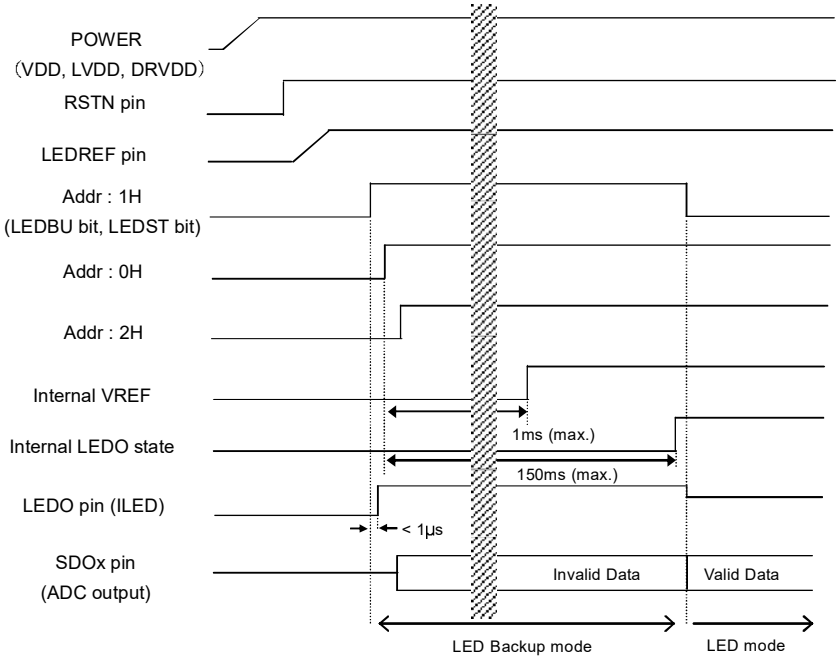


Figure 25. Power-Up Timing Example4 (LED Backup Mode)

By the register Write/Read sequence example shown below, LEDs will emit continuously during the power-up in LED backup mode.

<Example> Register Write/Read Sequence (Power Up in LED Backup Mode)

1. Register Write1	Addr= 1H: LEDBU bit= “1”, LEDST bit= “1”
	* LED Back Up Mode (* 49)
2. Register Read1	Addr = 1H
3. Register Write2	Addr = 0H
4. Register Read2	Addr = 0H
5. Register Write3	Addr = 2H
6. Register Read3	Addr = 2H
7. 50msec (Typ.)	Wait
8. Register Write4	Addr = 1H: LEDBU bit = “0”, LEDST bit = “0” *LED Mode (* 50)
9. Register Read4	Addr = 1H

Notes:

* 49. ILED current corresponding to VDD1 input voltage flows. (Table 17)

* 50. ILED current corresponding to the input voltage to the LEDREF pin flows. (Figure 17)

14. Register Setting

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0H	Power Management	0	0	0	PMREF	PMLED	PMAPC	PMAD1	PMAD0
1H	LED Driver / VREF	SDOT	0	LEDBU	LEDST	0	0	VREFV	VRMOD
2H	Filter/ Input Mode/ Gain	0	0	0	FIL	MOD	GAIN [2:0]		

Note:
* 51. Write “0” data to the bits specified as 0.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0H	Power Management	0	0	0	PMREF	PMLED	PMAPC	PMAD1	PMAD0
Default		0	0	0	0	0	0	0	0

PMREF: VREF Block Power Management
0: REF Power Down
1: REF Power Up

PMLED: LED Block Power Management
0: LED Power Down
1: LED Power Up

PMAPC: APC Block Power Management
0: APC Power Down
1: APC Power Up

PMAD1: PGA/ADC Block Power Management
0: PGA1/ADC1 Power Down
1: PGA1/ADC1 Power Up

PMAD0: PGA/ADC Block Power Management
0: PGA0/ADC0 Power Down
1: PGA0/ADC0 Power Up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1H	LED Driver / VREF	SDOT	0	LEDBU	LEDST	0	0	VREFV	VRMOD
Default		0	0	0	0	0	0	0	0

SDOT: ADC output timing Switch on SDOx
0: ADC output timing by 4th SCLK↓
1: ADC output timing by 3rd SCLK↓

LEDBU: LED Backup Mode ON/OFF
0: LED Backup Mode OFF
1: LED Backup Mode ON

LEDST: LED Mode ILED ON/OFF
0: LED Mode ILED ON
1: LED Mode LED STANDBY

VREFV: Internal Reference Voltage Switching
0: Internal VREF = “2.5V (typ.)”
1: Internal VREF = “1.5V (typ.)”

VRMOD: Reference Voltage Signal Switch
0: Internal VREF
1: External VREF

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2H	Filter/ Input Mode/ Gain	0	0	0	FIL	MOD	GAIN [2:0]		
Default		0	0	0	0	0	0	0	0

FIL: Low Pass Filter Cut-off Frequency Switch
0: 250 kHz (typ.)
1: 100 kHz (typ.)

MOD: Input Mode Switch
0: Voltage mode
1: Current mode

GAIN [2:0]: PGA0/1 Gain Switch
(1) Voltage Input mode (MOD bit= “0”)
000: PGA0/1 Gain = “14dB (typ.)”
001: PGA0/1 Gain = “17dB (typ.)”
010: PGA0/1 Gain = “20dB (typ.)”
011: PGA0/1 Gain = “23dB (typ.)”
100: PGA0/1 Gain = “26dB (typ.)”
101: PGA0/1 Gain = “29dB (typ.)”
110: PGA0/1 Gain = “32dB (typ.)”
111: PGA0/1 Gain = “35dB (typ.)”
(2) Current Input mode (MOD bit= “1”)
000: PGA0/1 Gain = “65kΩ (typ.)”
001: PGA0/1 Gain = “91kΩ (typ.)”
010: PGA0/1 Gain = “130kΩ (typ.)”
011: PGA0/1 Gain = “183kΩ (typ.)”
100: PGA0/1 Gain = “130kΩ (typ.)”
101: PGA0/1 Gain = “183kΩ (typ.)”
110: PGA0/1 Gain = “260kΩ (typ.)”
111: PGA0/1 Gain = “365kΩ (typ.)”

15. Recommended External Circuits

■ LED Backup mode

Figure 26 shows an example of external connection circuit in LED power down mode (voltage input).
Please refer to the evaluation board (AKD9240ENC) for specific circuits and measurement examples.

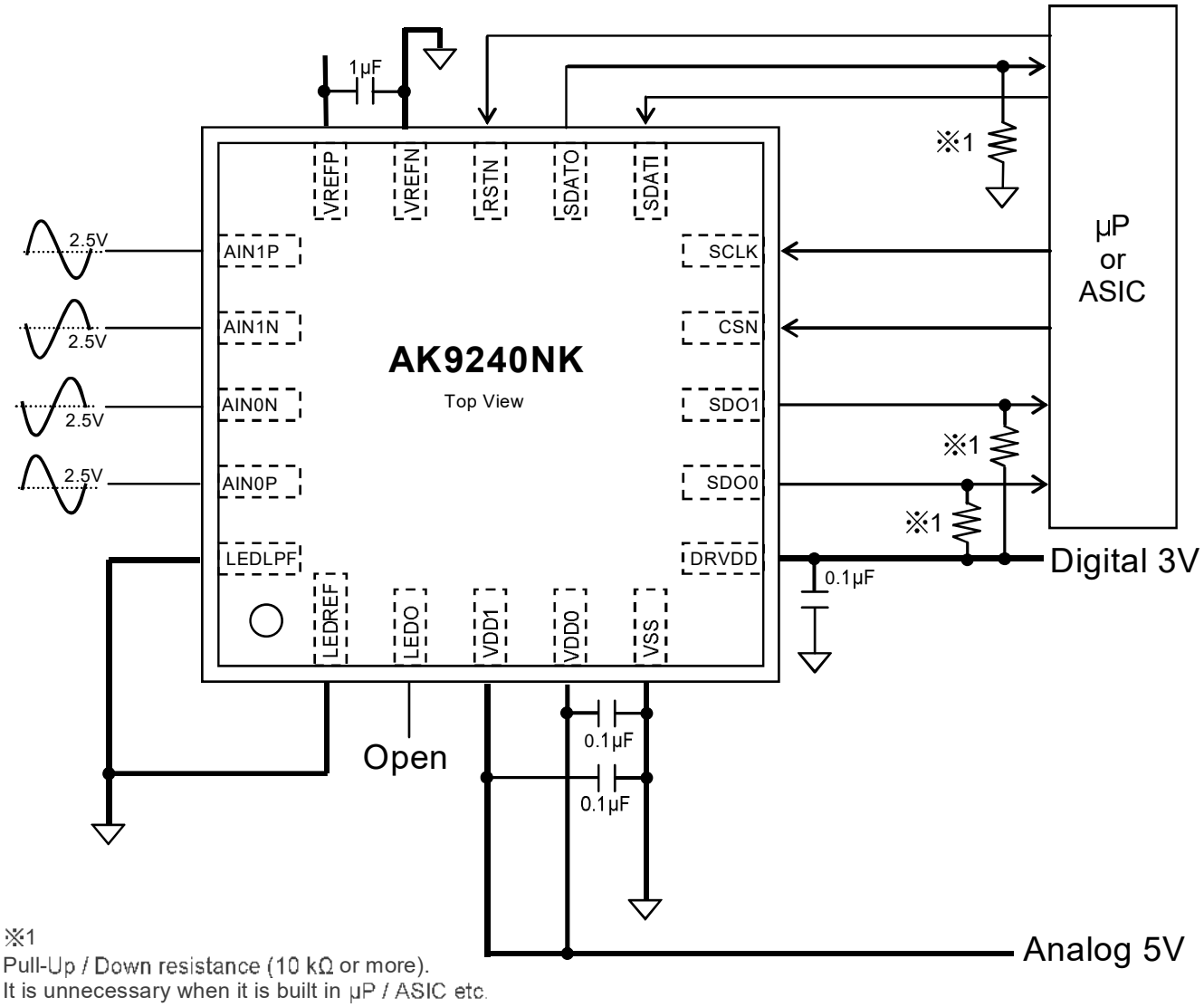


Figure 26. Typical Connection Diagram1

■ APC mode / LED mode

Figure 27 shows an external connection circuit example in APC / LED mode (current input).
Refer to the evaluation board (AKD9240) for specific circuits and measurement examples.

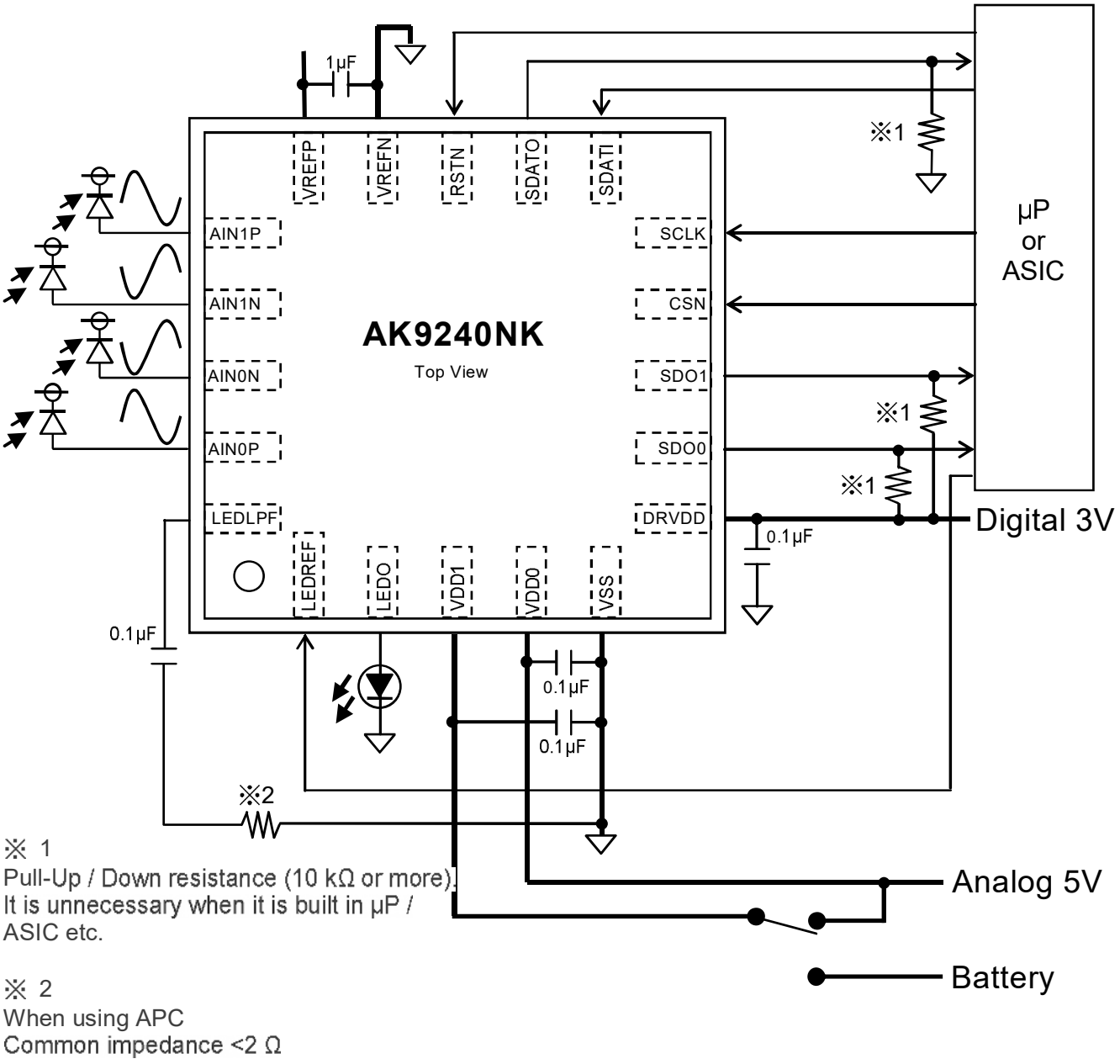


Figure 27. Typical Connection Diagram2

■ Battery backup mode

Figure 28 shows an external connection circuit example in battery backup mode (current input).

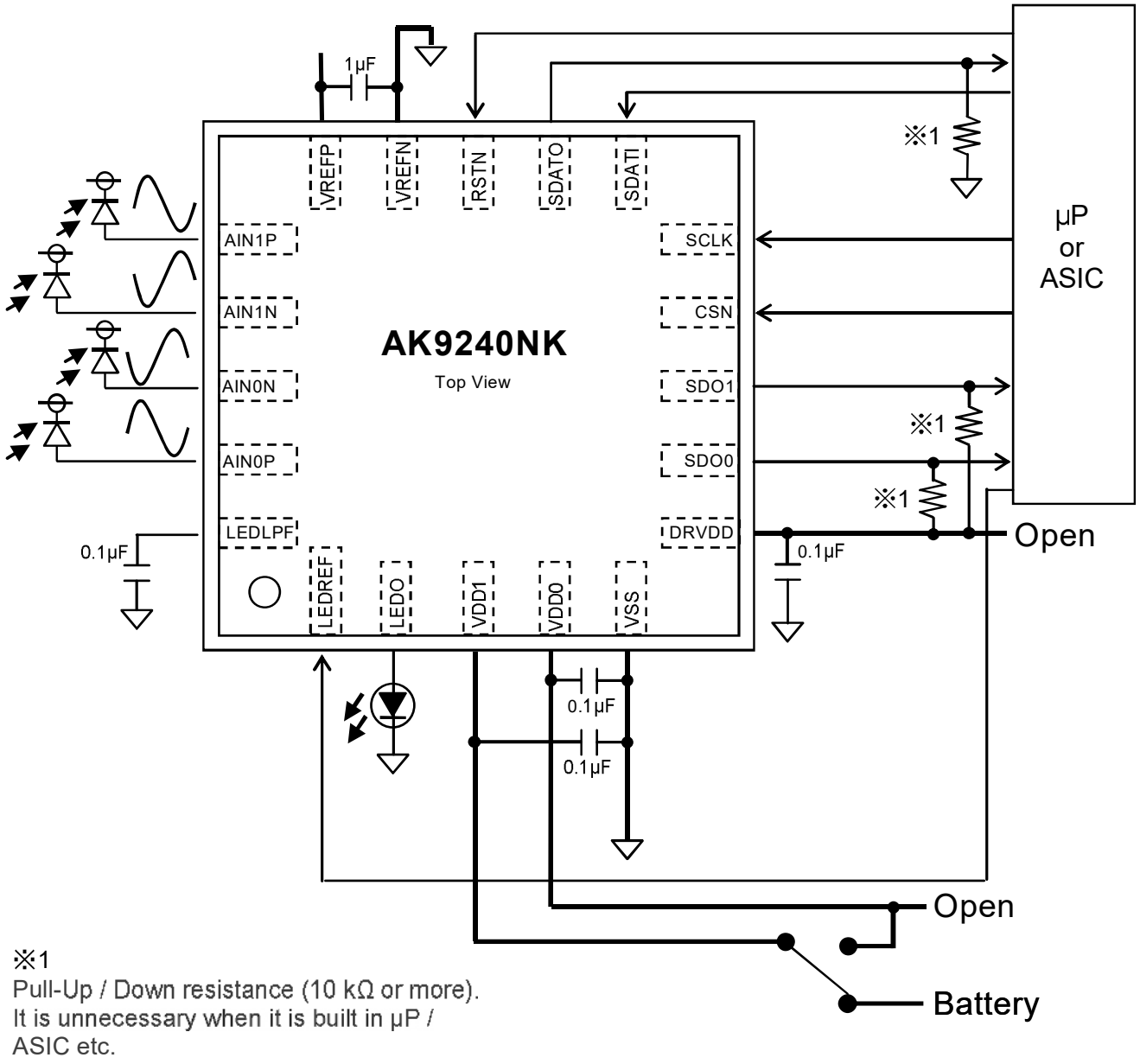
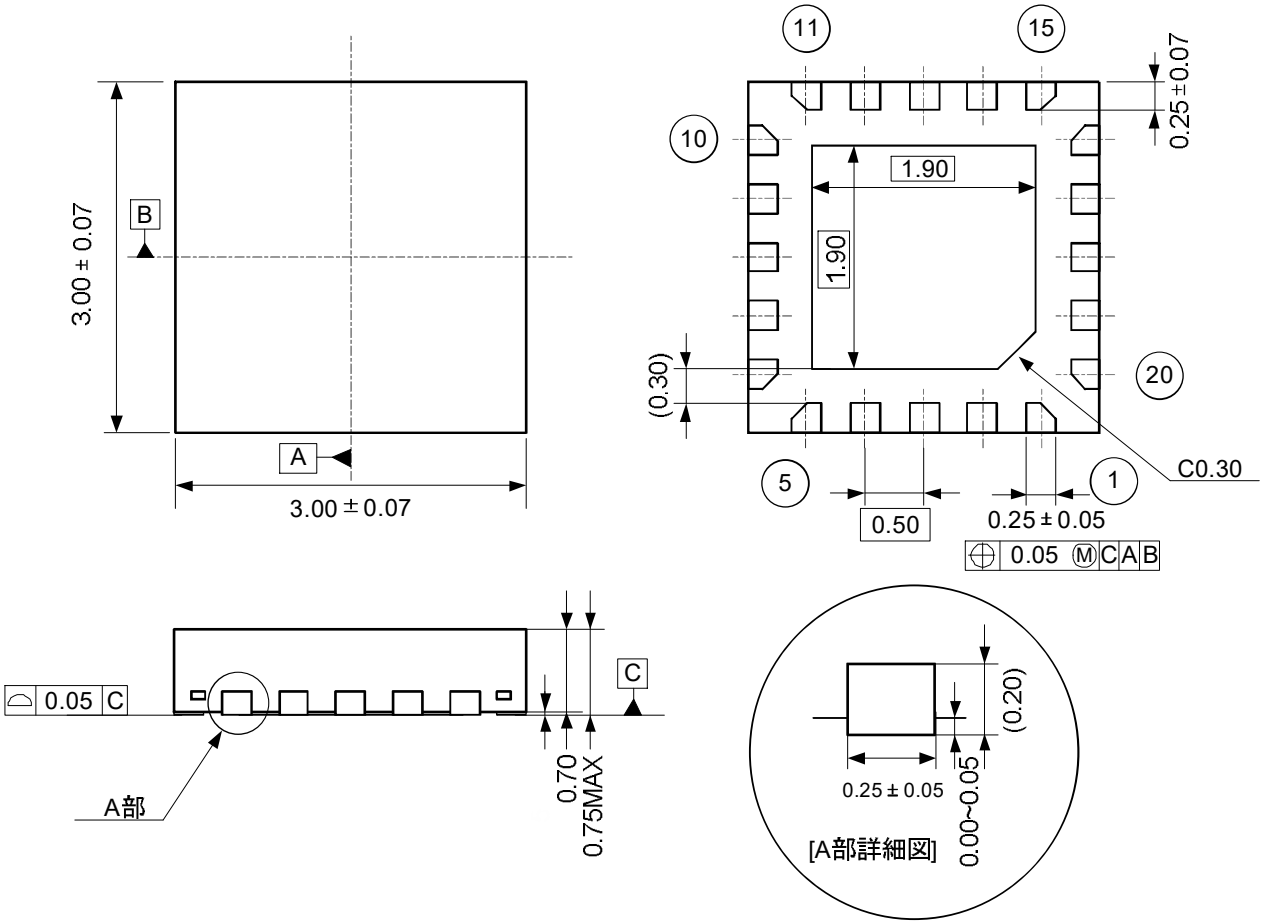


Figure 28. Typical Connection Diagram3

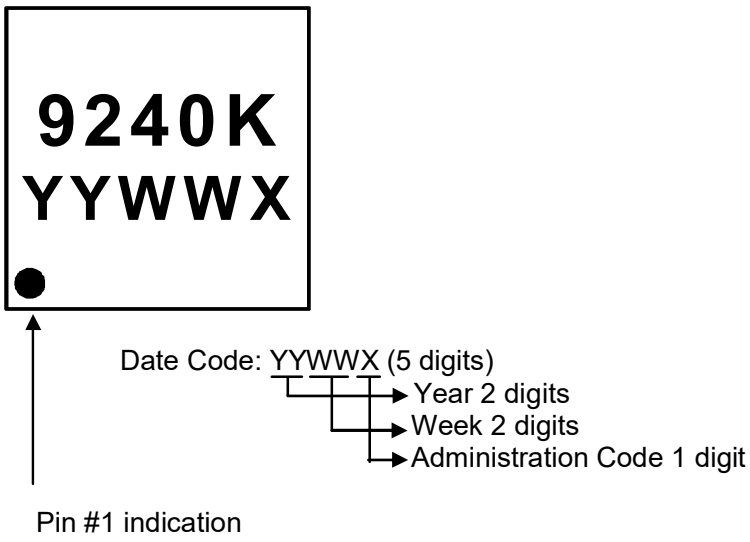
16. Package

■ **Outline Dimensions**



Note:
*52. The exposed pad on the bottom surface of the package must be open or connected to the ground.

■ **Marking**


9240K
YYWWX
Date Code: YYWWX (5 digits)
Year 2 digits
Week 2 digits
Administration Code 1 digit
Pin #1 indication

17. Ordering Guide

AK9240NK	-40 ~ 105ºC	20-pin QFN(3.0mm x 3.0mm, 0.5mm pitch)
AKD9240	Evaluation Board for the AK9240	

18. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
17/12/7	01	First Edition		

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