2.4MHz, 3A x 2ch Synchronous Buck Converter for POL

■FEATURES

- ●2ch Synchronous Rectification
- ●Current Mode Control
- ●Operating Voltage Range 2.7V to 5.5V
- ●Switching Current 3.3A min.
- ●Adjustable Oscillating Frequency 100kHz to 2.4MHz
- ●External Clock Synchronization
- ●PWM Control
- ●Maximum Duty Cycle 100%
- ●High Efficiency at Light Loads (Selectable)
- ●Low Iq at Sleep Mode 500μA typ.
- ●Anti-Phase switching
- ●External Compensation Circuit
- ●Correspond to Ceramic Capacitor (MLCC)
- ●Adjustable Soft Start Function
- ●UVLO (Under Voltage Lockout)
- ●Over Current Protection (Hiccup type)
- ●Thermal Shutdown Protection
- ●Power Good Function
- ●Standby Function
- ●Package Outline EQFN24-LE

■GENERAL DESCRIPTION

The NJW4110 is a synchronous 2ch buck converter with 3A MOSFET. The switching oscillating frequency is adjustable from 100kHz to 2,4MHz. Also, it can be synchronized with external clock. The NJW4110 can be selected PFM to ensure high efficiency at light load.

The NJW4110 has a single oscillator and operates an Ant-Phase switching to reduce input ripple current

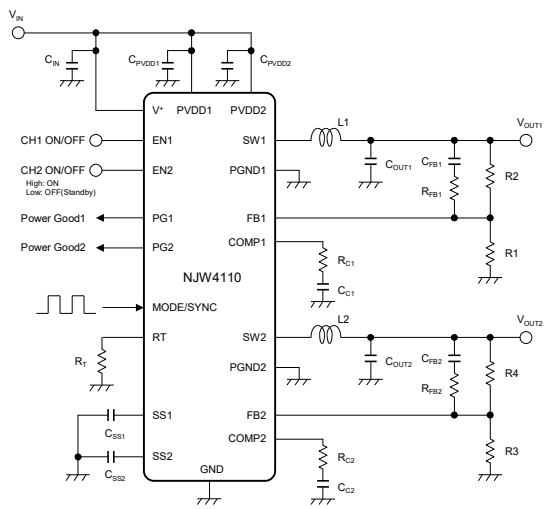
Each buck converters have independent enable functions, soft start functions, over current protection and power good functions. The protection functions are UVLO and thermal shutdown circuit.

It is suitable for power supply circuit of SoC, DSP, DDR memory and so on that need fast transient response.

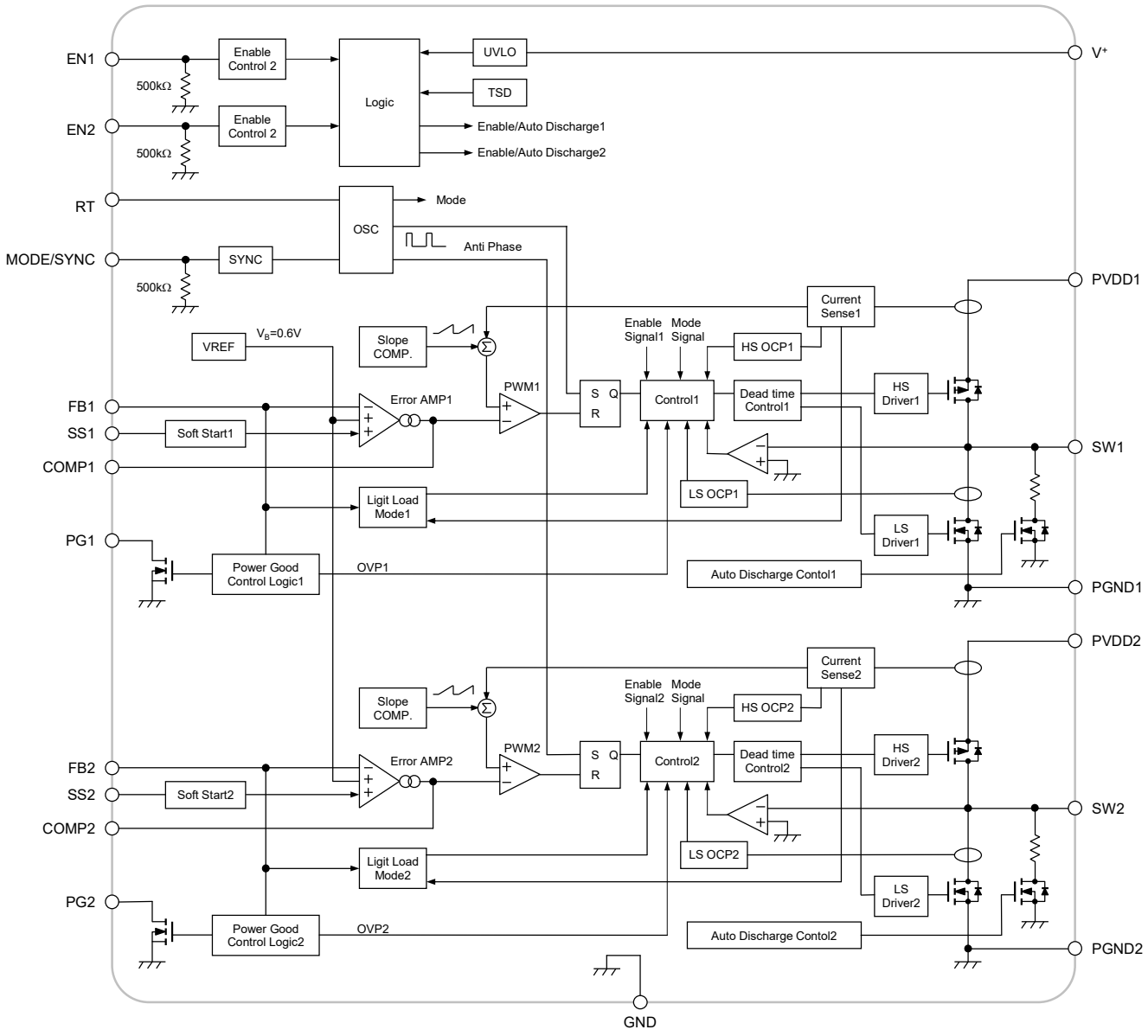
■APPLICATION

- ●Power supply for SoC, ASIC, DDR and the others

■TYPICAL APPLICATION

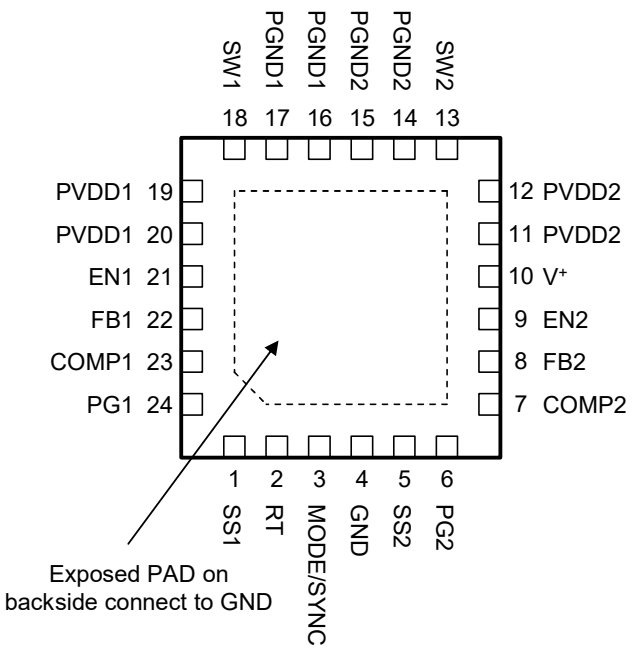


■BLOCK DIAGRAM



■PIN CONFIGURATION

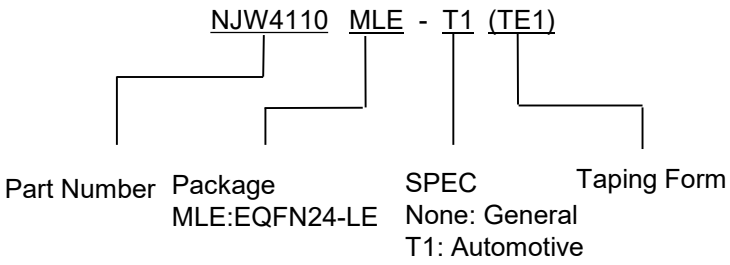
EQFN24-LE



Note) Exposed Pad on backside should be connected to ground and soldered to PCB.

PIN NO.	SYMBOL	DESCRIPTION
1	SS1	Soft start setting of Ch.1
2	RT	Oscillating frequency setting
3	MODE/SYNC	Light Load mode select and external clock synchronization
4	GND	Signal ground
5	SS2	Soft Start setting of Ch.2
6	PG2	Power Good output of Ch.2
7	COMP2	Error Amplifier output of Ch.2
8	FB2	Feedback input of Ch.2
9	EN2	Enable control of Ch.2
10	V^+	Power supply for IC Control
11	PVDD2	Power supply of Ch.2
12	PVDD2	
13	SW2	Switch output of Ch.2
14	PGND2	Power ground of Ch.2
15	PGND2	
16	PGND1	Power ground of Ch.1
17	PGND1	
18	SW1	Switch output of Ch.1
19	PVDD1	Power supply of Ch.1
20	PVDD1	
21	EN1	Enable control of Ch.1
22	FB1	Feedback input of Ch.1
23	COMP1	Error Amplifier output of Ch.1
24	PG1	Power Good output of Ch.1

■PRODUCT NAME INFORMATION



■ORDERING INFORMATION

PRODUCT NAME	PACKAGE OUTLINE	AUTO MOTIVE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ(pcs)
NJW4110MLE (TE1)	EQFN24-LE		yes	yes	Sn2Bi	4110	31	1,000
NJW4110MLE-T1 (TE1)	EQFN24-LE	yes	yes	yes	Sn2Bi	4110T1	31	1,000

This data sheet is applied to "NJW4110MLE".
Please refer to each data sheet for other versions.

■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	-0.3 to +7	V
PVDD1,2 pin Voltage	$PV_{DD1,2}$	-0.3 to +7	V
SW1,2 pin Voltage	$V_{SW1,2}$	-0.3 to +7	V
EN1,2 pin Voltage	$V_{EN1,2}$	-0.3 to +7	V
FB1,2 pin Voltage	$V_{FB1,2}$	-0.3 to +7	V
PG1,2 pin Voltage	$V_{PG1,2}$	-0.3 to +7	V
MODE/SYNC pin Voltage	$V_{MODE/SYNC}$	-0.3 to +7	V
Power Dissipation(Ta=25°C) EQFN24-LE	P_D	(2-layer / 4-layer) 1,000[1]/ 2,800[2]	mW
Junction Temperature	T_j	-40 to +150	°C
Operating Temperature	T_{opr}	-40 to +125	°C
Storage Temperature	T_{stg}	-50 to +150	°C

(1): Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

(2): Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)
(For 4Layers: Applying 99.5×99.5mm inner Cu area and thermal via holes to a board based on JEDEC standard JESD51-5)

■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	2.7 to 5.5	V
PVDD1,2 pin Voltage	$PV_{DD1,2}$	Up to 5.5	V
PG1,2 pin Voltage	$V_{PG1,2}$	0 to 5.5	V
Timing Resistor	R_T	2.26 to 84.5	kΩ
Oscillating Frequency	f_{OSC}	100 to 2,400	kHz
External Clock Input	f_{SYNC}	f_{OSC}×0.9 to f_{OSC}×1.9 (Minimum 200kHz, Maximum 2,800kHz)	kHz

■ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $PV_{DD}=V^{+}=V_{EN}=3.3V$, PGND=GND, $R_T=6.8k\Omega$, Common to CH1 and CH2, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Under Voltage Lockout Block						
ON Threshold Voltage	V_{T_ON}	V^{+}= L → H	2.5	2.6	2.7	V
OFF Threshold Voltage	V_{T_OFF}	V^{+}= H → L	2.4	2.5	2.6	V
Hysteresis Voltage	V_{HYS}		80	100	–	mV
Soft Start Block						
Charge Current	I_{CHG}		6	8	10	μA
Oscillator Block						
Oscillating Frequency 1	f_{OSC1}	R_T=26.1 kΩ	255	300	345	kHz
Oscillating Frequency 2	f_{OSC2}	R_T=6.8 kΩ	850	1,000	1,150	kHz
Oscillating Frequency 3	f_{OSC3}	R_T=2.26kΩ	2,160	2,400	2,640	kHz
Error Amplifier Block						
Reference Voltage	V_B		-1.0%	0.6	+1.0%	V
Input Bias Current	I_B		-0.1	–	0.1	μA
Error Amplifire Transconductance	gm		–	450	–	μA/V
Error Amplifire Gain	Av		–	1,400	–	–
Output Source Current	I_{OM+}		33	45	60	μA
Output Sink Current	I_{OM-}		33	45	60	μA
PWM Comparate Block						
Maximum Duty Cycle	$M_{AX}D_{UTY}$	V_{FB}=0.5V	100	–	–	%
Minimum OFF Time	$t_{OFF-min}$		–	80	–	ns
Minimum ON Time	t_{ON-min}		–	80	–	ns

■ELECTRICAL CHARACTERISTICS (CONTINUED)

(Unless otherwise noted, $PV_{DD}=V^{+}=V_{EN}=3.3V$, PGND=GND, $R_T=6.8k\Omega$, Common to CH1 and CH2, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
OCP Block						
COOL DOWN Time	t_{COOL}		–	120	–	ms
Output Block						
High-side SW ON Resistance	R_{ONH}	I_{SW}=-3A	–	80	120	mΩ
Low-side SW ON Resistance	R_{ONL}	I_{SW}=3A	–	60	100	mΩ
High-side Switching Current Limit	I_{LIMH}		3.3	4.5	6	A
Low-side Switching Current Limit	I_{LIML}	SW to PGND	2.3	3.5	5.5	A
Auto Discharge Resistance	$R_{AUTODIS}$	I_{SW}=10mA	–	60	100	Ω
High-side SW Leak Current	I_{LEAKH}	PV_{DD} - V_{SW}=5.5V	–	–	5	μA
Low-side SW Leak Current	I_{LEAKL}	V_{SW} - PGND=5.5V	–	–	1	μA
Enable Control Block						
EN pin High Threshold Voltage	V_{THH_EN}	V_{EN}= L → H	1.0	–	5.5	V
EN pin Low Threshold Voltage	V_{THL_EN}	V_{EN}= H → L	0	–	0.4	V
EN pin Input Bias Current	I_{EN}	V_{EN}=5.5V	–	10	15	μA
MODE Control / Sync Block						
MODE/SYNC pin High Threshold Voltage	$V_{THH\_MODE/SYNC}$	$V_{MODE/SYNC}$= L → H	1.2	–	5.5	V
MODE/SYNC pin Low Threshold Voltage	$V_{THL\_MODE/SYNC}$	$V_{MODE/SYNC}$= H → L	0	–	0.4	V
MODE/SYNC pin Input Bias Current	$I_{MODE/SYNC}$	$V_{MODE/SYNC}$= 5.5V	–	10	15	μA

■ELECTRICAL CHARACTERISTICS (CONTINUED)

(Unless otherwise noted, $PV_{DD}=V^{+}=V_{EN}=3.3V$, PGND=GND, $R_T=6.8k\Omega$, Common to CH1 and CH2, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Good Block						
High Level Detection Voltage	V_{THH_PG}	Measured at FB pin, Rising	0.63	0.642	0.654	V
Low Level Detection Voltage	V_{THL_PG}	Measured at FB pin, Falling	0.558	0.57	0.582	V
Hysterisis Region	V_{HYS_PG}		–	12	–	mV
Power Good ON Resistance	R_{ON_PG}	I_{PG}=10mA	–	100	–	Ω
Leak Current at OFF State	I_{LEAK_PG}	V_{PG}=5.5V	–	–	0.1	μA
General Characteristics						
Quiescent Current1 (PWM Mode)	I_{DD1}	R_L= no load, Not Switching, $V_{MODE/SYNC}$=H, Both channel operation	–	3.8	5.0	mA
Quiescent Current2 (Light Load Mode)	I_{DD2}	R_L= no load, Not Switching, $V_{MODE/SYNC}$=L, Both channel operation	–	500	750	μA
Standby Current	I_{DD_STB}	$V_{EN1,2}$=0V, PV_{DD}=open	–	–	1	μA

■THERMAL CHARACTERISTICS

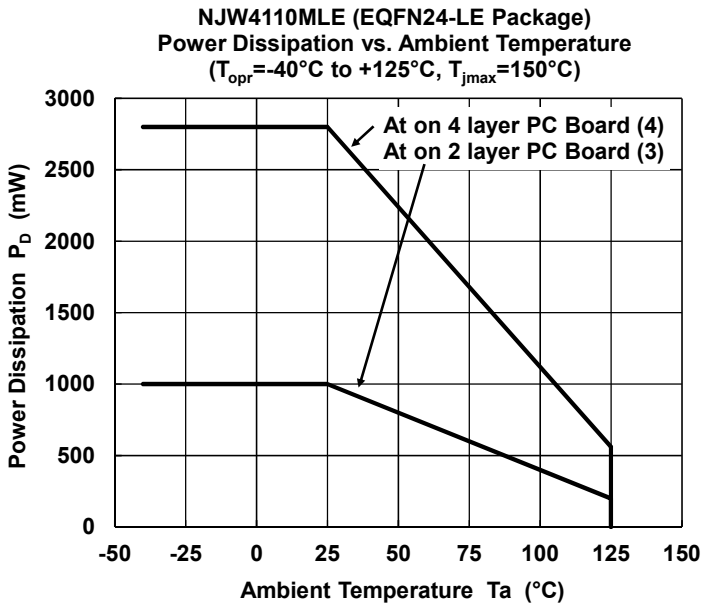
PARAMETER	SYMBOL	VALUE		UNIT
Junction-to-ambient thermal resistance	θja	EQFN24-LE	126(3) 45(4)	°C/W
Junction-to-Top of package characterization parameter	ψjt	EQFN24-LE	8.0(3) 2.8(4)	°C/W

(3): Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

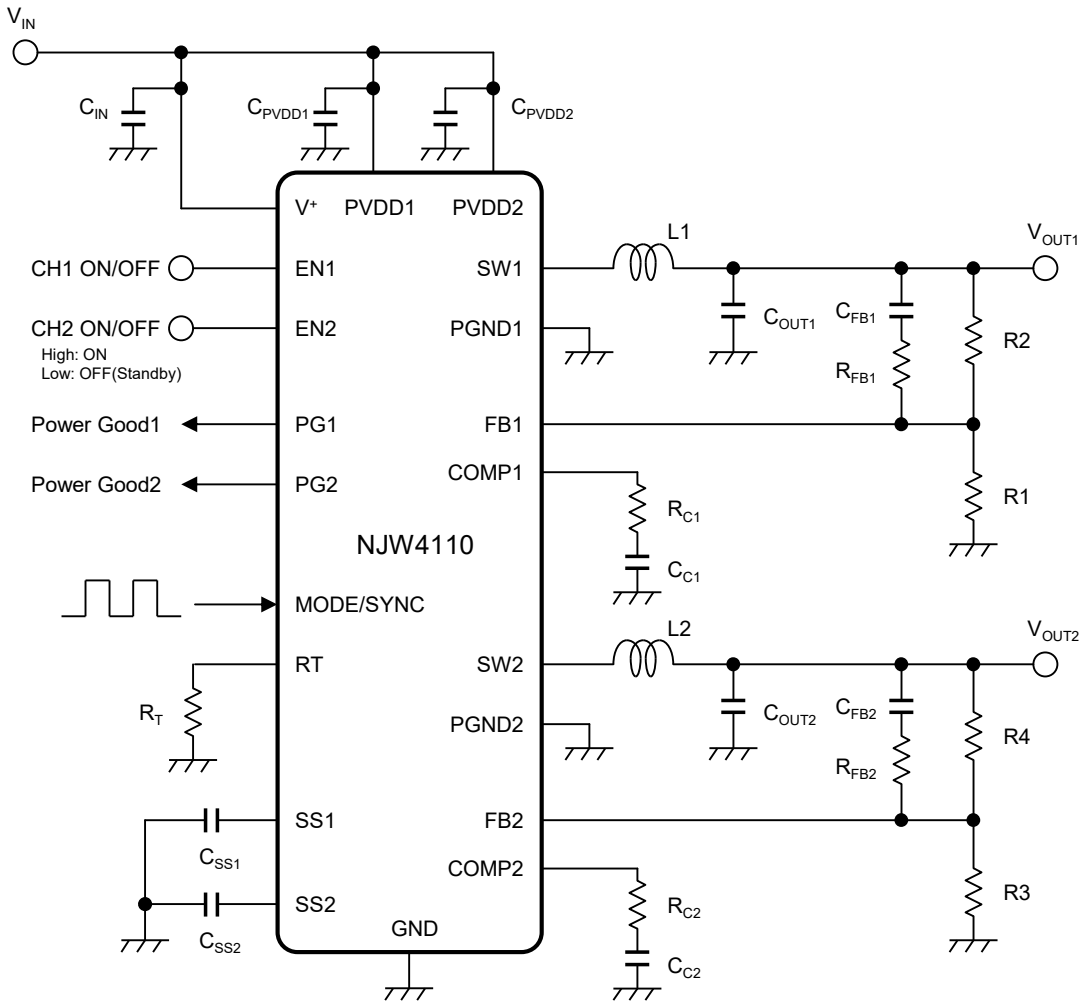
(4): Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)

(For 4Layers: Applying 99.5×99.5mm inner Cu area and thermal via holes to a board based on JEDEC standard JESD51-5)

■POWER DISSIPATION vs. AMBIENT TEMPERATURE



■TYPICAL APPLICATION

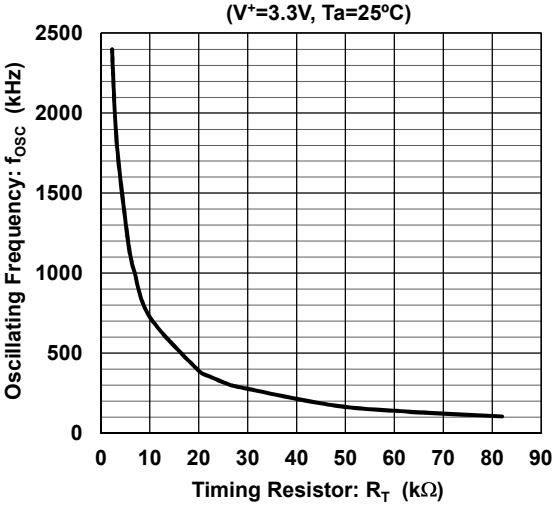


Operating mode select with the MODE/SYNC pin

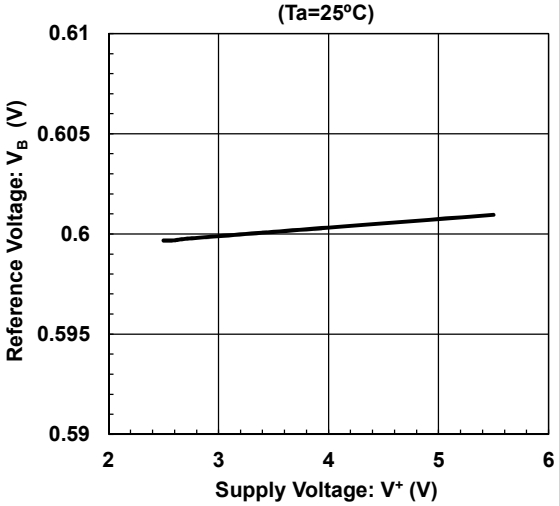
MODE/SYNC pin Voltage	Operating Mode	Oscillating Frequency
1.2V to 5.5V	Forced PWM operation	Internal frequency
0V to 0.4V	PWM/PFM operation for light loads	Internal frequency
External clock input	Forced PWM operation	External clock frequency

■TYPICAL CHARACTERISTICS

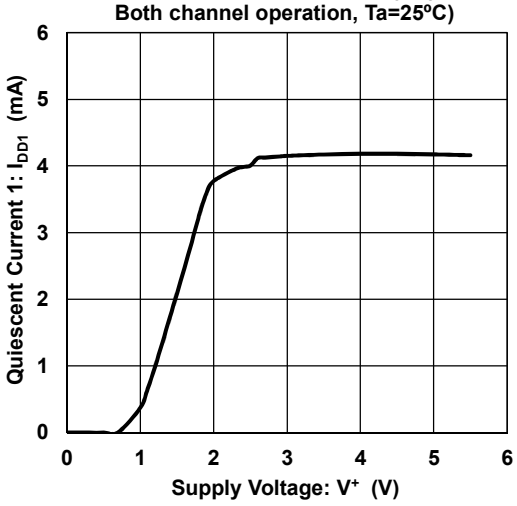
Timing Resistor vs. Oscillating Frequency
(V^+=3.3V, Ta=25°C)



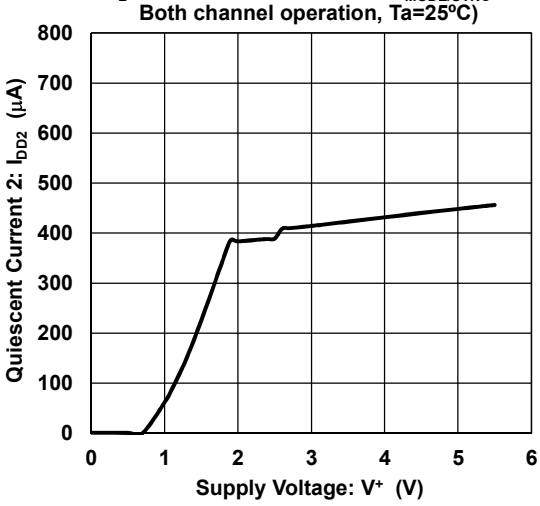
Reference Voltage vs. Supply Voltage
(Ta=25°C)



Quiescent Current 1 vs. Supply Voltage
(R_L=No Load, Not Switching, $V_{MODE/SYNC}$=H,
Both channel operation, Ta=25°C)

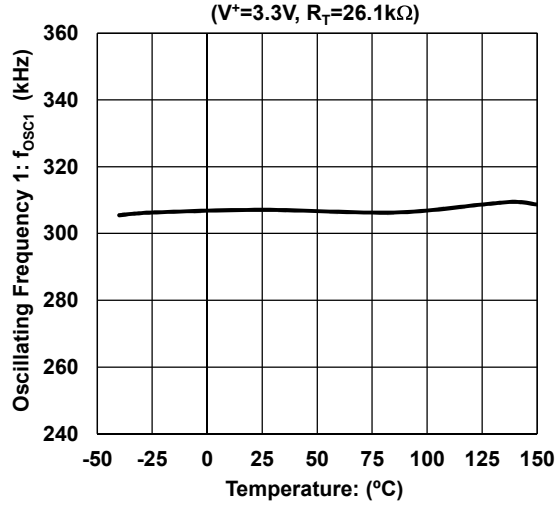


Quiescent Current 2 vs. Supply Voltage
(R_L=No Load, Not Switching, $V_{MODE/SYNC}$=L,
Both channel operation, Ta=25°C)

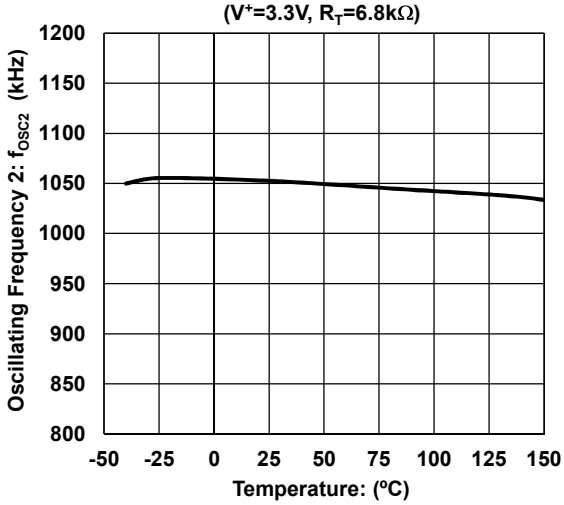


■TYPICAL CHARACTERISTICS

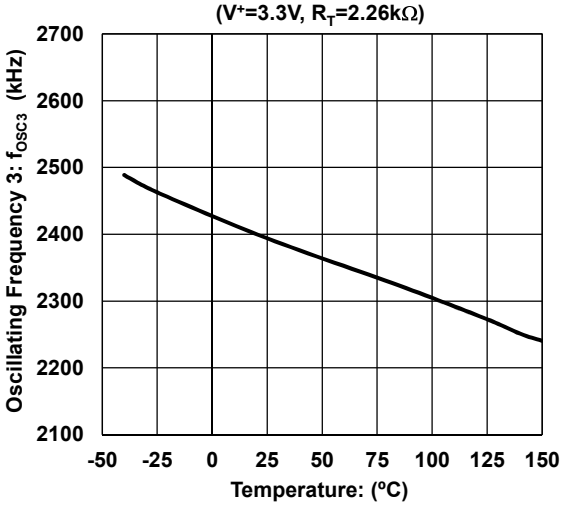
Oscillating Frequency 1 vs Temperature
(V^+=3.3V, R_T=26.1kΩ)



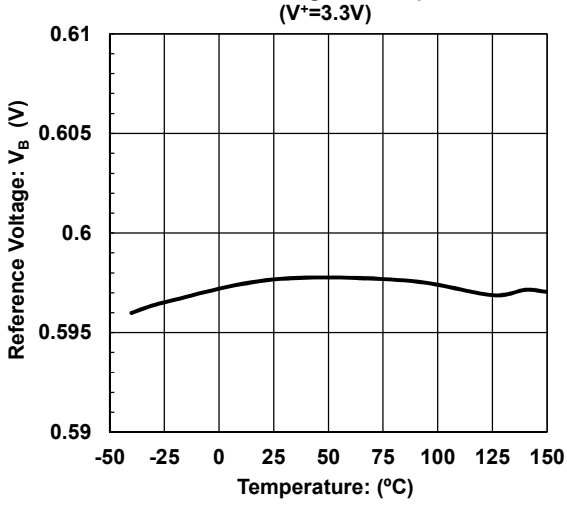
Oscillating Frequency 2 vs Temperature
(V^+=3.3V, R_T=6.8kΩ)



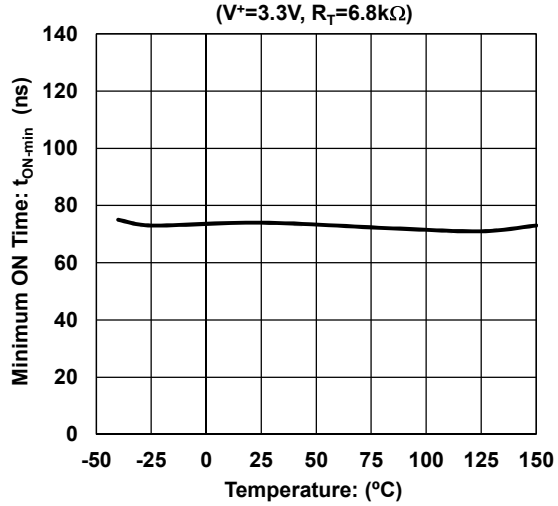
Oscillating Frequency 3 vs Temperature
(V^+=3.3V, R_T=2.26kΩ)



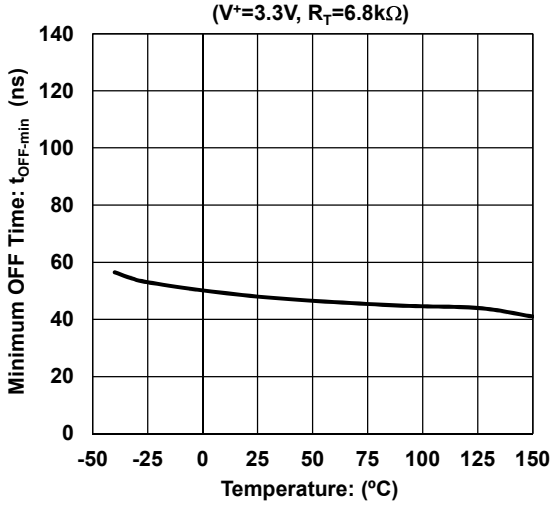
Reference Voltage vs. Temperature
(V^+=3.3V)



Minimum ON Time vs. Temperature
(V^+=3.3V, R_T=6.8kΩ)

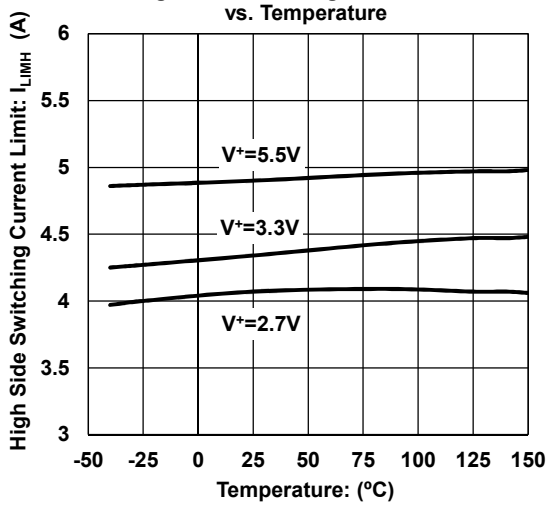


Minimum OFF Time vs. Temperature
(V^+=3.3V, R_T=6.8kΩ)

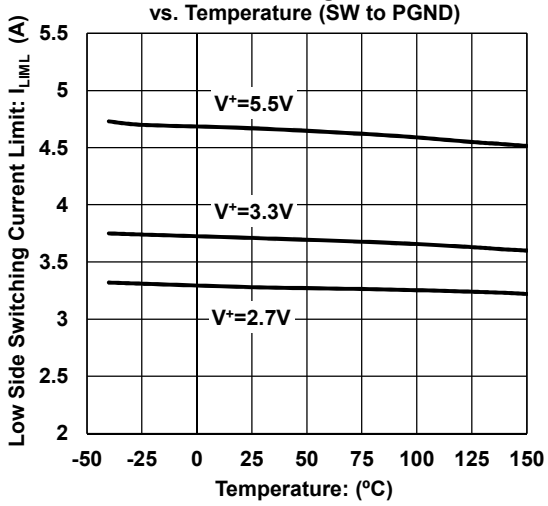


■TYPICAL CHARACTERISTICS

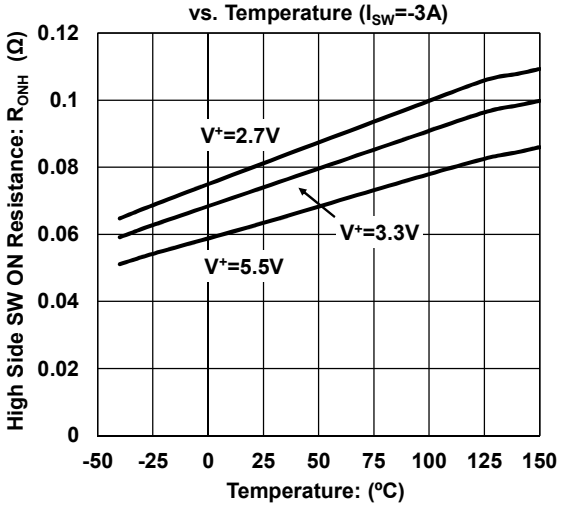
High Side Switching Current Limit vs. Temperature



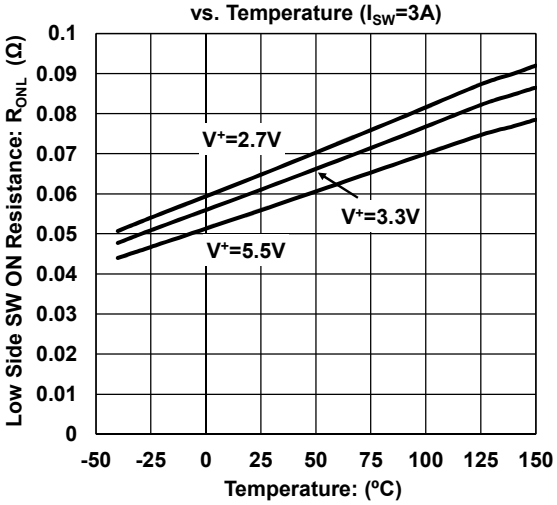
Low Side Switching Current Limit vs. Temperature (SW to PGND)



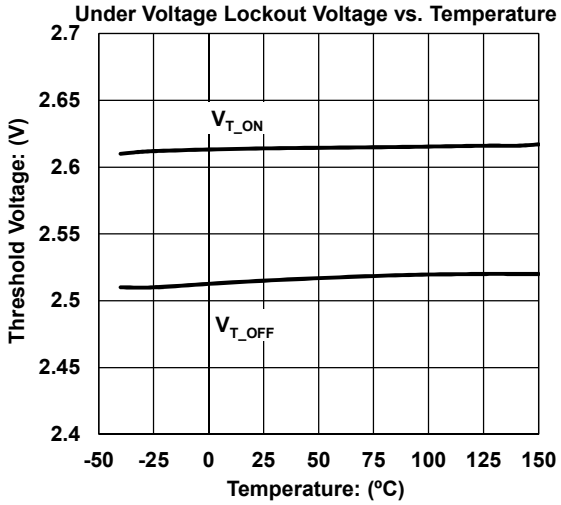
High Side SW ON Resistance vs. Temperature (I_{SW}=-3A)



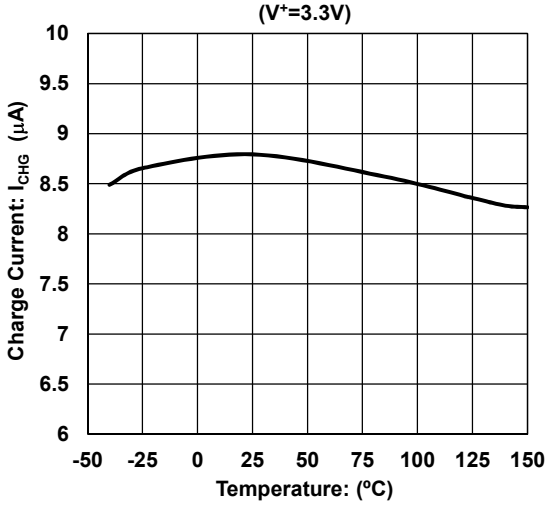
Low Side SW ON Resistance vs. Temperature (I_{SW}=3A)



Under Voltage Lockout Voltage vs. Temperature

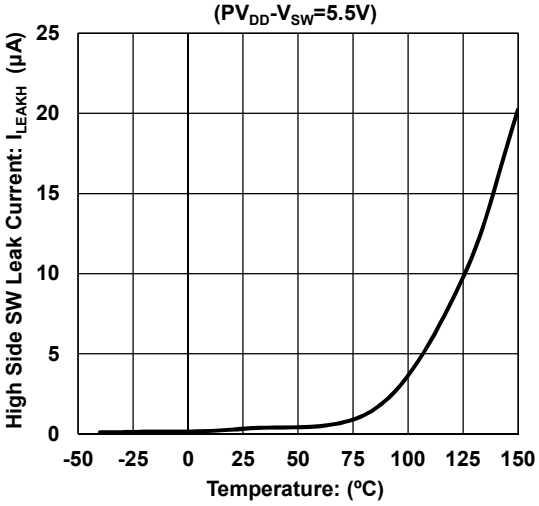


Charge Current vs. Temperature (V+=3.3V)

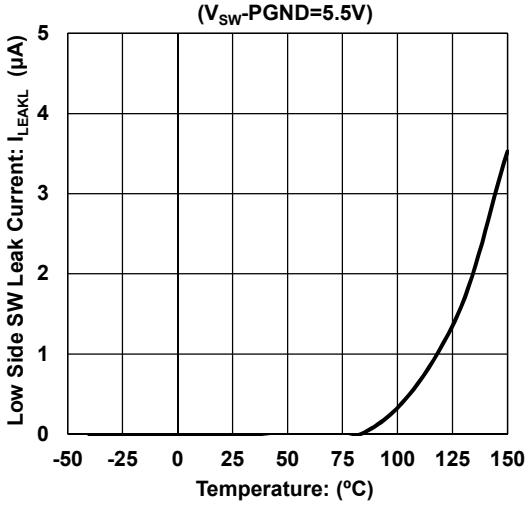


■TYPICAL CHARACTERISTICS

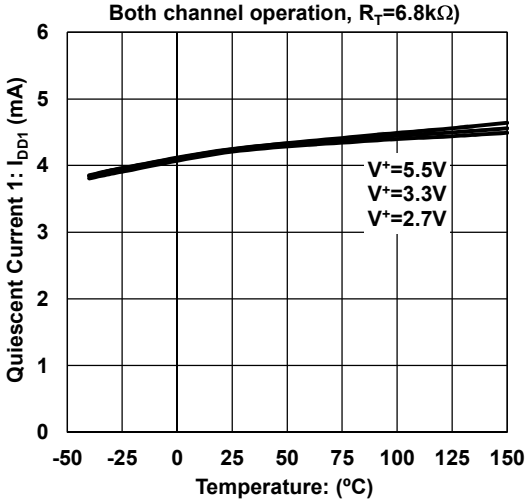
High Side SW Leak Current vs. Temperature
(PV_{DD}-V_{SW}=5.5V)



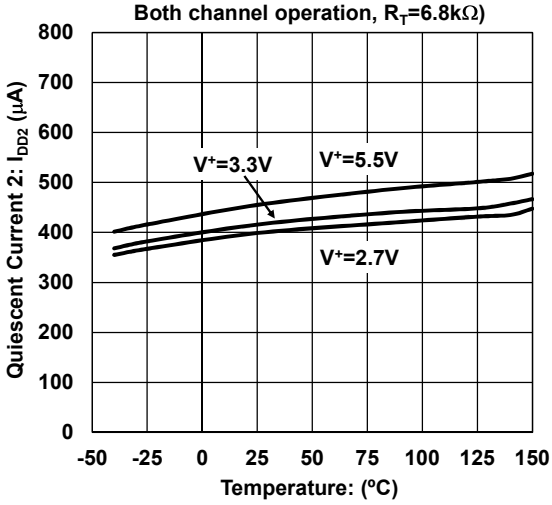
Low Side SW Leak Current vs. Temperature
(V_{SW}-PGND=5.5V)



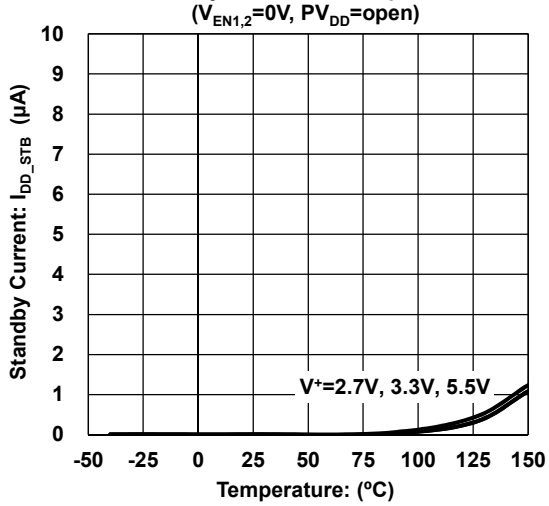
Quiescent Current 1 vs. Temperature
(R_L=No Load, Not Switching, $V_{MODE/SYNC}$=H,
Both channel operation, R_T=6.8kΩ)



Quiescent Current 2 vs. Temperature
(R_L=No Load, Not Switching, $V_{MODE/SYNC}$=L,
Both channel operation, R_T=6.8kΩ)



Standby Current vs. Temperature
($V_{EN1,2}$=0V, PV_{DD}=open)



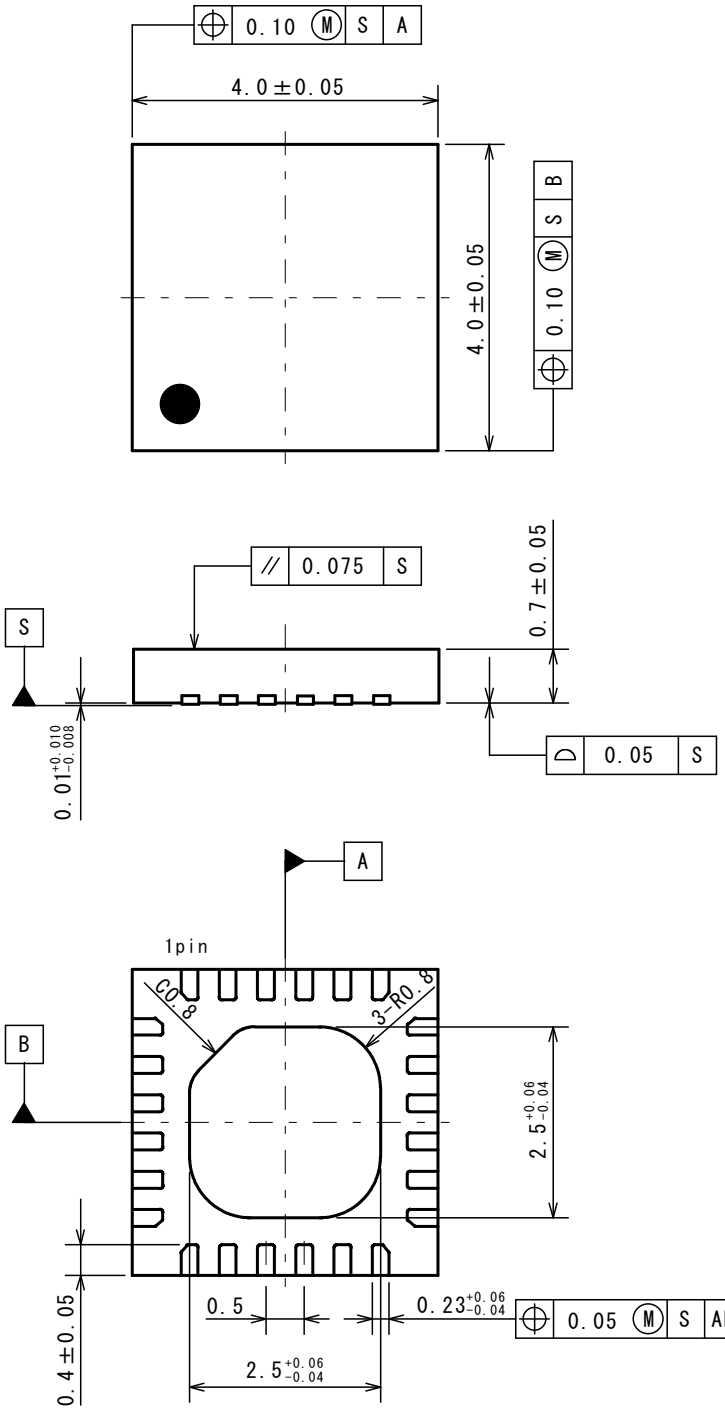
■ PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	FUNCTION
SS1	1	Soft Start timer setting pin of Ch.1. Soft start time is controlled by a capacitor.
RT	2	Oscillating Frequency Setting pin by Timing Resistor. Oscillating Frequency should set between 100kHz and 2.4MHz.
MODE/SYNC	3	Operating mode select pin. The MODE/SYNC pin internally pulls down resistor. Forced PWM operation at the time of High Level. PWM/PFM mode operation at the time of Low Level or OPEN. Moreover, it operates by inputting clock signal at the oscillatory frequency that synchronized with the input signal.
GND	4	GND pin
SS2	5	Soft Start timer setting pin of Ch.2. It has the same function as the SS1 pin.
PG2	6	Power Good pin of Ch.2. An open drain output that goes high impedance when the FB pin voltage is stable around +7% to -5%.
COMP2	7	Output pin of the Error Amplifier of Ch.2. A resistor and capacitors for compensation are connected between the COMP pin and the GND.
FB2	8	Output Voltage Detecting pin of Ch.2. Connects output voltage through the resistor divider tap to this pin in order to voltage of the FB pin become 0.6V.
EN2	9	Standby Control pin of Ch.2. The EN pin internally pulls down resistor. Normal Operation at the time of High Level. Standby Mode at the time of Low Level or OPEN.
V^+	10	Power Supply pin for IC control. Insert a bypass capacitor close to the V^+ pin – the GND pin connection in order to lower high frequency impedance.
PVDD2	11	Power Supply pin for Power Line of Ch.2.
PVDD2	12	
SW2	13	Switch Output pin of Power MOSFET of Ch.2.
PGND2	14	Power GND pin for Power Line of Ch.2.
PGND2	15	
PGND1	16	Power GND pin for Power Line of Ch.1.
PGND1	17	
SW1	18	Switch Output pin of Power MOSFET of Ch.1.
PVDD1	19	Power Supply pin for Power Line of Ch.1.
PVDD1	20	
EN1	21	Standby Control pin of Ch.1. It has the same function as the EN2 pin.
FB1	22	Output Voltage Detecting pin of Ch.1. It has the same function as the FB2 pin.
COMP1	23	Output pin of the Error Amplifier of Ch.1. It has the same function as the COMP2 pin.
PG1	24	Power Good pin of Ch.1. It has the same function as the PG2 pin.
Exposed PAD	–	Exposed PAD on backside should be connected to ground and soldered to PCB.

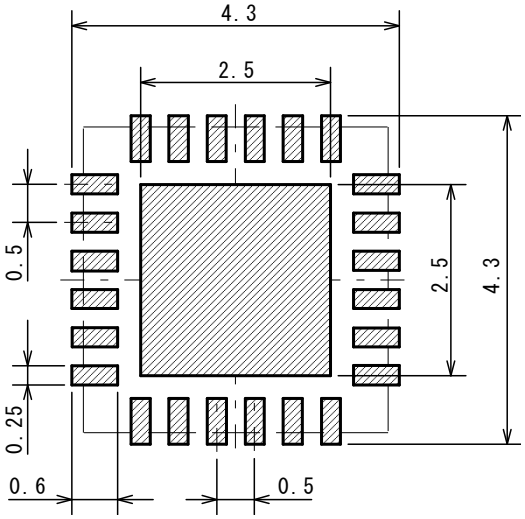
EQFN24-LE

Unit: mm

■PACKAGE DIMENSIONS



■EXAMPLE OF SOLDER PADS DIMENSIONS

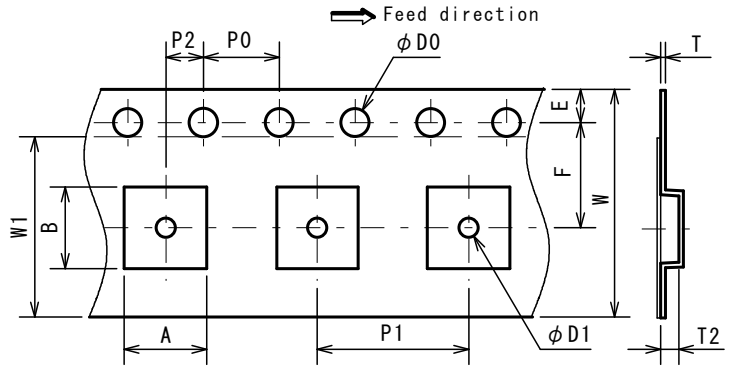


EQFN24-LE

■PACKING SPEC

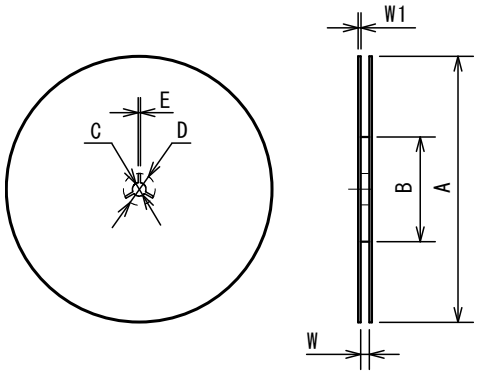
Unit: mm

TAPING DIMENSIONS



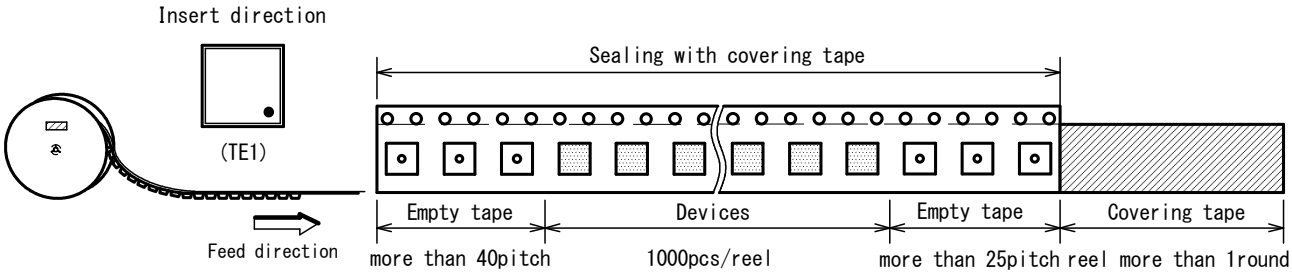
SYMBOL	DIMENSION	REMARKS
A	4.35±0.05	BOTTOM DIMENSION
B	4.35±0.05	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	1.0±0.1	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.1	
T	0.3±0.05	
T2	1.3±0.05	
W	12.0±0.3	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

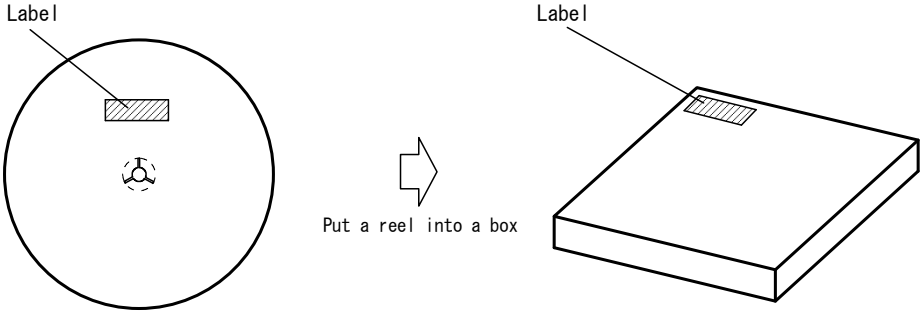


SYMBOL	DIMENSION
A	$\phi 180^{0}_{-1.5}$
B	$\phi 60^{+1}_{0}$
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	$13^{+1.0}_{0}$
W1	1.2

TAPING STATE



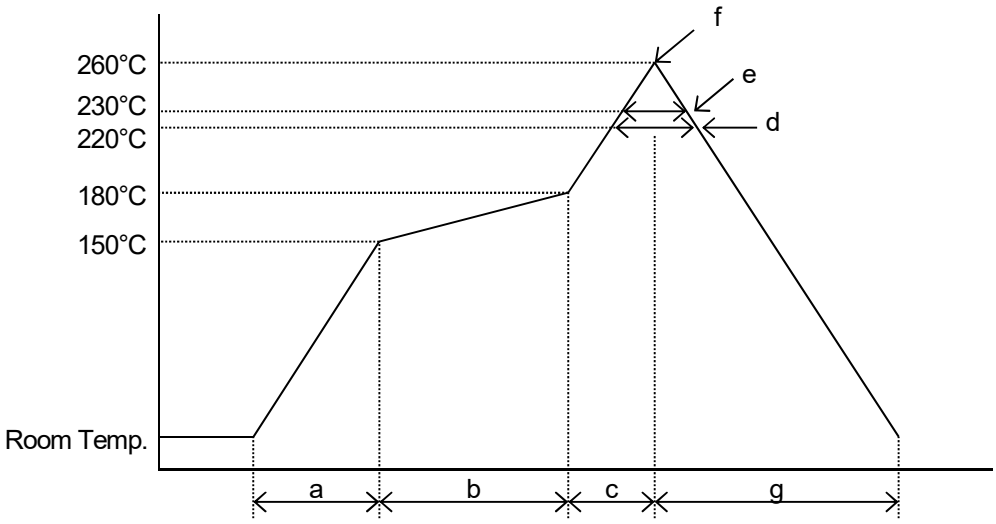
PACKING STATE



■MOUNTING METHOD

INFRARED REFLOW SOLDERING METHOD

Recommended reflow soldering procedure



a : Temperature ramping rate	: 1 to 4°C /s
b : Pre-heating temperature	: 150 to 180°C
time	: 60 to 120s
c : Temperature ramp rate	: 1 to 4°C /s
d : 220°C or higher time	: Shorter than 60s
e : 230°C or higher time	: Shorter than 40s
f : Peak temperature	: Lower than 260°C
g : Temperature ramping rate	: 1 to 6°C /s

The temperature indicates at the surface of mold package.

■REVISION HISTORY

DATE	REVISION	CHANGES
21.Aug.2017	Ver.1.0	New Release

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