



PSMN2R1-30YLE

N-channel 30 V, 2.2 mOhm, ASFET for hotswap with enhanced SOA in LFPAK56

10 November 2022

Product data sheet

1. General description

N-channel enhancement mode ASFET for hotswap with enhanced SOA in LFPAK56 package optimized for low R_{DSon} and strong safe operating area, optimized for hot-swap, inrush and linear-mode applications.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Optimized for low R_{DSon} / low I^2R conduction losses
- LFPAK56 package for applications that demand the highest performance and reliability in a 30 mm² footprint
- Low leakage <1 μ A at 25 °C
- Copper-clip for low parasitic inductance and resistance
- High reliability LFPAK package, qualified to 175 °C

3. Applications

- Hot swap in 12 V - 20 V applications
- e-Fuse
- DC switch
- Load switch
- Battery protection

4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|---|-----|------|------|------|
| V_{DS} | drain-source voltage | $25\text{ °C} \leq T_j \leq 175\text{ °C}$ | - | - | 30 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2 | [1] | - | 160 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Fig. 1 | - | - | 124 | W |
| T_j | junction temperature | | -55 | - | 175 | °C |
| Static characteristics | | | | | | |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10 | - | 1.87 | 2.17 | mΩ |
| | | $V_{GS} = 7\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10 | - | 2.32 | 2.8 | mΩ |
| Dynamic characteristics | | | | | | |
| Q_{GD} | gate-drain charge | $I_D = 25\text{ A}$; $V_{DS} = 15\text{ V}$; $V_{GS} = 4.5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 12 ; Fig. 13 | 1 | 6 | 12 | nC |
| $Q_{G(tot)}$ | total gate charge | | 8 | 17 | 28 | nC |

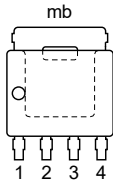
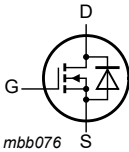
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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|-----------------|---|-----|------|-----|------|
| Source-drain diode | | | | | | |
| S | softness factor | $I_S = 25 \text{ A}$; $di_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 15 \text{ V}$; $T_J = 25 \text{ }^\circ\text{C}$; Fig. 16 | - | 0.99 | - | |

[1] 160 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|---|---|
| 1 | S | source |  <p>LFAK56; Power-SO8 (SOT669)</p> |  <p>mbb076</p> |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|---------------|-------------------|--|---------|
| | Name | Description | Version |
| PSMN2R1-30YLE | LFAK56; Power-SO8 | plastic, single-ended surface-mounted package; 4 terminals | SOT669 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|---------------|--------------|
| PSMN2R1-30YLE | 2E1L30Y |

8. Limiting values

Table 5. Limiting values

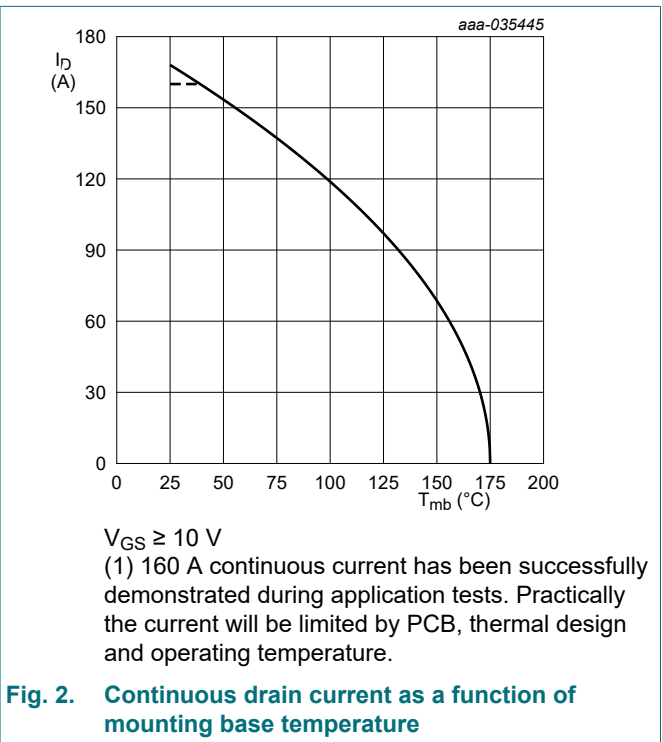
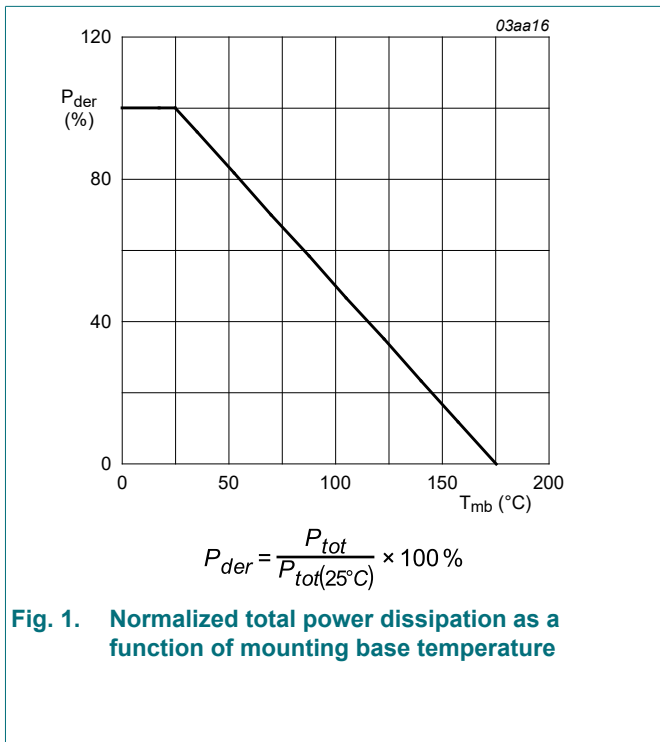
In accordance with the Absolute Maximum Rating System (IEC 60134). $T_J = 25 \text{ }^\circ\text{C}$ unless otherwise stated.

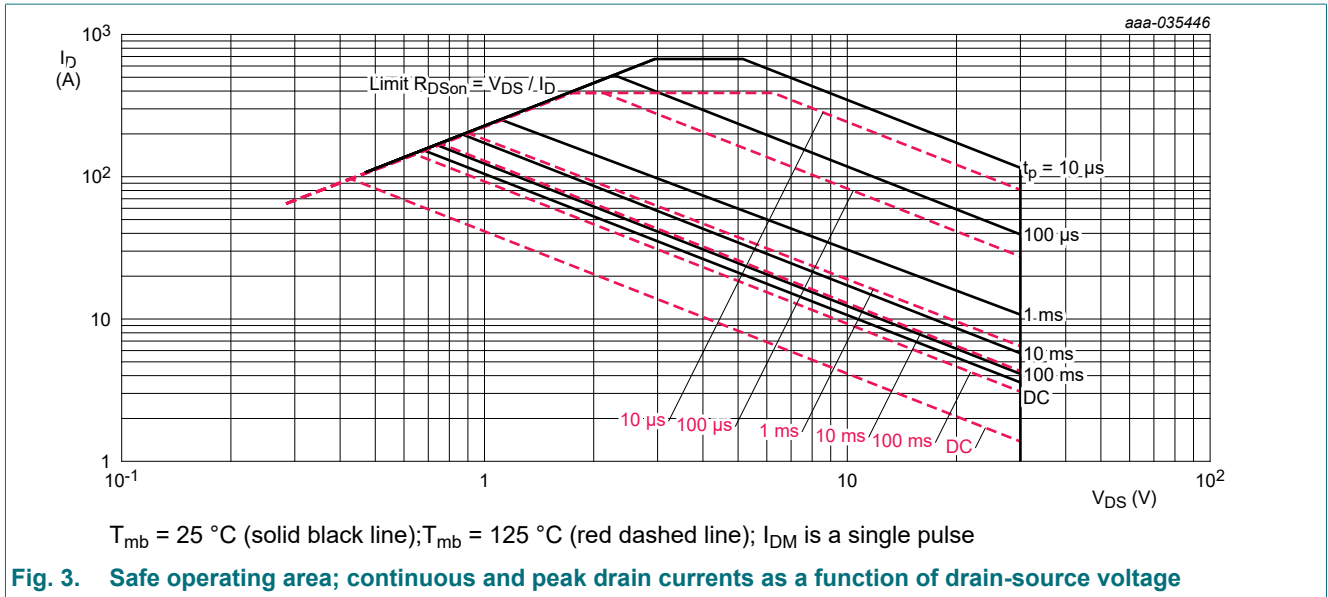
| Symbol | Parameter | Conditions | Min | Max | Unit | |
|-----------|-------------------------|---|-----|-----|------------------|---|
| V_{DS} | drain-source voltage | $25 \text{ }^\circ\text{C} \leq T_J \leq 175 \text{ }^\circ\text{C}$ | - | 30 | V | |
| V_{DGR} | drain-gate voltage | $25 \text{ }^\circ\text{C} \leq T_J \leq 175 \text{ }^\circ\text{C}$; $R_{GS} = 20 \text{ k}\Omega$ | - | 30 | V | |
| V_{GS} | gate-source voltage | | -20 | 20 | V | |
| P_{tot} | total power dissipation | $T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 1 | - | 124 | W | |
| I_D | drain current | $V_{GS} = 10 \text{ V}$; $T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 2 | [1] | - | 160 | A |
| | | $V_{GS} = 10 \text{ V}$; $T_{mb} = 100 \text{ }^\circ\text{C}$; Fig. 2 | | - | 119 | A |
| I_{DM} | peak drain current | pulsed; $t_p \leq 10 \text{ }\mu\text{s}$; $T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 3 | - | 672 | A | |
| T_{stg} | storage temperature | | -55 | 175 | $^\circ\text{C}$ | |
| T_J | junction temperature | | -55 | 175 | $^\circ\text{C}$ | |

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| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------------|--|--|-----|-----|------|
| $T_{\text{slid(M)}}$ | peak soldering temperature | | - | 260 | °C |
| Source-drain diode | | | | | |
| I_S | source current | $T_{\text{mb}} = 25\text{ °C}$ | - | 124 | A |
| I_{SM} | peak source current | pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{\text{mb}} = 25\text{ °C}$ | - | 672 | A |
| Avalanche ruggedness | | | | | |
| $E_{\text{DS(AL)S}}$ | non-repetitive drain-source avalanche energy | $I_D = 25\text{ A}$; $V_{\text{sup}} \leq 30\text{ V}$; $R_{\text{GS}} = 50\text{ }\Omega$; $V_{\text{GS}} = 10\text{ V}$; $T_{\text{j(init)}} = 25\text{ °C}$; unclamped; $t_p = 634\text{ }\mu\text{s}$ | [2] | 309 | mJ |
| I_{AS} | non-repetitive avalanche current | $V_{\text{sup}} \leq 30\text{ V}$; $V_{\text{GS}} = 10\text{ V}$; $T_{\text{j(init)}} = 25\text{ °C}$; $R_{\text{GS}} = 50\text{ }\Omega$ | [2] | 80 | A |

- [1] 160 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test.

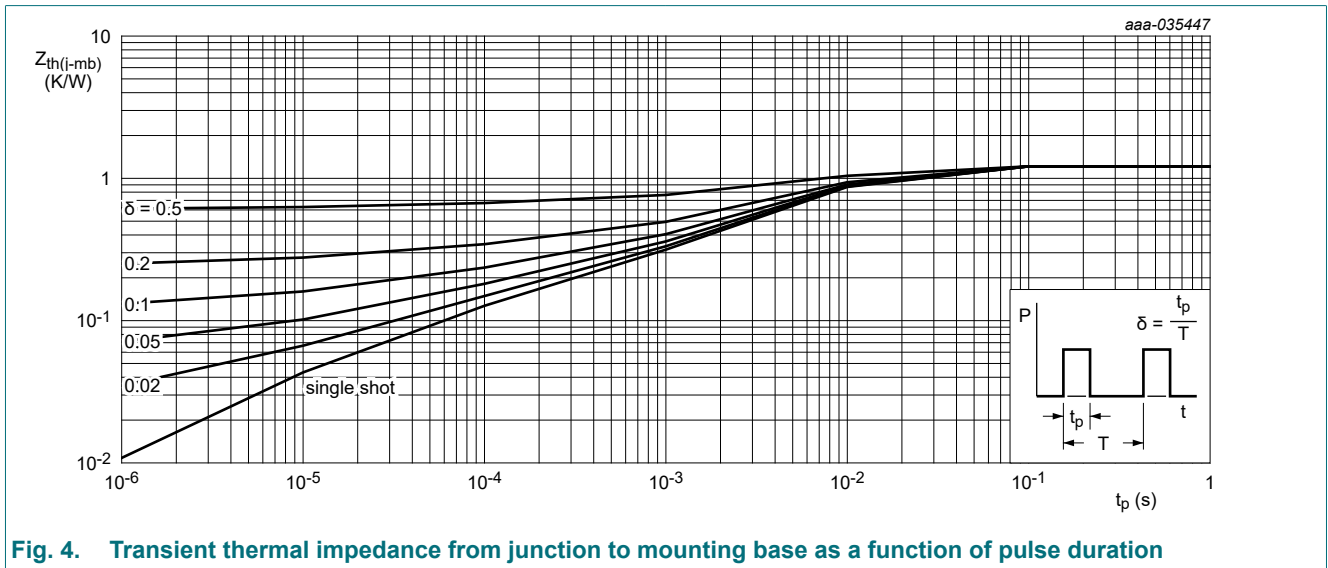


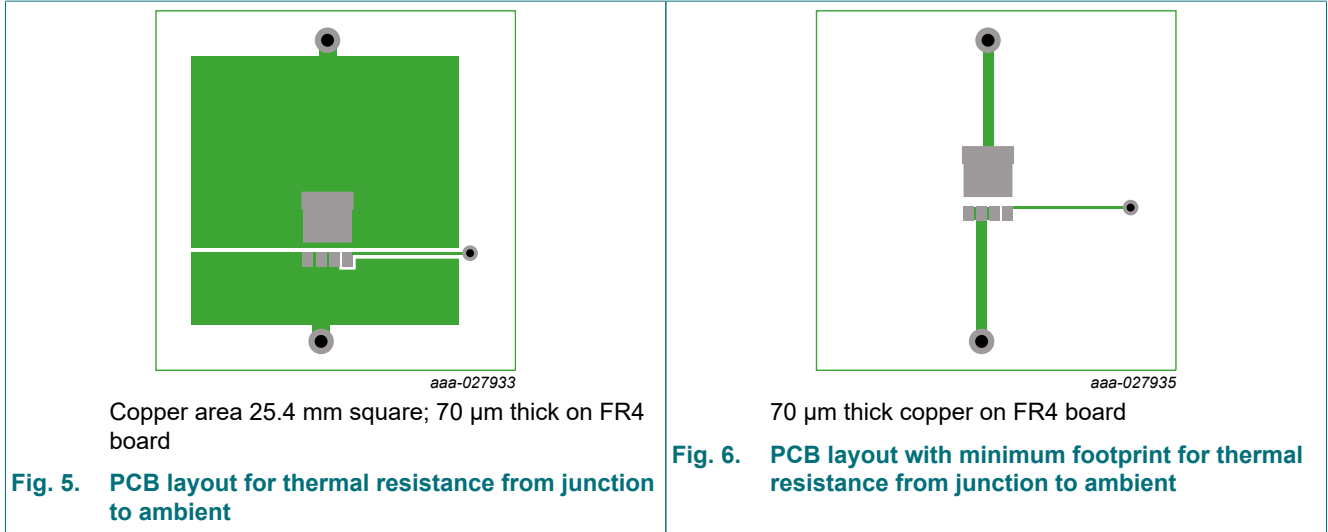


9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|------------|-----|------|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 4 | - | 0.69 | 1.21 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Fig. 5 | - | 42 | - | K/W |
| | | Fig. 6 | - | 85 | - | K/W |





10. Characteristics

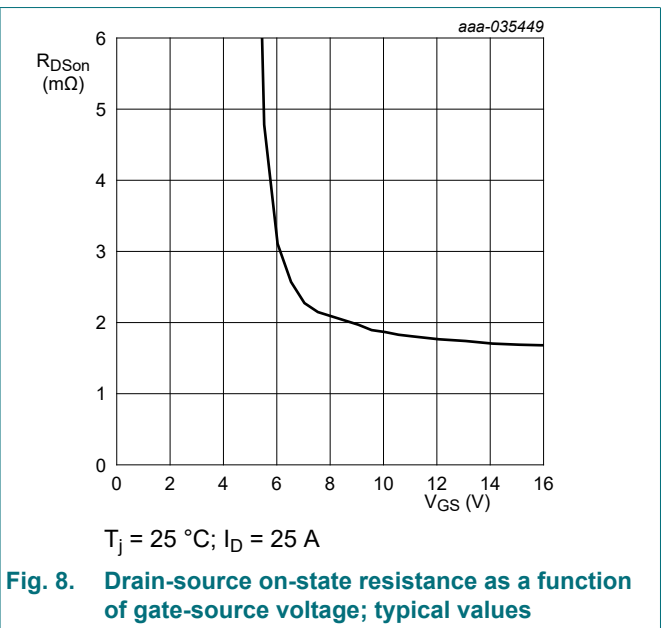
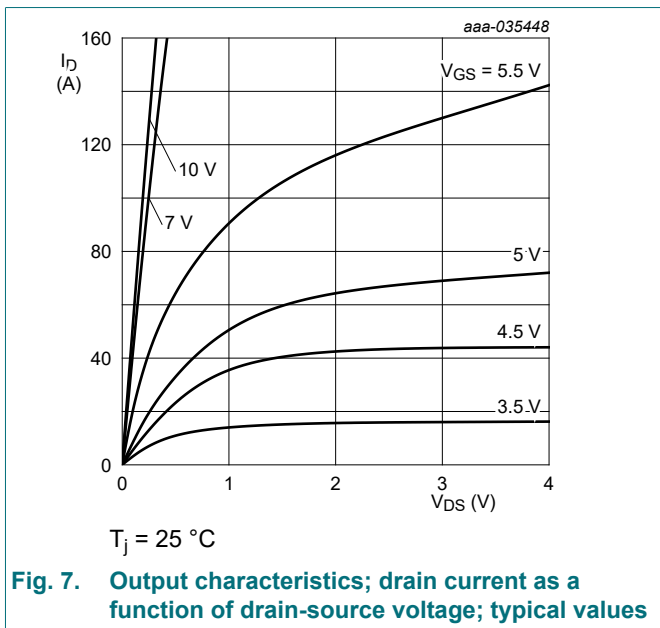
Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--|--|-----|------|------|------------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | 30 | - | - | V |
| | | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$ | 27 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ | 1.2 | 1.91 | 2.2 | V |
| $\Delta V_{GS(th)}/\Delta T$ | gate-source threshold voltage variation with temperature | $25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$ | - | -3.3 | - | mV/K |
| I_{DSS} | drain leakage current | $V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | - | 1 | μA |
| | | $V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$ | - | 2.5 | - | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | - | 100 | nA |
| | | $V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | - | 100 | nA |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 10 | - | 1.87 | 2.17 | m Ω |
| | | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ Fig. 11 | - | - | 4 | m Ω |
| | | $V_{GS} = 7 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 10 | - | 2.32 | 2.8 | m Ω |
| | | $V_{GS} = 7 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ Fig. 11 | - | - | 5.1 | m Ω |
| R_G | gate resistance | $f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$ | 1 | 2.6 | 6.5 | Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ $T_j = 25 \text{ }^\circ C;$ Fig. 12 ; Fig. 13 | 8 | 17 | 28 | nC |
| | | $I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ C;$ Fig. 12 ; Fig. 13 | 18 | 39 | 64 | nC |
| | | $I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ C$ | - | 21 | - | nC |

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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|-----------------------------------|--|------|------|------|------|
| Q_{GS} | gate-source charge | $I_D = 25\text{ A}; V_{DS} = 15\text{ V}; V_{GS} = 4.5\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 12 ; Fig. 13 | 2 | 9 | 17 | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | 1 | 4 | 8 | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | 1 | 5 | 10 | nC |
| Q_{GD} | gate-drain charge | | 1 | 6 | 12 | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D = 25\text{ A}; V_{DS} = 15\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 12 ; Fig. 13 | - | 3.8 | - | V |
| C_{iss} | input capacitance | $V_{DS} = 15\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C};$ Fig. 14 | 1499 | 2499 | 3749 | pF |
| C_{oss} | output capacitance | | 745 | 1242 | 1863 | pF |
| C_{rss} | reverse transfer capacitance | | 45 | 166 | 398 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 15\text{ V}; R_L = 0.6\text{ }\Omega; V_{GS} = 4.5\text{ V}; R_{G(ext)} = 5\text{ }\Omega; T_j = 25\text{ }^\circ\text{C}$ | - | 23 | - | ns |
| t_r | rise time | | - | 74 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 14 | - | ns |
| t_f | fall time | | - | 18 | - | ns |
| Q_{oss} | output charge | $V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C}$ | - | 26 | - | nC |
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 15 | - | 0.81 | 1 | V |
| t_{rr} | reverse recovery time | $I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 16 | - | 25 | - | ns |
| Q_r | recovered charge | | [1] | 15 | - | nC |
| t_a | reverse recovery rise time | | - | 12.5 | - | ns |
| t_b | reverse recovery fall time | | - | 12.4 | - | ns |
| S | softness factor | | - | 0.99 | - | |

[1] includes capacitive recovery



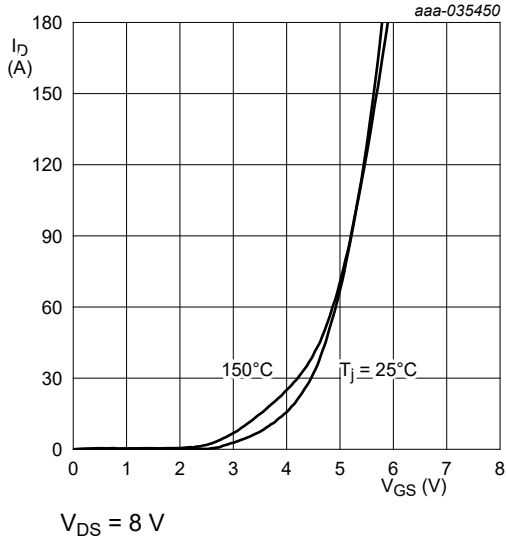


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

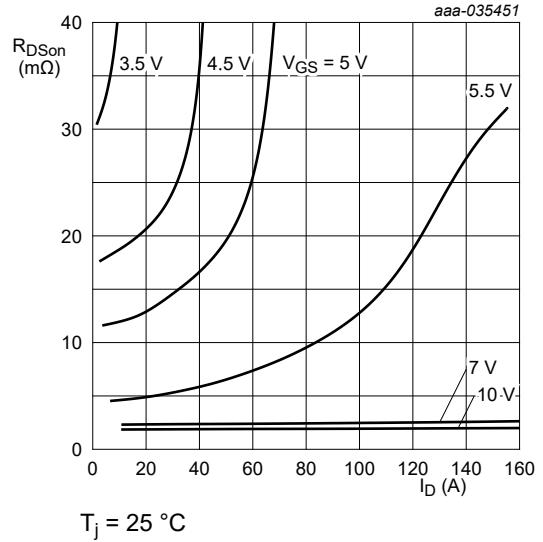


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

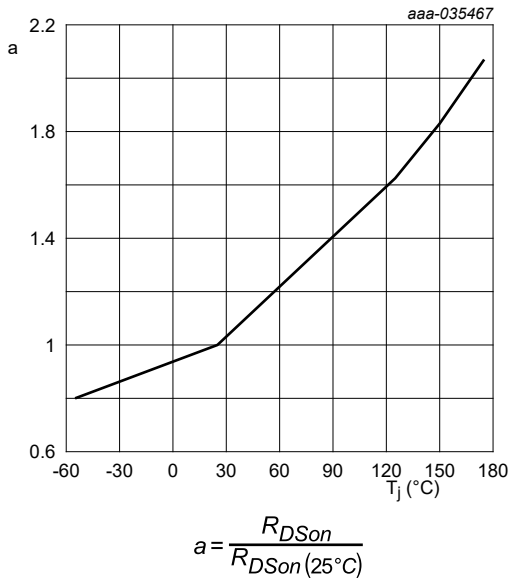


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

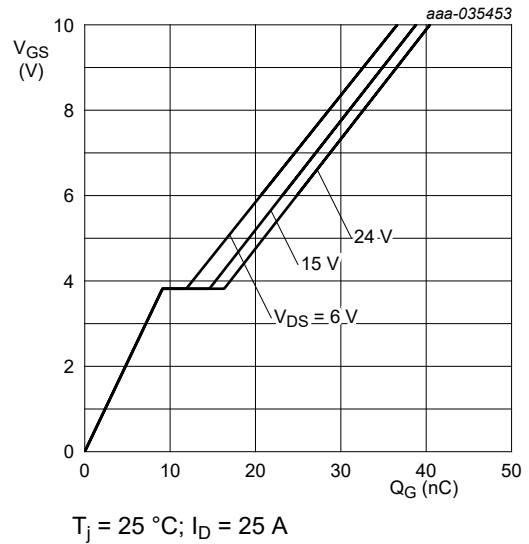


Fig. 12. Gate-source voltage as a function of gate charge; typical values

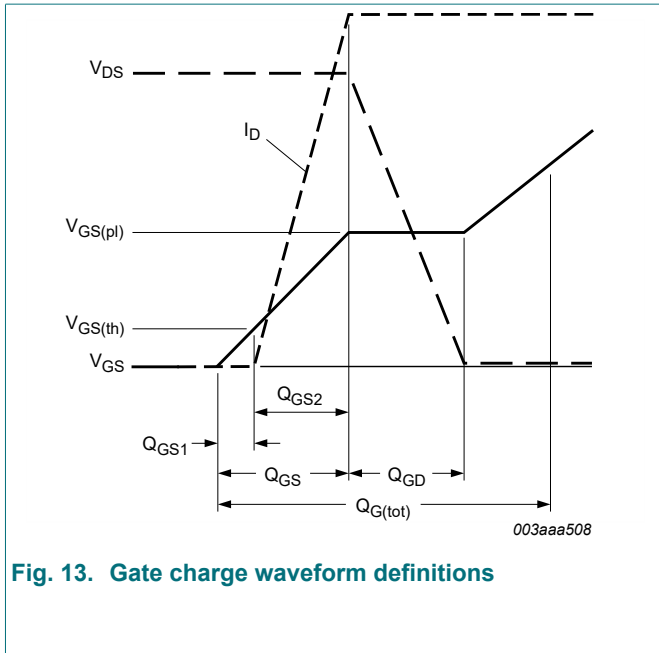


Fig. 13. Gate charge waveform definitions

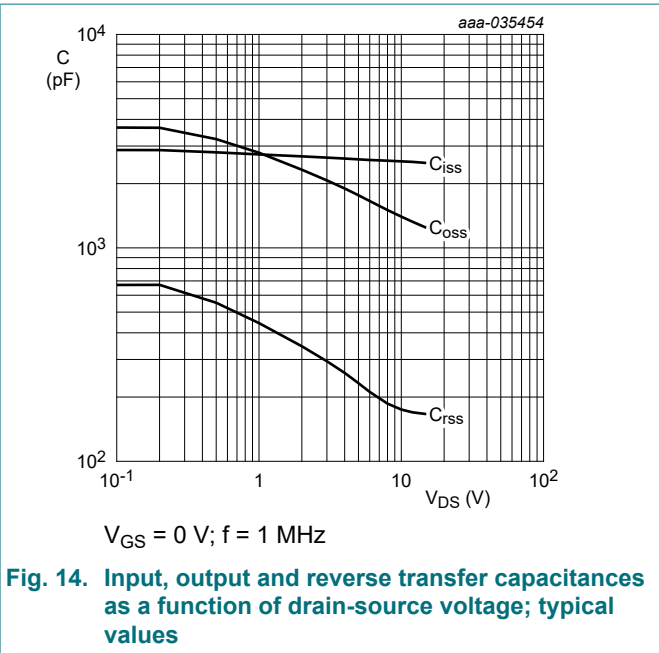


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

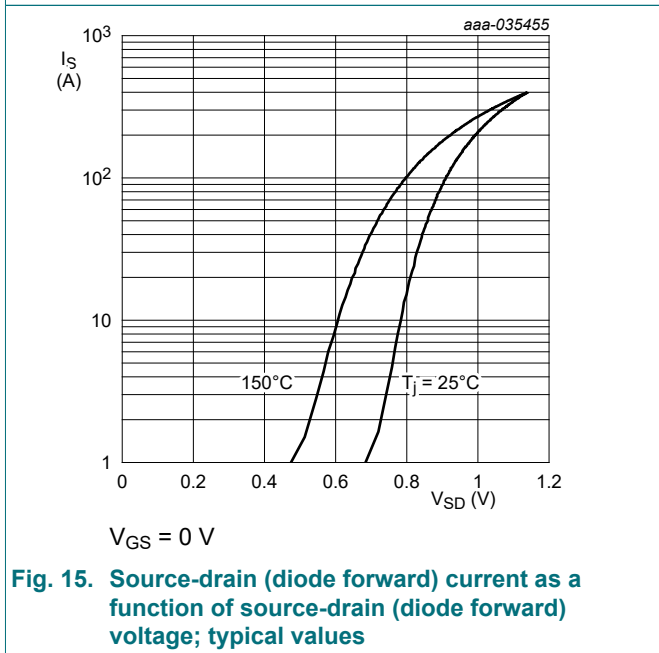


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

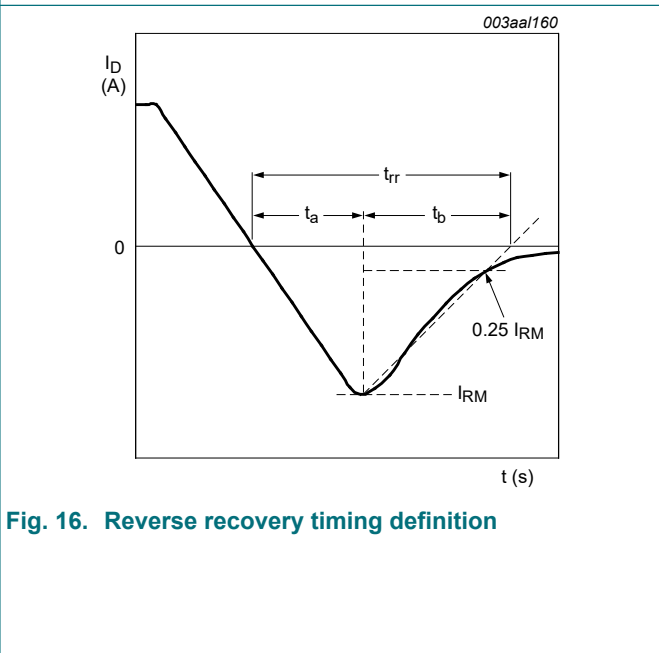


Fig. 16. Reverse recovery timing definition

11. Package outline

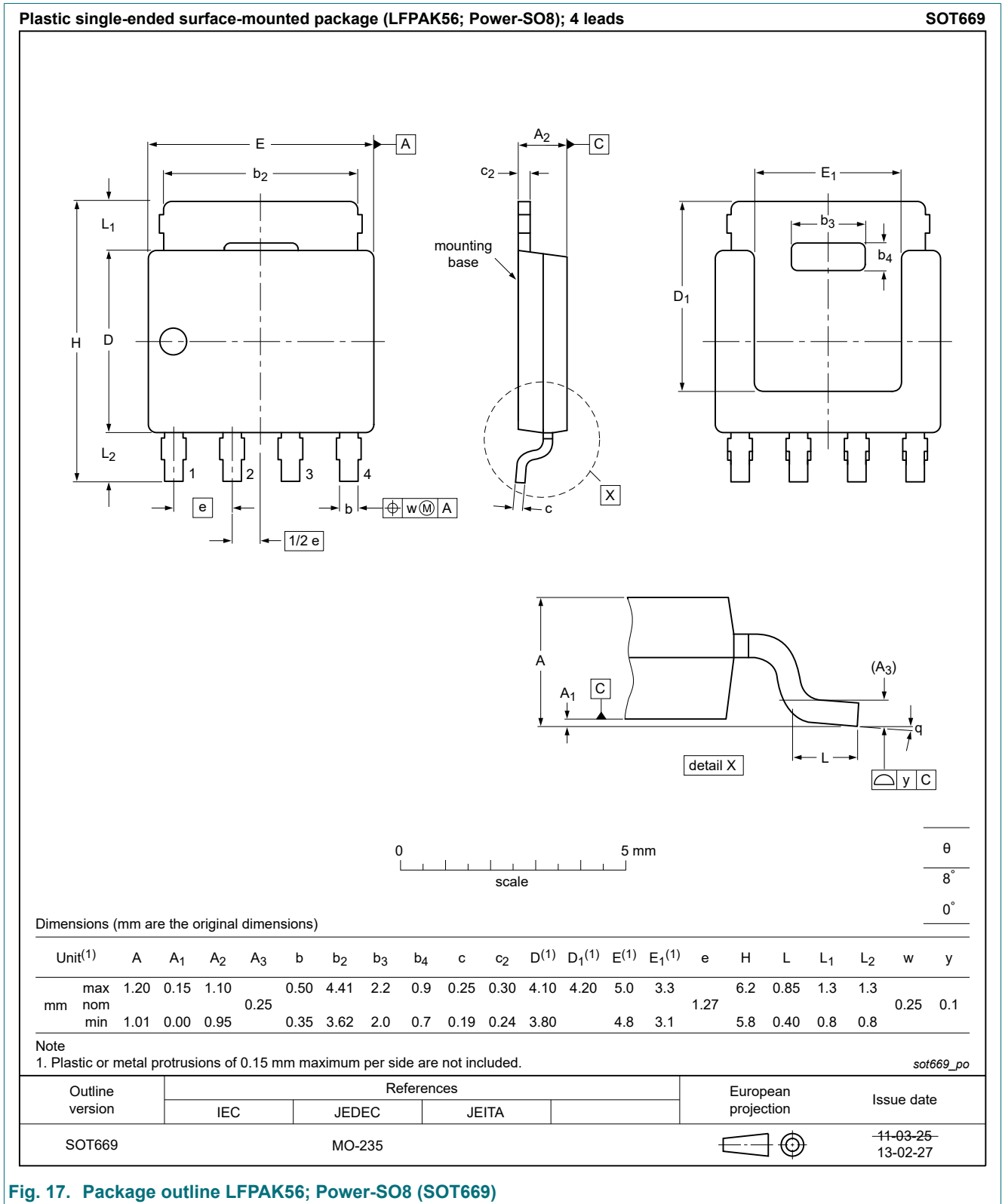


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering

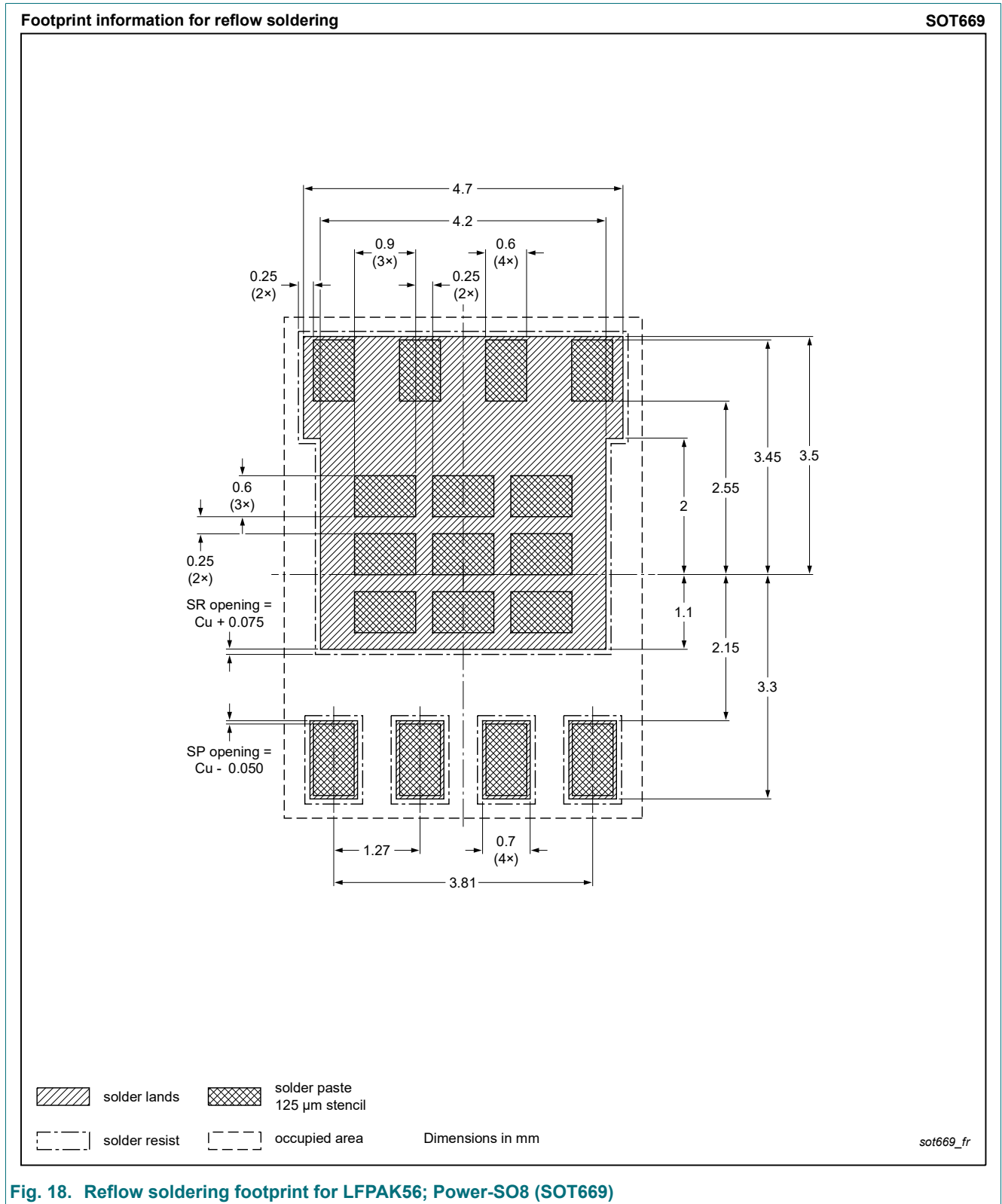
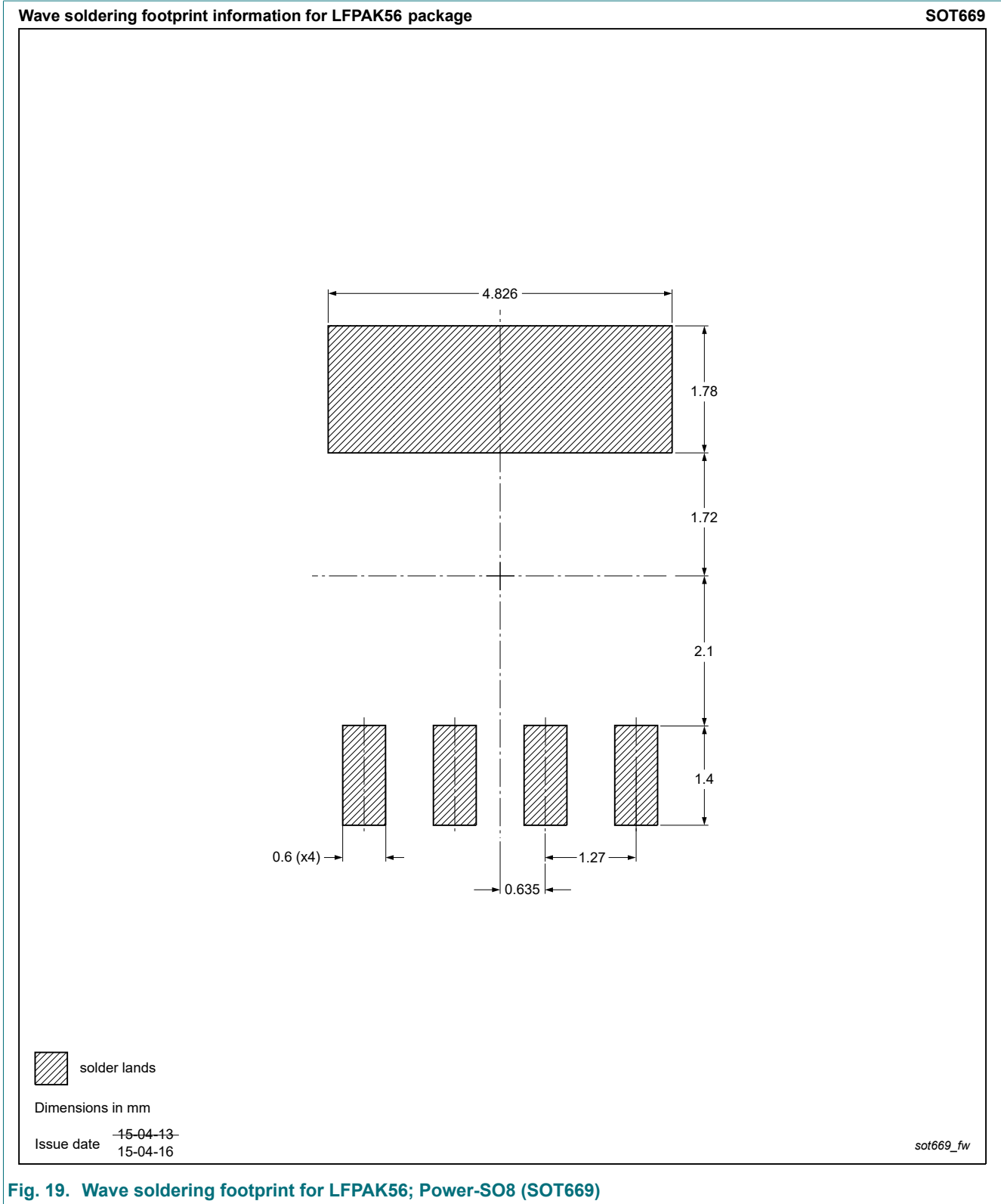


Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)



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|--------------------------------|--------------------|---|
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