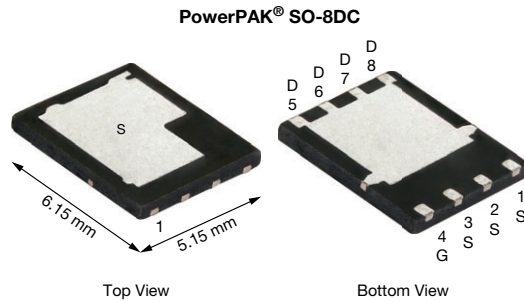


## N-Channel 25 V (D-S) MOSFET



### FEATURES

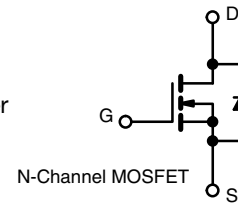
- TrenchFET® Gen IV power MOSFET
- Optimized  $Q_g$ ,  $Q_{gd}$ , and  $Q_{gd}/Q_{gs}$  ratio reduces switching related power loss
- Top side cooling feature provides additional venue for thermal transfer
- 100 %  $R_{\theta g}$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- Synchronous buck converter
- OR-ing
- Load switching
- Battery management



| PRODUCT SUMMARY                                    |                     |
|--|---------------------|
| $V_{DS}$ (V)                                       | 25                  |
| $R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V  | 0.00058             |
| $R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V | 0.00082             |
| $Q_g$ typ. (nC)                                    | 61                  |
| $I_D$ (A)  | 100 <sup>a, g</sup> |
| Configuration                                      | Single              |

| ORDERING INFORMATION            |                  |
|---------------------------------|------------------|
| Package                         | PowerPAK SO-8DC  |
| Lead (Pb)-free and halogen-free | SiDR220DP-T1-GE3 |

| ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted) |                |               |                      |
|---|----------------|---------------|----------------------|
| PARAMETER   | SYMBOL         | LIMIT         | UNIT                 |
| Drain-source voltage  | $V_{DS}$       | 25            | V                    |
| Gate-source voltage   | $V_{GS}$       | +16 / -12     |                      |
| Continuous drain current ( $T_J = 150$ °C)                        | $I_D$          | $T_C = 25$ °C | 100 <sup>a</sup>     |
|   |                | $T_C = 70$ °C | 100 <sup>a</sup>     |
|   |                | $T_A = 25$ °C | 87.7 <sup>b, c</sup> |
|   |                | $T_A = 70$ °C | 70.2 <sup>b, c</sup> |
| Pulsed drain current ( $t = 100$ $\mu$ s)                         | $I_{DM}$       | 500           | A                    |
| Continuous source-drain diode current                             | $I_S$          | $T_C = 25$ °C | 100                  |
|   |                | $T_A = 25$ °C | 5.6 <sup>b, c</sup>  |
| Single pulse avalanche current                                    | $I_{AS}$       | 60            |                      |
| Single pulse avalanche energy                                     | $E_{AS}$       | 180           | mJ                   |
| Maximum power dissipation   | $P_D$          | $T_C = 25$ °C | 125                  |
|   |                | $T_C = 70$ °C | 80                   |
|   |                | $T_A = 25$ °C | 6.25 <sup>b, c</sup> |
|   |                | $T_A = 70$ °C | 4 <sup>b, c</sup>    |
| Operating junction and storage temperature range                  | $T_J, T_{stg}$ | -55 to +150   | °C                   |
| Soldering recommendations (peak temperature) <sup>c</sup>         |                | 260           |                      |

| THERMAL RESISTANCE RATINGS               |            |         |         |      |
|--|------------|---------|---------|------|
| PARAMETER                                | SYMBOL     | TYPICAL | MAXIMUM | UNIT |
| Maximum junction-to-ambient <sup>b</sup> | $R_{thJA}$ | 15      | 20      | °C/W |
| Maximum junction-to-case (drain)         | $R_{thJC}$ | 0.8     | 1       |      |
| Maximum junction-to-case (source)        | $R_{thJC}$ | 1.1     | 1.4     |      |

#### Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8DC is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 54 °C/W
- $T_C = 25$  °C



| SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted) |                         |  |      |         |         |                      |
|---|-------------------------|--|------|---------|---------|----------------------|
| PARAMETER   | SYMBOL                  | TEST CONDITIONS  | MIN. | TYP.    | MAX.    | UNIT                 |
| <b>Static</b>   |                         |  |      |         |         |                      |
| Drain-source breakdown voltage  | $V_{DS}$                | $V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$   | 25   | -       | -       | V                    |
| $V_{DS}$ temperature coefficient  | $\Delta V_{DS}/T_J$     | $I_D = 10\text{ mA}$   | -    | 21      | -       | mV/ $^\circ\text{C}$ |
| $V_{GS(th)}$ temperature coefficient  | $\Delta V_{GS(th)}/T_J$ | $I_D = 250\text{ }\mu\text{A}$   | -    | -4.8    | -       |                      |
| Gate-source threshold voltage   | $V_{GS(th)}$            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$   | 1    | -       | 2.1     | V                    |
| Gate-source leakage   | $I_{GSS}$               | $V_{DS} = 0\text{ V}$ , $V_{GS} = +16 / -12\text{ V}$  | -    | -       | 100     | nA                   |
| Zero gate voltage drain current   | $I_{DSS}$               | $V_{DS} = 25\text{ V}$ , $V_{GS} = 0\text{ V}$   | -    | -       | 1       | $\mu\text{A}$        |
|   |                         | $V_{DS} = 25\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 70\text{ }^\circ\text{C}$  | -    | -       | 15      |                      |
| On-state drain current <sup>a</sup>   | $I_{D(on)}$             | $V_{DS} \geq 10\text{ V}$ , $V_{GS} = 10\text{ V}$   | 40   | -       | -       | A                    |
| Drain-source on-state resistance <sup>a</sup>                               | $R_{DS(on)}$            | $V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$   | -    | 0.00048 | 0.00058 | $\Omega$             |
|   |                         | $V_{GS} = 4.5\text{ V}$ , $I_D = 20\text{ A}$  | -    | 0.00065 | 0.00082 |                      |
| Forward transconductance <sup>a</sup>                                       | $g_{fs}$                | $V_{DS} = 15\text{ V}$ , $I_D = 20\text{ A}$   | -    | 110     | -       | S                    |
| <b>Dynamic <sup>b</sup></b>   |                         |  |      |         |         |                      |
| Input capacitance   | $C_{ISS}$               | $V_{DS} = 10\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$  | -    | 10 850  | -       | pF                   |
| Output capacitance  | $C_{OSS}$               |  | -    | 3360    | -       |                      |
| Reverse transfer capacitance  | $C_{RSS}$               |  | -    | 720     | -       |                      |
| Total gate charge   | $Q_g$                   | $V_{DS} = 10\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$  | -    | 134     | 200     | nC                   |
|   |                         | $V_{DS} = 10\text{ V}$ , $V_{GS} = 4.5\text{ V}$ , $I_D = 20\text{ A}$   | -    | 61      | 92      |                      |
| Gate-source charge  | $Q_{gs}$                |  | -    | 24      | -       |                      |
| Gate-drain charge   | $Q_{gd}$                |  | -    | 9.2     | -       |                      |
| Gate resistance   | $R_g$                   | $f = 1\text{ MHz}$   | 0.1  | 0.38    | 0.75    | $\Omega$             |
| Turn-on delay time  | $t_{d(on)}$             | $V_{DD} = 10\text{ V}$ , $R_L = 0.5\text{ }\Omega$ , $I_D \cong 20\text{ A}$ ,<br>$V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$  | -    | 19      | 38      | ns                   |
| Rise time   | $t_r$                   |  | -    | 24      | 48      |                      |
| Turn-off delay time   | $t_{d(off)}$            |  | -    | 53      | 105     |                      |
| Fall time   | $t_f$                   |  | -    | 9       | 18      |                      |
| Turn-on delay time  | $t_{d(on)}$             | $V_{DD} = 10\text{ V}$ , $R_L = 0.5\text{ }\Omega$ , $I_D \cong 20\text{ A}$ ,<br>$V_{GEN} = 4.5\text{ V}$ , $R_g = 1\text{ }\Omega$ | -    | 51      | 100     |                      |
| Rise time   | $t_r$                   |  | -    | 95      | 190     |                      |
| Turn-off delay time   | $t_{d(off)}$            |  | -    | 47      | 94      |                      |
| Fall time   | $t_f$                   |  | -    | 16      | 32      |                      |
| <b>Drain-Source Body Diode Characteristics</b>                              |                         |  |      |         |         |                      |
| Continuous source-drain diode current                                       | $I_S$                   | $T_C = 25\text{ }^\circ\text{C}$   | -    | -       | 94.5    | A                    |
| Pulse diode forward current   | $I_{SM}$                |  | -    | -       | 300     |                      |
| Body diode voltage  | $V_{SD}$                | $I_S = 5\text{ A}$ , $V_{GS} = 0\text{ V}$   | -    | 0.71    | 1.1     | V                    |
| Body diode reverse recovery time  | $t_{rr}$                | $I_F = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$  | -    | 63      | 126     | ns                   |
| Body diode reverse recovery charge  | $Q_{rr}$                |  | -    | 87      | 174     | nC                   |
| Reverse recovery fall time  | $t_a$                   |  | -    | 27      | -       | ns                   |
| Reverse recovery rise time  | $t_b$                   |  | -    | 36      | -       |                      |

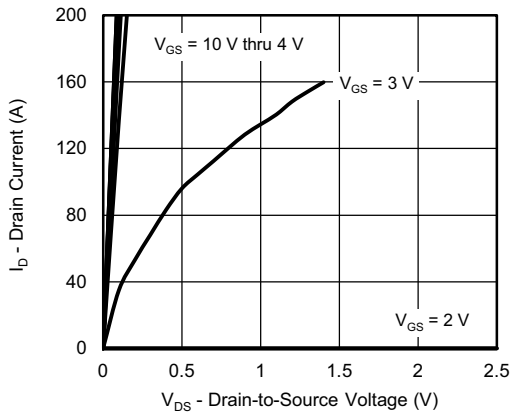
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

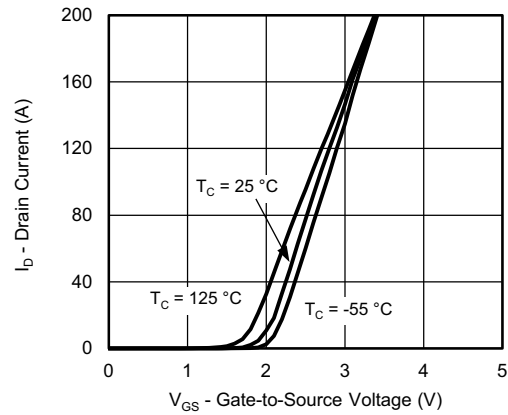
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



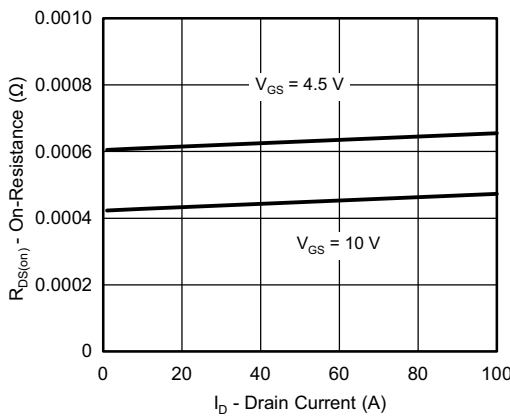
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



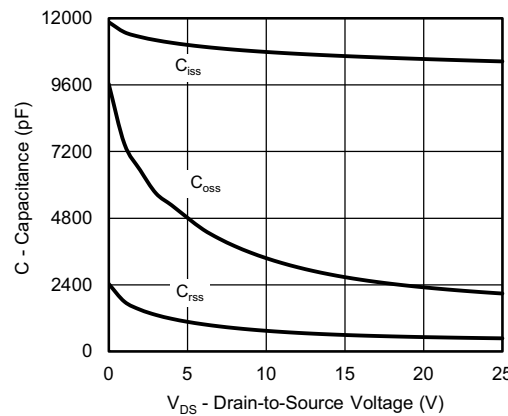
Output Characteristics



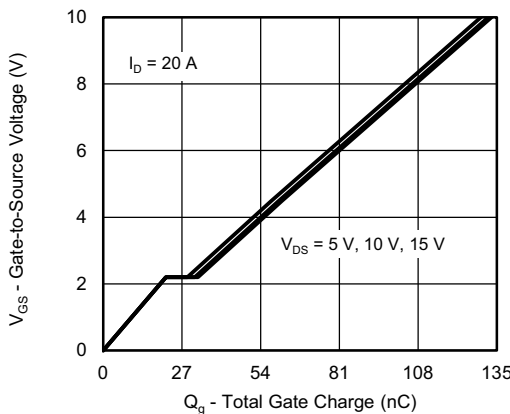
Transfer Characteristics



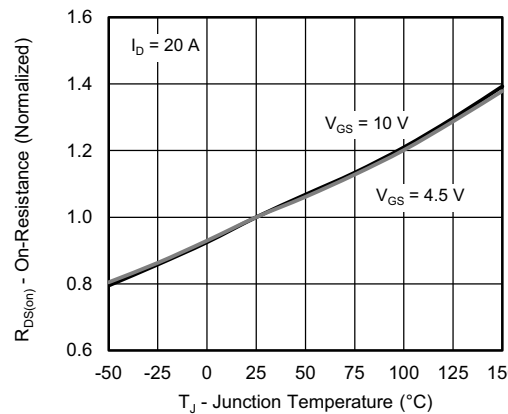
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



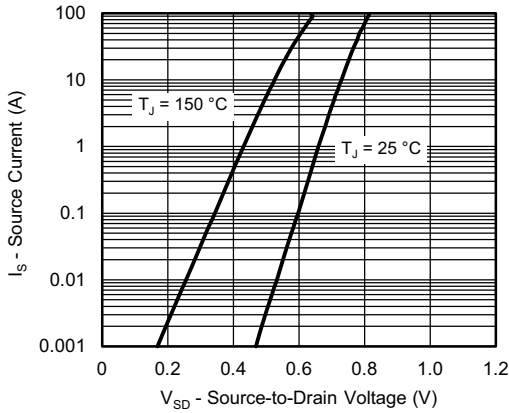
Gate Charge



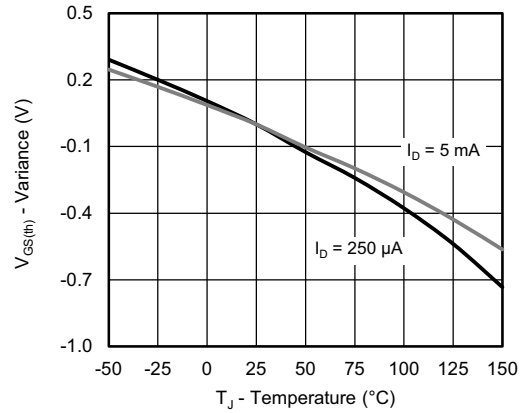
On-Resistance vs. Junction Temperature



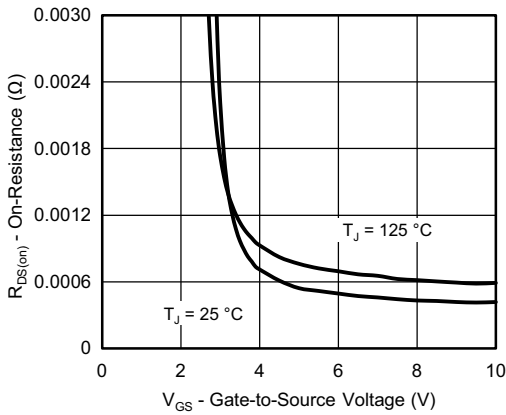
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



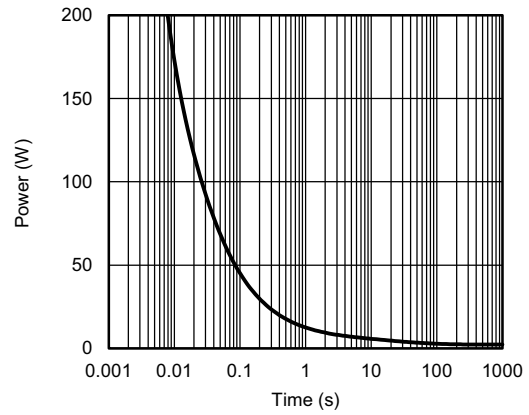
Source-Drain Diode Forward Voltage



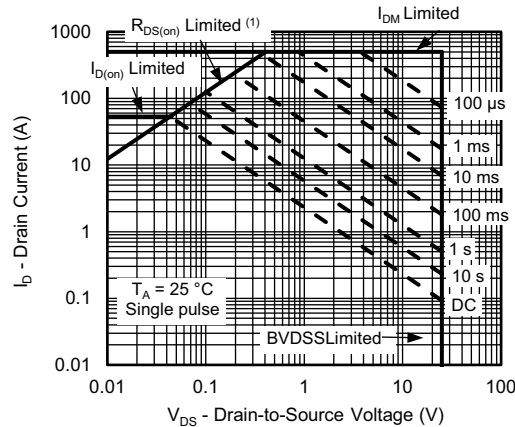
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient

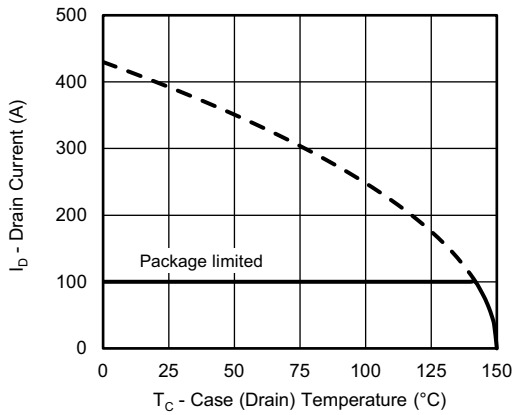


(1)  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

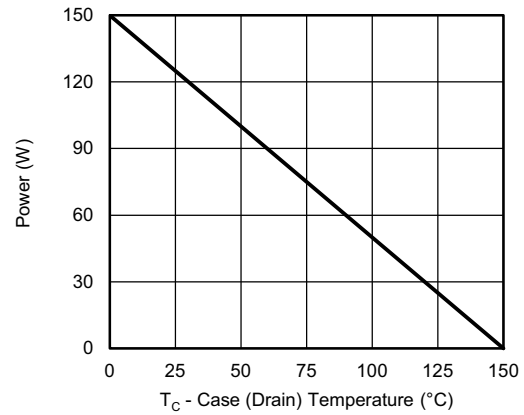
Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



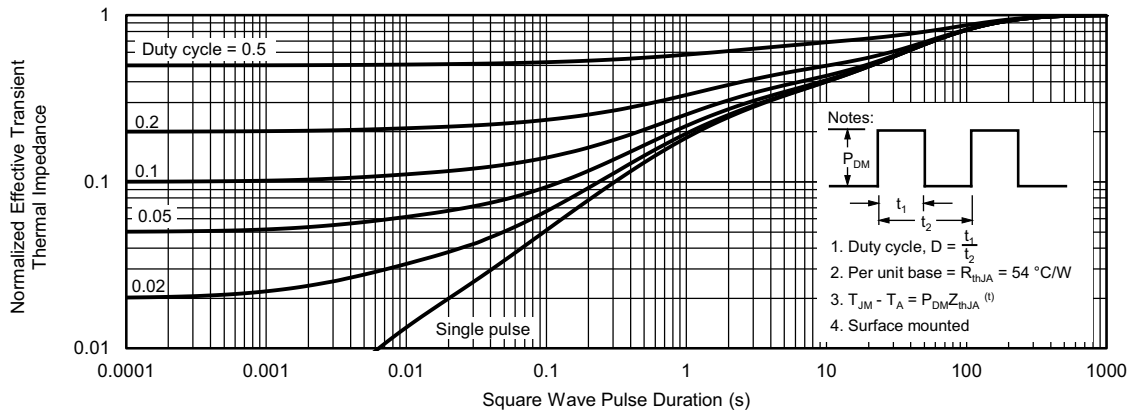
Current Derating <sup>a</sup>



Power, Junction-to-Case

Note

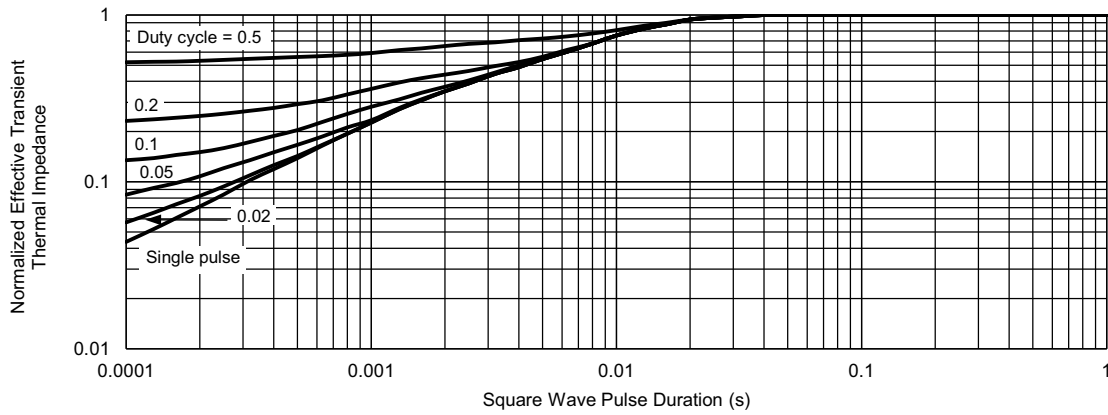
a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



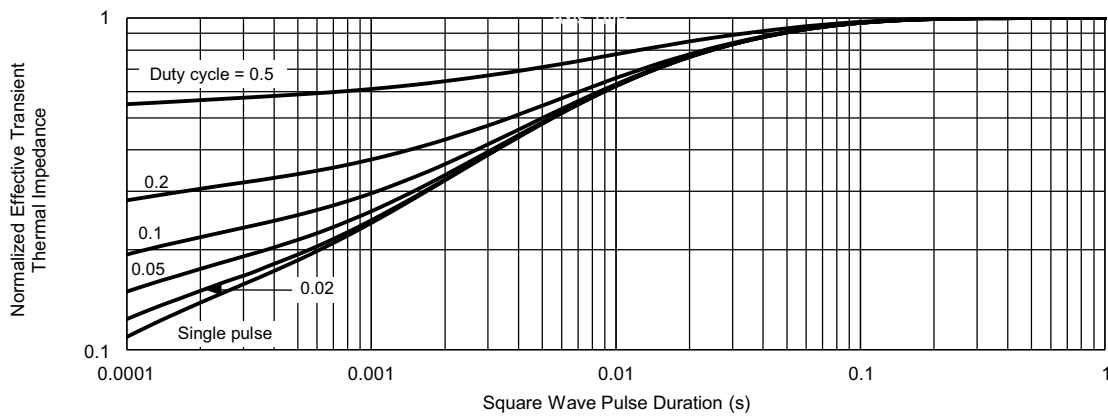
Normalized Thermal Transient Impedance, Junction-to-Ambient



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Case (Drain)**



**Normalized Thermal Transient Impedance, Junction-to-Case (Source)**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?75639](http://www.vishay.com/ppg?75639).



# PowerPAK<sup>®</sup> SO-8 Double Cooling Case Outline



| DIM. | MILLIMETERS |      |      | INCHES     |       |       |
|------|-------------|------|------|------------|-------|-------|
|      | MIN.        | NOM. | MAX. | MIN.       | NOM.  | MAX.  |
| A    | 0.51        | 0.56 | 0.61 | 0.020      | 0.022 | 0.024 |
| A1   | 0.00        | 0.02 | 0.05 | 0.000      | 0.001 | 0.002 |
| b    | 0.36        | 0.41 | 0.46 | 0.014      | 0.016 | 0.018 |
| c    | 0.15        | 0.20 | 0.25 | 0.006      | 0.008 | 0.010 |
| D    | 4.90        | 5.00 | 5.10 | 0.193      | 0.197 | 0.201 |
| D1   | 3.71        | 3.76 | 3.81 | 0.146      | 0.148 | 0.150 |
| e    | 1.27 BSC    |      |      | 0.050 BSC  |       |       |
| E    | 5.90        | 6.00 | 6.10 | 0.232      | 0.236 | 0.240 |
| E1   | 3.60        | 3.65 | 3.70 | 0.142      | 0.144 | 0.146 |
| E2   | 0.46 typ.   |      |      | 0.018 typ. |       |       |
| H    | 0.49        | 0.54 | 0.59 | 0.019      | 0.021 | 0.023 |
| K    | 1.22        | 1.27 | 1.32 | 0.048      | 0.050 | 0.052 |
| K1   | 0.64 typ.   |      |      | 0.025 typ. |       |       |
| L    | 0.49        | 0.54 | 0.59 | 0.019      | 0.021 | 0.023 |
| M1   | 3.85        | 3.90 | 3.95 | 0.152      | 0.154 | 0.156 |
| M2   | 2.74        | 2.79 | 2.84 | 0.108      | 0.110 | 0.112 |
| M3   | 1.06        | 1.11 | 1.16 | 0.042      | 0.044 | 0.046 |
| M4   | 0.56 typ.   |      |      | 0.022 typ. |       |       |
| N    | 8           |      |      | 8          |       |       |
| T1   | 4.51        | 4.56 | 4.61 | 0.178      | 0.180 | 0.182 |
| T2   | 2.58        | 2.63 | 2.68 | 0.102      | 0.104 | 0.106 |
| T3   | 1.88        | 1.93 | 1.98 | 0.074      | 0.076 | 0.078 |
| T4   | 0.97 typ.   |      |      | 0.038 typ. |       |       |
| T5   | 0.48 typ.   |      |      | 0.019 typ. |       |       |

ECN: T21-0014-Rev. B, 08-Feb-2021  
DWG: 6048

## RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)





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