ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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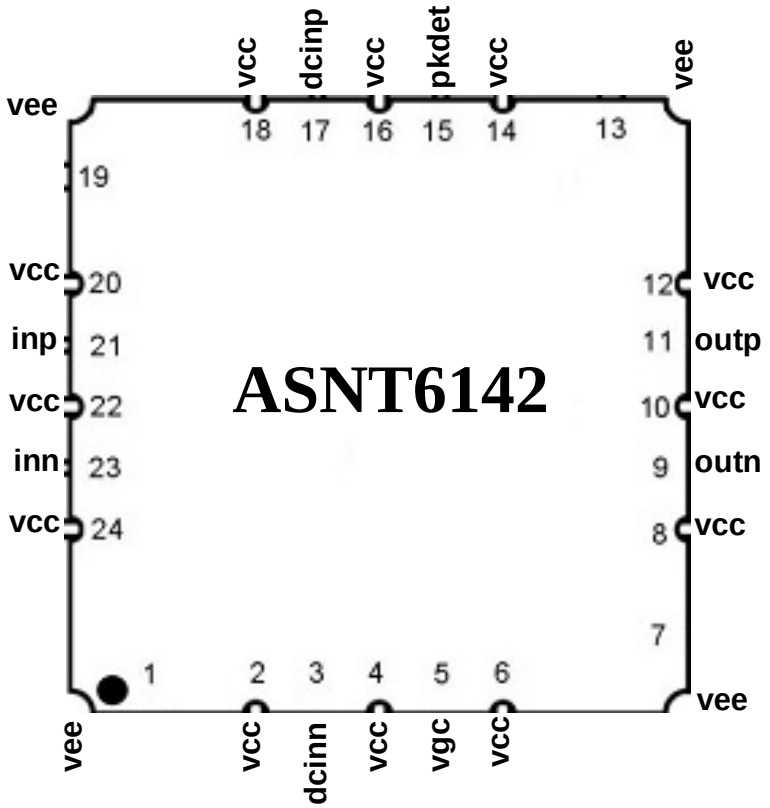
ASNT6142-KHC
DC-20*GHz* Linear amplifier

- Broadband (DC-20*GHz*) linear amplifier for receiver-side applications
- Features gain control, input offset adjustment, and input peak detector
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Fully differential input interface with on-chip 50*Ohm* termination
- Fully differential output interface with on-chip 50*Ohm* termination
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 695*mW*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFN 24-pin package



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DESCRIPTION

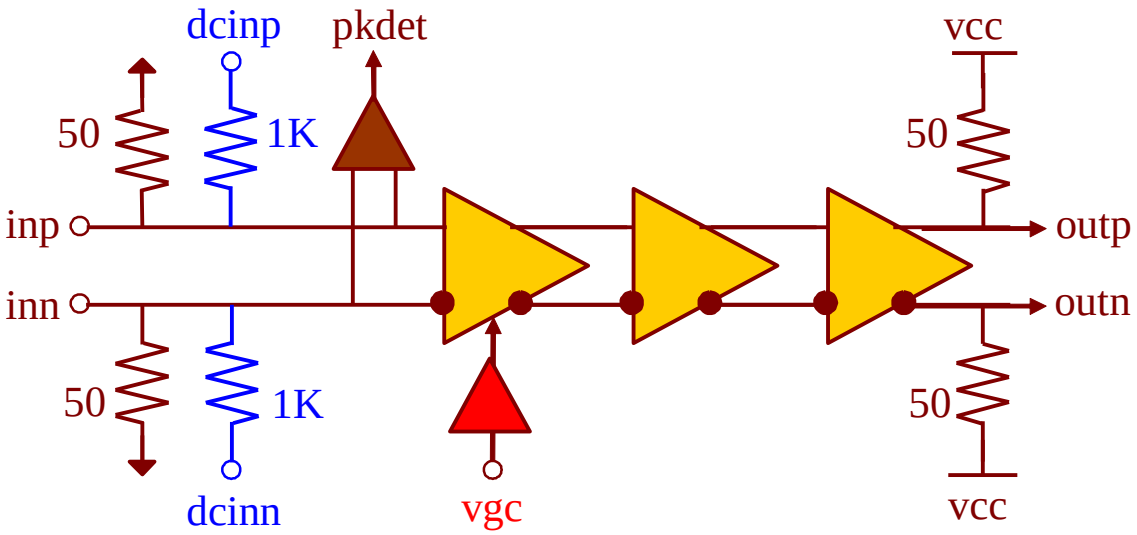

Fig. 1. Functional Block Diagram

The temperature-stable linear amplifier ASNT6142-KHC, which is fabricated in an advanced SiGe technology, provides low-jitter broadband variable signal amplification between its input inp/inn and output outp/outn signal ports and is intended for use in high-speed communication systems. Gain adjustment is performed through the external control port vgc. A graph of the amplifier's single-ended gain vs. vgc (where vcc=0*V* and x-axis values are settings below vcc) is shown below. Differential gain is found by adding 6*dB* to these y-axis numbers.

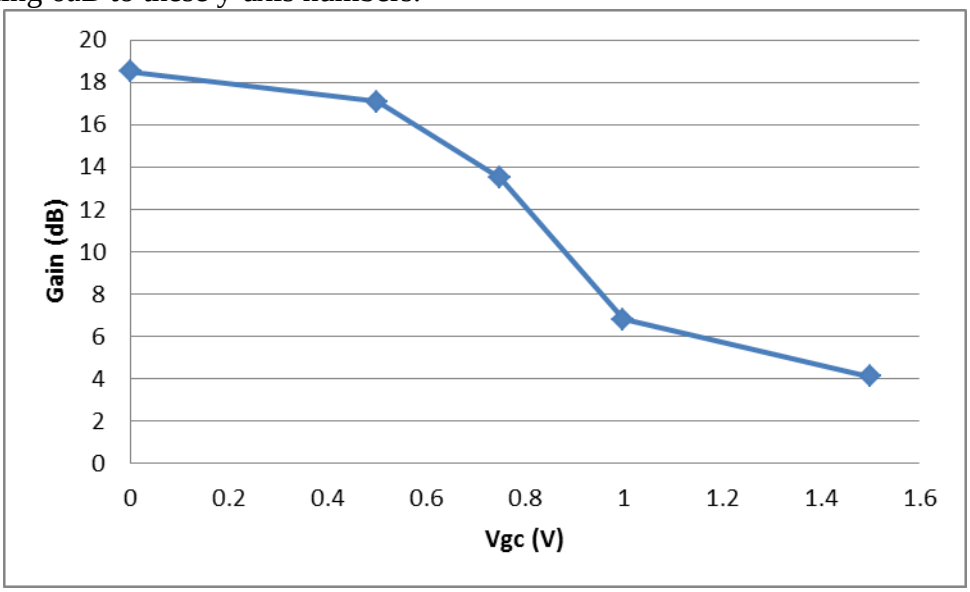

Fig. 2. Single-ended Gain vs. Vgc

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The part's I/Os support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

The on-chip peak detector delivers a single-ended output voltage pkdet proportional to the input signal's amplitude. Additional control ports dcinp and dcinn can be used for input signal common-mode voltage adjustment.

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V*=ground and vee = -3.3*V*), or a positive supply (vcc = +3.3*V* and vee = 0.0*V*=ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Main Supply Voltage (vcc-vee)		3.6	*V*
Power Consumption		0.80	*W*
RF Input Voltage Swing (SE)		1.0	*V*
CM control Voltage (dcinp/n-vcc)	-2.2	+0.8	*V*
Gain Control Voltage (vgc1-vcc)	-2.0	+0.4	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
inp	21	CML input	Differential high-speed data inputs with internal SE 50*Ohm* termination to vcc
inn	23		
outp	11	CML output	Differential high-speed data outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
outn	9		
Low-Speed I/Os			
dcinp	17	Analog Input	inp common mode control voltage
dcinn	3		inn common mode control voltage
vgc	5	Input	Low-speed amplitude adjustment tuning input
pkdet	15	Output	Analog voltage generated by the peak detector

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V* or 0*V*)	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0*V* or -3.3*V*)	1, 7, 13, 19

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		210		*mA*	
Power consumption		695		*mW*	
Junction temperature	-25	50	85	*°C*	
HS Input Data (inp/inn)					
Bandwidth		20		*GHz*	-3*dB*
CM level	-0.8		0	*V*	
Input noise density		1.5		*nV*/sqrt*(Hz)*	High Gain
S11		-10		*dB*	DC to 20*GHz*
HS Output Data (outp/outn)					
CM level		-0.6		*V*	
S22		-8		*dB*	DC to 20*GHz*
Differential gain			25	*dB*	At 10*GHz*, vgc= vcc
Differential gain	10			*dB*	At 10*GHz*, vgc= vcc -1.5*V*
Output referred 1dB compression point		2.7		*dBm*	Single-Ended, 20*GHz*
THD		0.2		*%*	At 350*mV*p-p output swing, SE
Low-Speed Control Input (vgc)					
Voltage range	vcc-2.0		vcc	*V*	
Input Impedance		2		*KOhm*	
DC Offset Control Inputs (dcinp/dcinn)					
Voltage range	vcc-2.0		vcc	*V*	
Input Impedance		1		*KOhm*	

PACKAGE INFORMATION

The chip die is housed in a custom, 24-pin CQFN package shown in Fig. 3. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT6142-KHC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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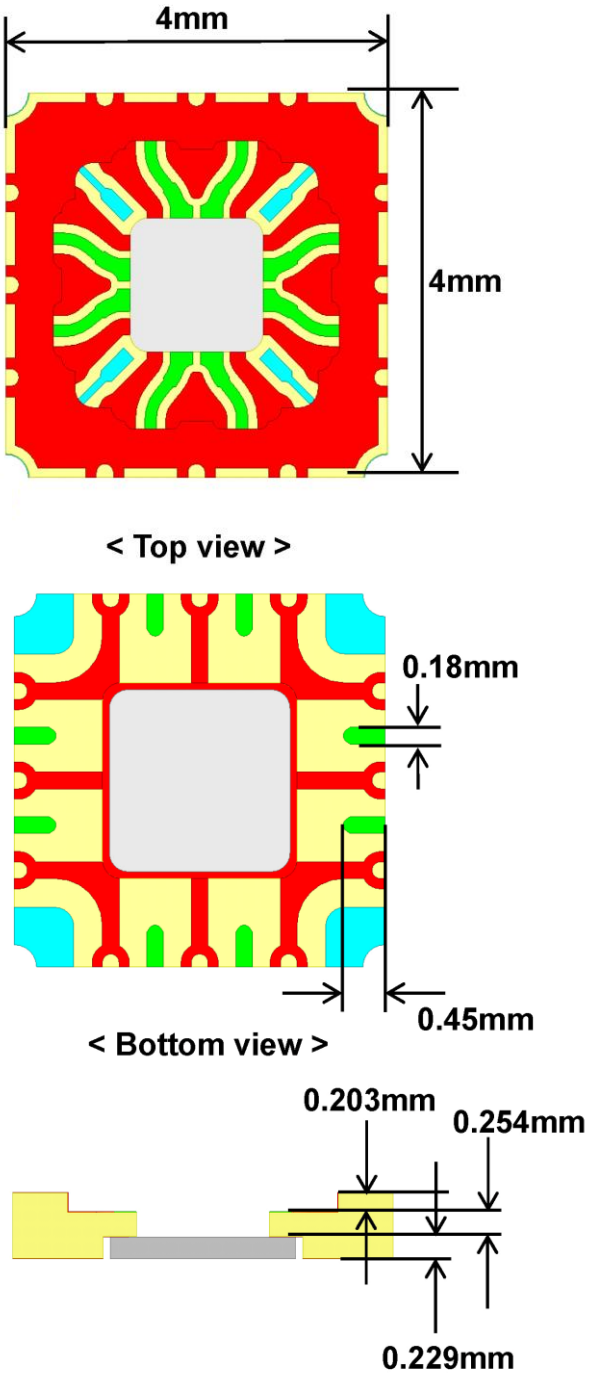

Fig. 3. CQFN 24-Pin Package Drawing (All Dimensions in mm)

REVISION HISTORY

Revision	Date	Changes
1.1.2	05-2020	Updated Package Information
1.0.2	01-2020	First release