iMX6 SoloX COM Board Datasheet

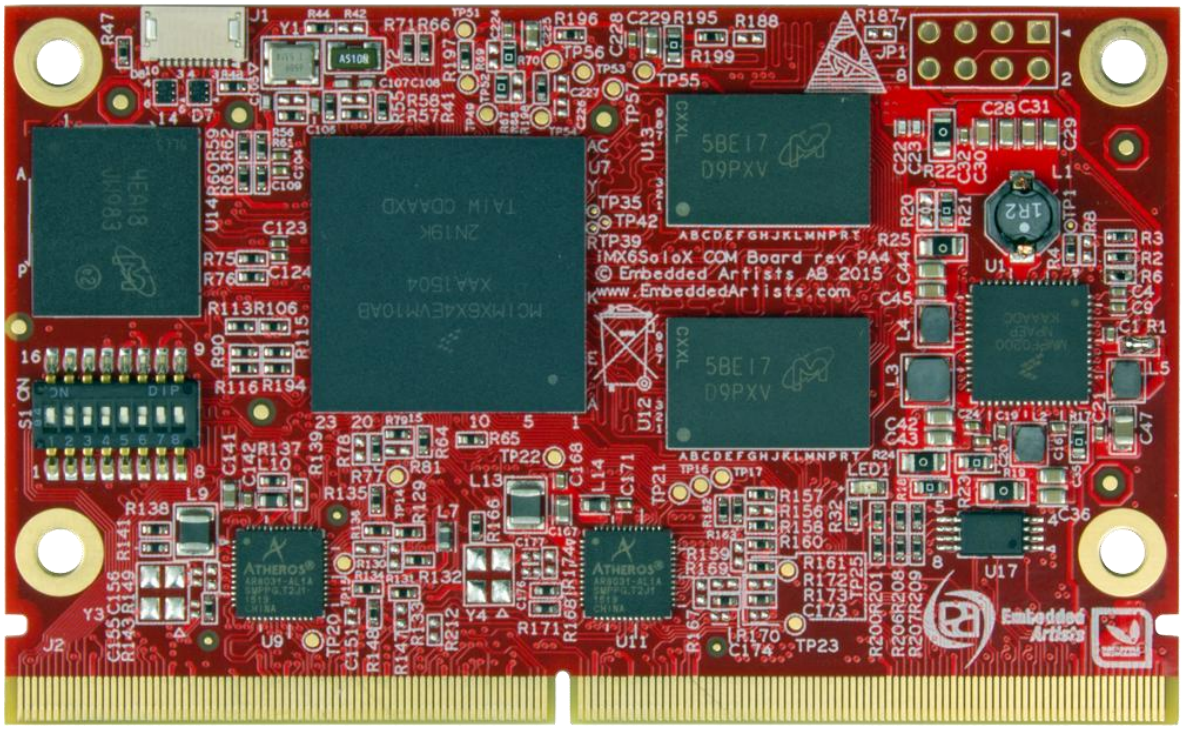

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Table of Contents

1 Document Revision History 5

2 Introduction 6

2.1 Hardware 6

2.2 Software 7

2.3 Features and Functionality 7

2.4 Interface Overview 9

2.5 Reference Documents 10

3 EACOM Board Pinning 12

3.1 Pin Numbering 12

3.2 Pin Assignment 13

4 Pin Mapping 23

4.1 Functional Multiplexing on I/O Pins 23

4.1.1 Alternative I/O Function List 23

4.2 I/O Pin Control 23

5 Interface Description 24

5.1 Analogue Inputs 24

5.2 Analogue Video Interface 24

5.3 CAN 25

5.4 Display Interfaces 25

5.4.1 Parallel RGB LCD Interface 26

5.4.2 LVDS Interface 28

5.5 Digital Audio Interfaces: Synchronous Serial Interface and AUDMUX 29

5.6 Digital Audio Interfaces: ESAI 33

5.7 Digital Audio Interfaces: S/PDIF 34

5.8 Digital Audio Interfaces: MQS 34

5.9 Ethernet 35

5.10 GPIOs 36

5.11 I2C 36

5.12 JTAG 38

5.13 Matrix Keypad 39

5.14 PCI Express 40

5.15 Parallel Camera Interface 40

5.16 Power Management 43

5.17 Power Supply Signals 43

5.18 PWM 44

5.19 SD/MMC 44

5.20 SPI 47

5.21 UART 48

5.22 USB 50

6 Boot Options 52

6.1 iMX6 SoloX COM Board, rev A, Boot Control Differences 53

7 Technical Specification 55

7.1 Absolute Maximum Ratings 55

7.2 Recommended Operating Conditions 55

7.3 Power Ramp-Up Time Requirements 55

7.4 Electrical Characteristics 55

7.4.1 Reset Output Voltage Range 55

7.4.2 Reset Input 56

7.4.3 ADC_VREFH 56

7.5 Power Consumption 56

7.6 Mechanical Dimensions 56

7.6.1 MXM3 Socket 58

7.6.2 Module Assembly Hardware 58

7.7 Environmental Specification 58

7.7.1 Operating Temperature 58

7.7.2 Relative Humidity (RH) 59

7.8 Thermal Design Considerations 59

7.8.1 Thermal Management 59

7.8.2 Thermal Parameters 59

7.9 Product Compliance 60

8 Functional Verification and RMA 61

9 Things to Note 62

9.1 Shared Pins and Multiplexing 62

9.2 Only Use EA Board Support Package (BSP) 62

9.3 OTP Fuse Programming 62

9.4 Write Protect on Parameter Storage E2PROM 62

9.5 Integration - Contact Embedded Artists 62

9.6 ESD Precaution when Handling iMX6 SoloX COM Board 64

9.7 EMC / ESD 64

10 Custom Design 65

11 Disclaimers 66

11.1 Definition of Document Status 67

1 Document Revision History

Revision	*Date*	*Description*
PA1	2015-10-01	First version.
A	2016-07-18	Updated to alphanumerical numbering of EACOM UART, SPI and I2C channels. Removed slide switches on rev A boards.
PB1	2017-07-31	Added information about boot pins.
PB2	2018-03-16	Changed QPSI memory size to 16 MByte (according to PCN008) and added current consumption information. Corrected PWM4_OUT pinning in table on page 44 (section 5.18 PWM).

2 Introduction

This document is a datasheet that specifies and describes the *iMX6 SoloX COM Board* mainly from a hardware point of view. Some basic software related issues are also addressed, like booting and functional verification, but there are separate software development manuals that should also be consulted.

2.1 Hardware

The *iMX6 SoloX COM Board* is a Computer-on-Module (COM) based on NXP's dual-core ARM Cortex-A9 / M4 i.MX 6SoloX System-on-Chip (SoC) application processor. The board provides a quick and easy solution for implementing a high-performance ARM dual-core Cortex-A9 / M4 based design. The Cortex-A9 runs at up to 1 GHz/800 MHz and the Cortex-M4 core at up to 227 MHz.

The dual-core architecture enables the system to run an OS like Linux on the Cortex-A9 and a Real-Time OS (RTOS) on the Cortex-M4. This architecture is ideal for real time applications where Linux cannot be used for all time critical task. The Cortex-M4 can handle (real time) critical tasks and can also be used to lower the power consumption.

The *iMX6 SoloX COM Board* delivers high computational and graphical performance at very low power consumption. The on-board PMIC, supporting DVFS (Dynamic Voltage and Frequency Scaling), together with a DDR3L memory sub-system reduce the power consumption to a minimum.

The SoC is part of the scalable i.MX6 product family. There is a range of iMX6 COM Boards from Embedded Artists with single, dual and quad Cortex-A9 cores. All boards share the same basic pinning (EACOM specification) for maximum flexibility and performance scalability.

The *iMX6 SoloX COM Board* has a very small form factor and shields the user from a lot of complexity of designing a high performance system. It is a robust and proven design that allows the user to focus the product development, shorten time to market and minimize the development risk.

The *iMX6 SoloX COM Board* targets a wide range of applications, such as:

- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- HMI/GUI solutions
- Smart Toll Systems
- Connected vending machines
- Digital signage
- Point-of-Sale (POS) applications
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- Portable systems
- ...and much more

The picture below illustrates the block diagram of the iMX6 SoloX COM Board.

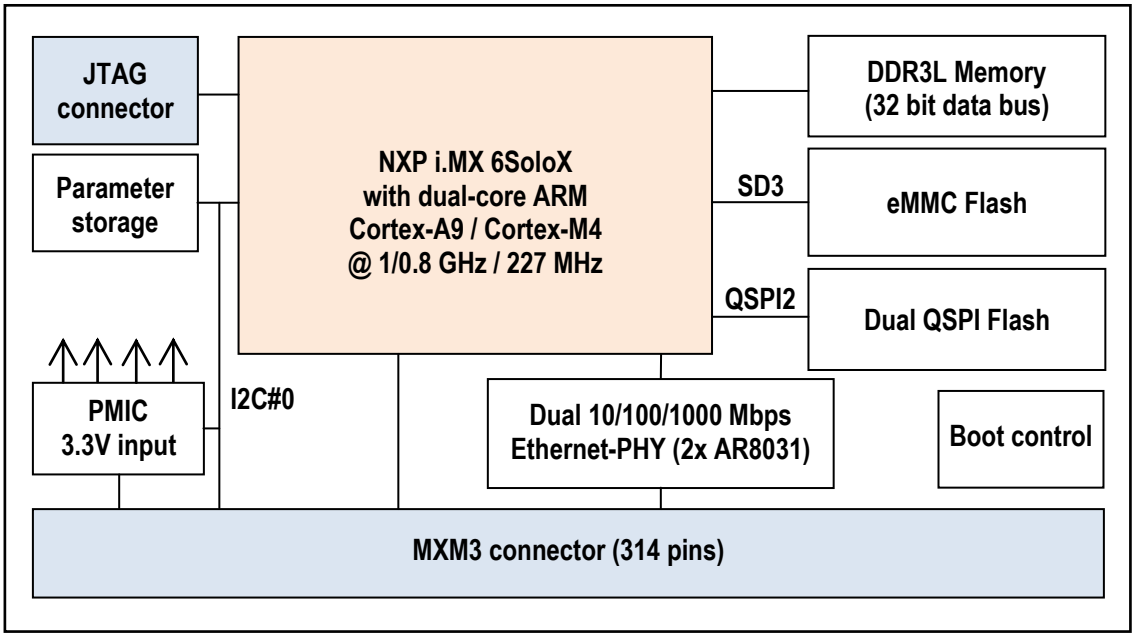


Figure 1 – iMX6 SoloX COM Board Block Diagram

The *iMX6 SoloX COM Board* pin assignment focus on direct connection to (carrier board) interface connectors and minimize trace and layer crossing. This is important for high speed, serial interfaces with impedance controlled differential pairs. As a result, carrier boards can be designed with few routing layers. In many cases, a four layer pcb is enough to implement advanced and compact carrier boards. The pin assignment is common for the *iMX6 COM Boards* from Embedded Artists and the general, so called, EACOM specification is found in separate document.

2.2 Software

The iMX6 SoloX COM Board has Board Support Packages (BSPs) for Embedded Linux. Precompiled images are available. Embedded Artists works with partners that can provide support for other operating systems (OS). For more information contact Embedded Artists support.

This document has a hardware focus and does not cover software development. See other documents related to the iMX6 SoloX COM Board for more information about software development.

2.3 Features and Functionality

The i.MX 6SoloX is a powerful SoC. The full specification can be found in NXP's *iMX6 SoloX Datasheet* and *iMX6 SoloX Reference Manual*. The table below lists the main features and functions of the iMX6 SoloX COM board - which represents Embedded Artists integration of the iMX6 SoloX SoC. Due to pin configuration some functions and interfaces of the iMX6 SoloX are not available on the iMX6 SoloX COM board.

Group	Feature		iMX6 SoloX COM Board
CPUs	NXP SoC	commercial temperature range industrial temperature range	MCIMX6X4EVM10AB MCIMX6X4CVM08AB
	CPU Cores		1x Cortex-A9 1x Cortex-M4 with MPU/FPU
	L1 Instruction cache		32 KByte on Cortex-A9 16 KByte on Cortex-M4

	L1 Data cache	32 KByte on Cortex-A9 16 KByte on Cortex-M4
	L2 Cache on Cortex-A9	512 KByte
	TCM on Cortex-M4	64 KByte
	NEON SIMD media accelerator on Cortex-A9	✓
	Maximum CPU frequency (comm./ind. temp. range)	996/792 MHz on Cortex-A9 227 MHz on Cortex-M4
Security Functions	ARM TrustZone	✓
	Advanced High Assurance Boot	✓
	Cryptographic Acceleration and Assurance Module	✓
	Secure Non-Volatile Storage, incl. Secure Real-Time Clock	✓
	System JTAG controller	✓
Memory	DDR3L RAM Size	1 GByte
	DDR3L RAM Speed	800 MT/s
	DDR3L RAM Memory Width	32 bit
	eMMC NAND Flash (8 bit)	4 GByte
	QSPI (two 4-bit in parallel)	16 MByte
Graphical Processing	GPU 2D/3D	Vivante GC400T
	Open GL ES 2.0 (17Mtri/s 133Mpxl/s)	✓
	PiXel Processing Pipeline (PXP)	✓
Graphical Output	LVDS, 18/24-bit	✓
	RGB, 24-bit parallel interface	✓
Graphical Input	CMOS sensor interface (camera), digital 20-bit parallel interface	✓
	NTSC/PAL analogue video input interface (4 ch)	✓
Interfaces (all functions are not available at the same time)	Dual 10/100/1000 Mbps Gigabit Ethernet controllers with support for Audio Video Bridging (AVB)	✓ with on-board PHY
	PCIe v2.0 (1 lane)	✓
	Dual 4 ch 12-bit ADC (8 ch in total)	✓
	2x USB 2.0 ports, HS OTG + PHY	✓
	3x SD/MMC 4.5	✓ SD3 interface used on-board
	5x SPI, 6x UART, 4x I²C, 5x I²S/SSI	✓
	Dual FlexCAN, CAN bus 2.0B	✓
Other	PMIC (MMPF0200) supporting DVFS techniques for low power modes	✓

	On-board switches to select eMMC or QSPI boot source, or USB OTG booting	✓
	E2PROM storing board information including Ethernet MAC address and memory bus setup parameters	✓
	i.MX 6SoloX on-chip RTC	✓
	On-board watchdog functionality	✓

2.4 Interface Overview

The table below lists the interfaces that are specified in the EACOM specification (see separate document for details) and what is supported by the iMX6 SoloX COM board.

Interface	EACOM specification	iMX6 SoloX COM Board	Note
UART	3 ports (two 4 wire and one 2 wire)	3 ports	More ports available as alternative pin functions
SPI	2 ports	2 ports	More ports available as alternative pin functions
I2C	3 ports	3 ports	
SD/MMC	2 ports (one 4 databits and one 8 databits)	2 ports	
Parallel LCD	24 databits and CLK/HS/VS/DE	Full support	
LCD support	LCD power ctrl, Backlight power/contrast control, touch panel ctrl (RST and IRQ)	Full support	1 PWM and 4 GPIO
LVDS LCD	2 ports (18/24 bit LVDS data)	1 port	
HDMI (TDMS)		-	
Parallel Camera		1 port	
Serial Camera	CSI, 4 lane	-	
Gigabit Ethernet	2 ports	2 ports	
PCIe	1 post, 1 lane	1 port, 1 lane	
SATA		-	
USB	1 USB3.0 OTG 1 USB3.0 Host 1 USB2.0 Host	1 USB2.0 OTG 1 USB2.0 Host	
SPDIF	1 TX/RX port	1 port	
CAN	2 ports	2 ports	
I2S/SSI/AC97	1 port (4 wire synchronous plus MCLK)	1 port	Shared pins are used. More ports available as alternative pin functions.

Analog audio	Stereo output	-	
GPIO	9 pins	7 pins	More GPIO pins are available as alternative pin functions.
PWM	1 pin	1 pin	More pins are available as alternative pin functions.
ADC	8 inputs	8 inputs	
Type specific	39 pins	4 Video ADC inputs	35 type specific pins not used since all i.MX 6SoloX pins allocated.
Power	10 VIN, VBAT and 47 GND	10 VIN, VBAT and 47 GND	About 15% of the pins are ground pins.

2.5 Reference Documents

The following documents are important reference documents and should be consulted when integrating the iMX6 SoloX COM board:

- EACOM Board Specification
- EACOM Board Integration Manual

The following NXP documents are also important reference documents and should be consulted for functional details:

- IMX6SXCEC, i.MX 6SoloX Applications Processors for Consumer Products - Data Sheet, latest revision
- IMX6SXRM, i.MX 6SoloX Applications Processor Reference Manual, latest revision
- IMX6SXCE, Chip Errata for the i.MX 6SoloX, latest revision
  Note: It is the user's responsibility to make sure all errata published by the manufacturer are taken note of. The manufacturer's advice should be followed.
- AN5050, i.MX 6SoloX Power Consumption Measurement, latest revision
- AN5062, i.MX 6SoloX Product Lifetime Usage Estimates, latest revision

The following documents are external industry standard reference documents and should also be consulted when applicable:

- eMMC (Embedded Multi-Media Card) the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org)
- GbE MDI (Gigabit Ethernet Medium Dependent Interface) defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)
- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com)

- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)
- JTAG (Joint Test Action Group) defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org)
- MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org)
- PCI Express Specifications (www.pci-sig.org)
- SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org)
- SPDIF (aka S/PDIF) (Sony Philips Digital Interface) - IEC 60958-3
- SPI Bus – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)
- USB Specifications (www.usb.org)

3 EACOM Board Pinning

Embedded Artists has defined the EACOM board standard that is based on the SMARC form factor; module size 82 x 50 mm. Note that pinning is different from the SMARC standard. See the *EACOM Board specification* document for details and background information. Hereafter this standard will be referred to as **EACOM**.

The carrier board connector has 314 pins with 0.5 mm pitch and the COM board is inserted in a right angle (R/A) style. The connector is originally defined for use with MXM3 graphics cards. There are multiple sources for carrier board (MXM3) connectors due to the popular standard. The signal integrity is excellent and suitable for data rates up to 5 GHz.

Overall assembly height of the COM board/Carrier board connector can be as low as 6 mm. There are different stack height options available, including 2.7 mm (resulting in overall 6 mm height), 5 mm and 8 mm.

3.1 Pin Numbering

The figures below show the pin numbering for EACOM. Top side edge fingers are numbered P1-P156. Bottom side edge fingers are numbered S1-S158. There is an alternative pin numbering that follows the MXM3 standard with even numbers on the bottom and odd numbers on the top. This numbering is from 1-321, with 7 numbers/pins (150-156) removed due to the keying.

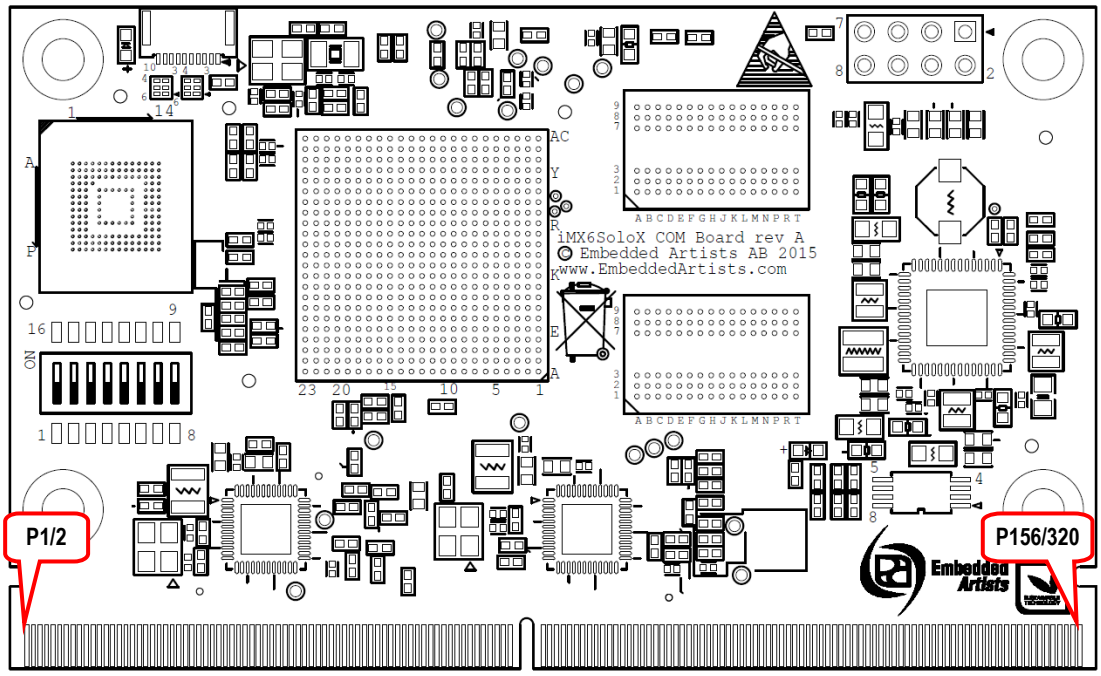


Figure 2 – EACOM Board Pin Numbering, Top Side

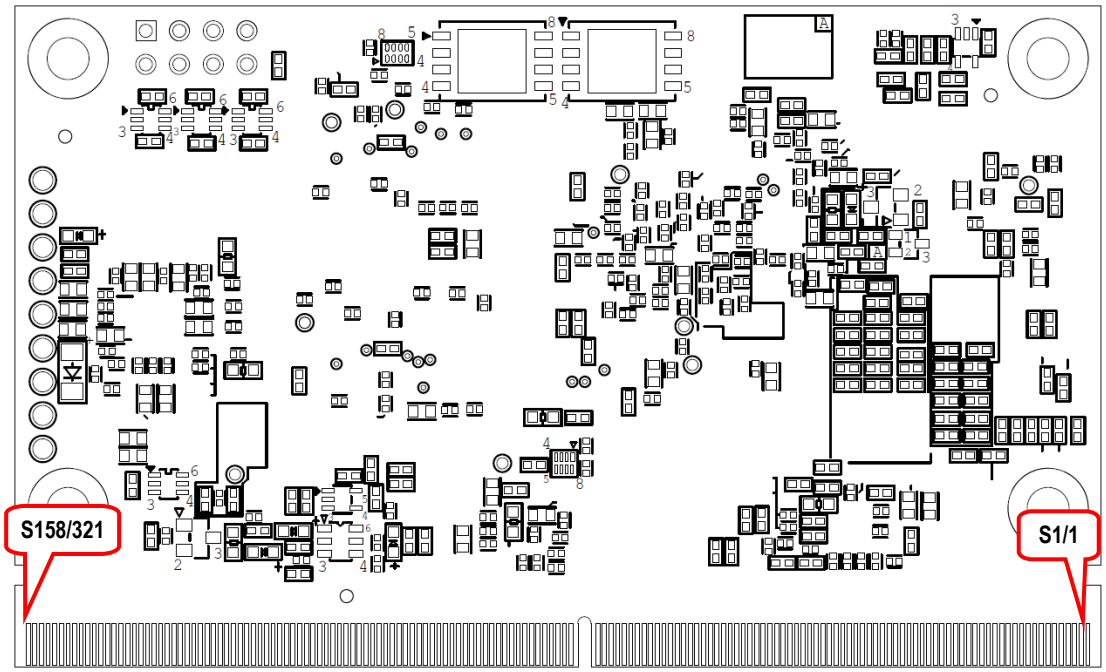


Figure 3 – EACOM Board Pin Numbering, Bottom Side

3.2 Pin Assignment

This section describes the pin assignment of the board, with the following columns:

Pin number	**Px** are top side edge fingers. **Sx** are bottom side edge fingers. An alternative, consecutive, numbering is also shown with odd numbers on the top and even numbers on the bottom side.
EACOM Board	Describe the typical usage of the pin according to EACOM. This pin usage should be followed to get compatibility between different COM boards. If this is not needed, then any of the alternative functions on the pin can also be used.
i.MX 6SoloX Ball Name	The name of the ball of the i.MX 6SoloX SoC (or other component on the COM board) that is connected to this pin.
Notes	When relevant, the preferred pin function is listed.

There are 47 ground pins, which equal to about 15%, and 10 input voltage supply pins.

Note that some pins are COM board *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using these may result in lost compatibility between EACOM boards, but not always. Check details between EACOM boards of interest.

The table below lists the top side pins, P1-P156, odd numbers.

Top Side Pin Number	EACOM Board	i.MX 6SoloX Ball Name	Alternative pin functions?	Notes
P1/2	GPIO6	KEY_ROW2	Yes	GPIO6 controlled by alternative pin function GPIO2_IO17
P2/4	GPIO5	KEY_COL2	Yes	GPIO5 controlled by alternative pin function GPIO2_IO12
P3/6	GPIO4	KEY_ROW1	Yes	GPIO4 controlled by alternative pin function GPIO2_IO16
P4/8	GPIO3	SD4_RESET	Yes	GPIO3 controlled by alternative pin function GPIO6_IO22
P5/10	SD_D1	SD2_DATA1	Yes	

P6/12	SD_D0	SD2_DATA0	Yes	
P7/14	SD_CLK	SD2_CLK	Yes	
P8/16	SD_CMD	SD2_CMD	Yes	
P9/18	SD_D3	SD2_DATA3	Yes	
P10/20	SD_D2	SD2_DATA2	Yes	
P11/22	SD_VCC			Supply voltage for SD interface (3.1-3.3V). Should only supply the SD interface.
P12/24	MMC_D1	SD4_DATA1	Yes	
P13/26	MMC_D0	SD4_DATA0	Yes	
P14/28	MMC_D7	SD4_DATA7	Yes	
P15/30	MMC_D6	SD4_DATA6	Yes	
P16/32	MMC_CLK	SD4_CLK	Yes	
P17/34	MMC_D5	SD4_DATA5	Yes	
P18/36	MMC_CMD	SD4_CMD	Yes	
P19/38	MMC_D4	SD4_DATA4	Yes	
P20/40	MMC_D3	SD4_DATA3	Yes	
P21/42	MMC_D2	SD4_DATA2	Yes	
P22/44	GND			
P23/46	HDMI_TXC_N			HDMI interface not assigned on this COM board.
P24/48	HDMI_TXC_P			HDMI interface not assigned on this COM board.
P25/50	GND			
P26/52	HDMI_TXD0_N			HDMI interface not assigned on this COM board.
P27/54	HDMI_TXD0_P			HDMI interface not assigned on this COM board.
P28/56	HDMI_HPD			HDMI interface not assigned on this COM board.
P29/58	HDMI_TXD1_N			HDMI interface not assigned on this COM board.
P30/60	HDMI_TXD1_P			HDMI interface not assigned on this COM board.
P31/62	GND			
P32/64	HDMI_TXD2_N			HDMI interface not assigned on this COM board.
P33/66	HDMI_TXD2_P			HDMI interface not assigned on this COM board.
P34/68	HDMI_CEC			HDMI interface not assigned on this COM board.
P35/70	GND			
P36/72	ETH1_MD1_P			Connects to Ethernet-PHY AR8031 #1, pin 14
P37/74	ETH1_MD1_N			Connects to Ethernet-PHY AR8031 #1, pin 15
P38/76	GND			
P39/78	ETH1_MD0_P			Connects to Ethernet-PHY AR8031 #1, pin 11
P40/80	ETH1_MD0_N			Connects to Ethernet-PHY AR8031 #1, pin 12
P41/82	ETH1_LINK1000			Connects to Ethernet-PHY AR8031 #1, pin 24
P42/84	ETH1_ACT			Connects to Ethernet-PHY AR8031 #1, pin 23
P43/86	ETH1_LINK			Connects to Ethernet-PHY AR8031 #1, pin 26
P44/88	ETH1_MD3_N			Connects to Ethernet-PHY AR8031 #1, pin 21
P45/90	ETH1_MD3_P			Connects to Ethernet-PHY AR8031 #1, pin 20
P46/92	GND			

P47/94	ETH1_MD2_N			Connects to Ethernet-PHY AR8031 #1, pin 18
P48/96	ETH1_MD2_P			Connects to Ethernet-PHY AR8031 #1, pin 17
P49/98	GND			
P50/100	ETH2_MD1_P			Connects to Ethernet-PHY AR8031 #2, pin 14
P51/102	ETH2_MD1_N			Connects to Ethernet-PHY AR8031 #2, pin 15
P52/104	GND			
P53/106	ETH2_MD0_P			Connects to Ethernet-PHY AR8031 #2, pin 11
P54/108	ETH2_MD0_N			Connects to Ethernet-PHY AR8031 #2, pin 12
P55/110	ETH2_LINK1000			Connects to Ethernet-PHY AR8031 #1, pin 24
P56/112	ETH2_ACT			Connects to Ethernet-PHY AR8031 #2, pin 23
P57/114	ETH2_LINK			Connects to Ethernet-PHY AR8031 #2, pin 26
P58/116	ETH2_MD3_N			Connects to Ethernet-PHY AR8031 #2, pin 21
P59/118	ETH2_MD3_P			Connects to Ethernet-PHY AR8031 #2, pin 20
P60/120	GND			
P61/122	ETH2_MD2_N			Connects to Ethernet-PHY AR8031 #2, pin 18
P62/124	ETH2_MD2_P			Connects to Ethernet-PHY AR8031 #2, pin 17
P63/126	GND			
P64/128	USB_O1_DN	USB_OTG1_DN	No	
P65/130	USB_O1_DP	USB_OTG1_DP	No	
P66/132	USB_O1_OTG_ID	GPIO1_IO10	Yes	Controlled by alternative pin function USB_OTG1_ID
P67/134	USB_O1_SSTXN			USB OTG port #1 on iMX6SoloX does not support USB 3.0 so this pin is unconnected.
P68/136	USB_O1_SSTXP			USB OTG port #1 on iMX6SoloX does not support USB 3.0 so this pin is unconnected.
P69/138	GND			
P70/140	USB_O1_SSRXN			USB OTG port #1 on iMX6SoloX does not support USB 3.0 so this pin is unconnected.
P71/142	USB_O1_SSRXP			USB OTG port #1 on iMX6SoloX does not support USB 3.0 so this pin is unconnected.
P72/144	USB_O1_VBUS	USB_OTG1_VBUS	No	
P73/146	USB_O1_PWR_EN	QSPI1A_DATA2	Yes	Controlled by alternative pin function USB_OTG1_PWR
P74/148	USB_O1_OC	GPIO1_IO08	Yes	Controlled by alternative pin function USB_OTG1_OC
150	Non existing pin			
152	Non existing pin			
154	Non existing pin			
156	Non existing pin			
P75/158	USB_H1_PWR_EN	GPIO1_IO12	Yes	Controlled by alternative pin function USB_OTG2_OC
P76/160	USB_H1_OC	GPIO1_IO11	Yes	Controlled by alternative pin function USB_OTG2_PWR
P77/162	GND			
P78/164	USB_H1_DN	USB_HOST_DN	No	
P79/166	USB_H1_DP	USB_HOST_DP	No	
P80/168	USB_H1_SSTXN			USB Host port #1 on iMX6SoloX does not support USB 3.0 so this pin is unconnected.
P81/170	USB_H1_SSTXP			USB Host port #1 on iMX6SoloX does not support USB 3.0 so this pin is unconnected.

P82/172	GND			
P83/174	USB_H1_SSRXN			USB Host port #1 on iMX6SoloX does not support USB 3.0 so this pin is unconnected.
P84/176	USB_H1_SSRXP			USB Host port #1 on iMX6SoloX does not support USB 3.0 so this pin is unconnected.
P85/178	USB_H1_VBUS	USB_HOST_VBUS	No	
P86/180	USB_H2_PWR_EN	SNVS_TAMPER	No	USB Host port #2 on iMX6SoloX does not exist. Non-standard pin allocation. Pin carry signal SNVS_TAMPER, iMX6SoloX ball V14.
P87/182	USB_H2_OC	ONOFF	No	USB Host port #2 on iMX6SoloX does not exist. Non-standard pin allocation. Pin carry signal ONOFF, iMX6SoloX ball W17
P88/184	GND			
P89/186	USB_H2_DN	KEY_COL0	Yes	USB Host port #2 on iMX6SoloX does not exist. Non-standard pin allocation. KEY_COL0 signal, iMX6SoloX ball C23, During boot from eMMC, this pin carry signal SD3_CD_B. The signal has a 10K pulldown resistor to ground. Signal can be used if it does not interfere with booting (not driving the signal high before eMMC boot is complete).
P90/188	USB_H2_DP	CCM_CLK2	No	USB Host port #2 on iMX6SoloX does not exist. Non-standard pin allocation. Pin carry signal CCM_CLK2, iMX6SoloX ball W18
P91/190	GND			
P92/192	COM board specific			
P93/194	COM board specific			
P94/196	COM board specific			
P95/198	COM board specific			
P96/200	COM board specific			
P97/202	COM board specific			
P98/204	COM board specific			
P99/206	COM board specific			
P100/208	COM board specific			
P101/210	COM board specific			
P102/212	COM board specific			
P103/214	COM board specific			
P104/216	COM board specific			
P105/218	COM board specific			
P106/220	COM board specific			
P107/222	COM board specific			
P108/224	COM board specific			
P109/226	COM board specific			
P110/228	COM board specific			
P111/230	COM board specific			
P112/232	COM board specific			
P113/234	COM board specific			

P114/236	COM board specific			
P115/238	COM board specific			
P116/240	COM board specific			
P117/242	COM board specific			
P118/244	GND			
P119/246	SPI-B_SSEL	QSPI1B_SS0_B	Yes	Controlled by alternative pin function ECSPI3_SS0
P120/248	SPI-B_MOSI	QSPI1B_DATA0	Yes	Controlled by alternative pin function ECSPI3_MOSI
P121/250	SPI-B_MISO	QSPI1B_DATA1	Yes	Controlled by alternative pin function ECSPI3_MISO
P122/252	SPI-B_CLK	QSPI1B_SCLK	Yes	Controlled by alternative pin function ECSPI3_SCLK
P123/254	SPI-A_SSEL	QSPI1A_SS0_B	Yes	Controlled by alternative pin function ECSPI1_SS0
P124/256	SPI-A_MOSI	QSPI1A_DATA0	Yes	Controlled by alternative pin function ECSPI1_MOSI
P125/258	SPI-A_MISO	QSPI1A_DATA1	Yes	Controlled by alternative pin function ECSPI1_MISO
P126/260	SPI-A_CLK	QSPI1A_SCLK	Yes	Controlled by alternative pin function ECSPI1_SCLK
P127/262	GND			
P128/264	UART-C_RXD	KEY_ROW3	Yes	Controlled by alternative pin function UART5_RX_DATA
P129/266	UART-C_TXD	KEY_COL3	Yes	Controlled by alternative pin function UART5_TX_DATA
P130/268	UART-B_RXD	SD1_DATA0	Yes	Controlled by alternative pin function UART2_RX_DATA
P131/270	UART-B_CTS	SD1_DATA2	Yes	Controlled by alternative pin function UART2_CTS_B
P132/272	UART-B_RTS	SD1_DATA3	Yes	Controlled by alternative pin function UART2_RTS_B
P133/274	UART-B_TXD	SD1_DATA1	Yes	Controlled by alternative pin function UART2_TX_DATA
P134/276	UART-A_RXD	GPIO1_IO05	Yes	Controlled by alternative pin function UART1_RX_DATA
P135/278	UART-A_CTS	GPIO1_IO07	Yes	Controlled by alternative pin function UART1_CTS_B
P136/280	UART-A_RTS	GPIO1_IO06	Yes	Controlled by alternative pin function UART1_RTS_B
P137/282	UART.A_TXD	GPIO1_IO04	Yes	Controlled by alternative pin function UART1_TX_DATA
P138/284	PWM	USB_H_STROBE	Yes	Controlled by alternative pin function PWM1_OUT. Pin can only be an output since signal pass through a voltage level translator.
P139/286	GPIO2	SD1_CMD	Yes	GPIO2 controlled by alternative pin function GPIO6_IO01
P140/288	GPIO1	SD1_CLK	Yes	GPIO1 controlled by alternative pin function GPIO6_IO00
P141/290	PERI_PWR_EN	GPIO4_IO26	Yes	Enable signal (active high) for carrier board peripheral power supplies. More information about carrier board design can be found in *EA COM Board specification*.
P142/292	RESET_IN			Reset input, active low. Pull signal low to activate reset. No need to pull signal high externally.
P143/294	RESET_OUT			Reset (open drain) output, active low. Driven low during reset. 1.5K pull-up resistor to VIN.
P144/296	GND			
P145/298	VBAT			Supply voltage from coin cell battery for keeping PMIC and RTC functioning during standby.
P146/300	E2PROM_WP			Should be left open (will write protect the on-board parameter storage E2PROM), or connected to GND (will enable writes to the on-board parameter storage E2PROM AND place the i.MX 6SoloX SoC in USB OTG boot mode after a power cycle).
P147/302	VIN			Main input voltage supply (3.3V)
P148/304	VIN			Main input voltage supply (3.3V)
P149/306	VIN			Main input voltage supply (3.3V)

P150/308	VIN	Main input voltage supply (3.3V)
P151/310	VIN	Main input voltage supply (3.3V)
P152/312	VIN	Main input voltage supply (3.3V)
P153/314	VIN	Main input voltage supply (3.3V)
P154/316	VIN	Main input voltage supply (3.3V)
P155/318	VIN	Main input voltage supply (3.3V)
P156/320	VIN	Main input voltage supply (3.3V)

The table below lists the bottom side pins, S1-S158, even numbers.

Bottom Side Pin Number	EACOM Board	i.MX 6SoloX Ball Name	Alternative pin functions?	Notes
S1/1	MQS_RIGHT	CSI_VSYNC	Yes	Signal also available on pin S115/235. Both interfaces cannot be active simultaneous.
S2/3	MQS_LEFT	CSI_HSYNC	Yes	Signal also available on pin S114/233. Both interfaces cannot be active simultaneous.
S3/5	GND			
S4/7	AUDIO_TXFS	CSI_DATA01	Yes	ESAI, AUD6 or SAI1 interface. Note that CSI_DATA01 is also available on pin S120/245.
S5/9	AUDIO_RXD	CSI_VSYNC	Yes	ESAI, AUD6 or SAI1 interface. Note that CSI_VSYNC is also available on pin S115/235.
S6/11	AUDIO_TXC	CSI_DATA00	Yes	ESAI, AUD6 or SAI1 interface. Note that CSI_DATA00 is also available on pin S119/243.
S7/13	AUDIO_TXD	CSI_HSYNC	Yes	ESAI, AUD6 or SAI1 interface. Note that CSI_HSYNC is also available on pin S114/233.
S8/15	AUDIO_MCLK	CSI_PIXCLK	Yes	ESAI, AUD6 or SAI1 interface Alternative function AUDIO_CLK_OUT. Note that CSI_PIXCLK is also available on pin S117/239.
S9/17	GND			
S10/19	SPDIF_IN	ENET2_COL	Yes	Controlled by alternative pin function SPDIF_IN
S11/21	SPDIF_OUT	ENET1_RX_CLK	Yes	Controlled by alternative pin function SPDIF_OUT
S12/23	CAN2_TX	QSPI1A_DQS	Yes	Controlled by alternative pin function CAN2_TX
S13/25	CAN2_RX	QSPI1B_SS1_B	Yes	Controlled by alternative pin function CAN2_RX
S14/27	CAN1_TX	QSPI1B_DQS	Yes	Controlled by alternative pin function CAN1_TX
S15/29	CAN1_RX	QSPI1A_SS1_B	Yes	Controlled by alternative pin function CAN1_RX
S16/31	GND			
S17/33	LVDS1_D3_P			LVDS interface #1 not assigned on this COM board.
S18/35	LVDS1_D3_N			LVDS interface #1 not assigned on this COM board.
S19/37	GPIO			
S20/39	LVDS1_D2_P			LVDS interface #1 not assigned on this COM board.
S21/41	LVDS1_D2_N			LVDS interface #1 not assigned on this COM board.
S22/43	GND			
S23/45	LVDS1_D1_P			LVDS interface #1 not assigned on this COM board.
S24/47	LVDS1_D1_N			LVDS interface #1 not assigned on this COM board.
S25/49	GND			
S26/51	LVDS1_D0_P			LVDS interface #1 not assigned on this COM board.

S27/53	LVDS1_D0_N			LVDS interface #1 not assigned on this COM board.
S28/55	GND			
S29/57	LVDS1_CLK_P			LVDS interface #1 not assigned on this COM board.
S30/59	LVDS1_CLK_N			LVDS interface #1 not assigned on this COM board.
S31/61	GND			
S32/63	LVDS0_D3_P	LVDS_DATA3_P	No	
S33/65	LVDS0_D3_N	LVDS_DATA3_N	No	
S34/67	GPIO			
S35/69	LVDS0_D2_P	LVDS_DATA2_P	No	
S36/71	LVDS0_D2_N	LVDS_DATA2_N	No	
S37/73	GND			
S38/75	LVDS0_D1_P	LVDS_DATA1_P	No	
S39/77	LVDS0_D1_N	LVDS_DATA1_N	No	
S40/79	GND			
S41/81	LVDS0_D0_P	LVDS_DATA0_P	No	
S42/83	LVDS0_D0_N	LVDS_DATA0_N	No	
S43/85	GND			
S44/87	LVDS0_CLK_P	LVDS_CLK_P	No	
S45/89	LVDS0_CLK_N	LVDS_CLK_N	No	
S46/91	I2C-A_SDA	GPIO1_IO01	Yes	Controlled by alternative pin function I2C1_SDA
S47/93	I2C-A_SCL	GPIO1_IO00	Yes	Controlled by alternative pin function I2C1_SCL
S48/95	I2C-B_SDA	GPIO1_IO03	Yes	Controlled by alternative pin function I2C2_SDA
S49/97	I2C-B_SCL	GPIO1_IO02	Yes	Controlled by alternative pin function I2C2_SCL
S50/99	HDMI/I2C-C_SDA	KEY_ROW4	Yes	Controlled by alternative pin function I2C3_SDA
S51/101	HDMI/I2C-C_SCL	KEY_COL4	Yes	Controlled by alternative pin function I2C3_SCL
S52/103	TP_RST	QSPI1A_DATA3	Yes	Controlled by alternative pin function GPIO4_IO19
S53/105	TP_IRQ	KEY_ROW0	Yes	Controlled by alternative pin function GPIO2_IO15
S54/107	DISP_PWR_EN	ENET1_CRS	Yes	Controlled by alternative pin function GPIO2_IO01
S55/109	BL_PWR_EN	GPIO1_IO09	Yes	Controlled by alternative pin function GPIO4_IO18
S56/111	BL_PWM	USB_H_DATA	Yes	Controlled by alternative pin function PWM2_OUT. Signal can **only be output** since signal pass through a voltage level translator.
S57/113	GND			
S58/115	LCD_R0	LCD1_DATA16	Yes	
S59/117	LCD_R1	LCD1_DATA17	Yes	
S60/119	LCD_R2	LCD1_DATA18	Yes	
S61/121	LCD_R3	LCD1_DATA19	Yes	
S62/123	LCD_R4	LCD1_DATA20	Yes	
S63/125	LCD_R5	LCD1_DATA21	Yes	
S64/127	LCD_R6	LCD1_DATA22	Yes	
S65/129	LCD_R7	LCD1_DATA23	Yes	
S66/131	LCD_G0	LCD1_DATA08	Yes	
S67/133	LCD_G1	LCD1_DATA09	Yes	

S68/135	LCD_G2	LCD1_DATA10	Yes	
S69/137	LCD_G3	LCD1_DATA11	Yes	
S70/139	LCD_G4	LCD1_DATA12	Yes	
S71/141	LCD_G5	LCD1_DATA13	Yes	
S72/143	LCD_G6	LCD1_DATA14	Yes	
S73/145	LCD_G7	LCD1_DATA15	Yes	
S74/147	GND			
S75/149	LCD_B0	LCD1_DATA00	Yes	
151	Non existing pin			
153	Non existing pin			
155	Non existing pin			
S76/157	LCD_B1	LCD1_DATA01	Yes	
S77/159	LCD_B2	LCD1_DATA02	Yes	
S78/161	LCD_B3	LCD1_DATA03	Yes	
S79/163	LCD_B4	LCD1_DATA04	Yes	
S80/165	LCD_B5	LCD1_DATA05	Yes	
S81/167	LCD_B6	LCD1_DATA06	Yes	
S82/169	LCD_B7	LCD1_DATA07	Yes	
S83/171	LCD_CLK	LCD1_CLK	Yes	
S84/173	GPIO7	LCD1_RESET	Yes	GPIO1 controlled by alternative pin function GPIO3_IO27 Typically used as LCD DISPLAY_ENABLE signals.
S85/175	LCD_HSYNC	LCD1_HSYNC	Yes	
S86/177	LCD_VSYNC	LCD1_VSYNC	Yes	
S87/179	LCD_ENABLE	LCD1_ENABLE	Yes	
S88/181	GND			
S89/183	AIN_VREF	ADC_VREFH, AA16	No	
S90/185	AIN7	ADC2_IN3	No	
S91/187	AIN6	ADC2_IN2	No	
S92/189	AIN5	ADC2_IN1	No	
S93/191	AIN4	ADC2_IN0	No	
S94/193	AIN3	ADC1_IN3	No	
S95/195	AIN2	ADC1_IN2	No	
S96/197	AIN1	ADC1_IN1	No	
S97/199	AIN0	ADC1_IN0	No	
S98/201	GND			
S99/203	COM board specific	VADC_IN0	No	
S100/205	COM board specific	VADC_IN1	No	
S101/207	GND			
S102/209	COM board specific	VADC_IN2	No	
S103/211	COM board specific	VADC_IN3	No	
S104/213	GND			
S105/215	COM board specific			

S106/217	COM board specific			
S107/219	COM board specific			
S108/221	COM board specific			
S109/223	COM board specific			
S110/225	COM board specific			
S111/227	COM board specific			
S112/229	COM board specific			
S113/231	COM board specific			
S114/233	CSI_HSYNC	CSI_HSYNC	Yes	Signal also available on pin S2/3. Both interfaces cannot be active simultaneous.
S115/235	CSI_VSYNC	CSI_VSYNC	Yes	Signal also available on pin S1/1. Both interfaces cannot be active simultaneous.
S116/237	CSI_MCLK	CSI_MCLK	Yes	
S117/239	CSI_PCLK	CSI_PIXCLK	Yes	
S118/241	GND			
S119/243	CSI_D0	CSI_DATA00	Yes	
S120/245	CSI_D1	CSI_DATA01	Yes	
S121/247	CSI_D2	CSI_DATA02	Yes	
S122/249	CSI_D3	CSI_DATA03	Yes	
S123/251	CSI_D4	CSI_DATA04	Yes	
S124/253	CSI_D5	CSI_DATA05	Yes	
S125/255	CSI_D6	CSI_DATA06	Yes	
S126/257	CSI_D7	CSI_DATA07	Yes	
S127/259	GND			
S128/261	CSI_D3_M			CSI/MIPI interface not assigned on this COM board.
S129/263	CSI_D3_P			CSI/MIPI interface not assigned on this COM board.
S130/265	GND			
S131/267	CSI_D2_M			CSI/MIPI interface not assigned on this COM board.
S132/269	CSI_D2_P			CSI/MIPI interface not assigned on this COM board.
S133/271	GND			
S134/273	CSI_D1_M			CSI/MIPI interface not assigned on this COM board.
S135/275	CSI_D1_P			CSI/MIPI interface not assigned on this COM board.
S136/277	GND			
S137/279	CSI_D0_M			CSI/MIPI interface not assigned on this COM board.
S138/281	CSI_D0_P			CSI/MIPI interface not assigned on this COM board.
S139/283	GND			
S140/285	CSI_CLK_M			CSI/MIPI interface not assigned on this COM board.
S141/287	CSI_CLK_P			CSI/MIPI interface not assigned on this COM board.
S142/289	GND			
S143/291	SATA_TX_P			SATA interface not assigned on this COM board.
S144/293	SATA_TX_N			SATA interface not assigned on this COM board.
S145/295	GND			
S146/297	SATA_RX_N			SATA interface not assigned on this COM board.

S147/299	SATA_RX_P			SATA interface not assigned on this COM board.
S148/301	GND			
S149/303	GND			
S150/305	PCIE_CLK_P	CCM_CLK1_P	No	100 MHz PCIE clock signal generated by CCM_CLK1 outputs.
S151/307	PCIE_CLK_N	CCM_CLK1_N	No	100 MHz PCIE clock signal generated by CCM_CLK1 outputs.
S152/309	GND			
S153/311	PCIE_TX_P	PCIE_TX_P	No	
S154/313	PCIE_TX_N	PCIE_TX_N	No	
S155/315	GND			
S156/317	PCIE_RX_P	PCIE_RX_P	No	
S157/319	PCIE_RX_N	PCIE_RX_N	No	
S158/321	GND			

4 Pin Mapping

4.1 Functional Multiplexing on I/O Pins

There are a lot of different peripherals inside the i.MX 6SoloX SoC. Many of these peripherals are connected to the IOMUX block, that allows the I/O pins to be configured to carry one of many (up to nine different) alternative functions. This leave great flexibility to select a function multiplexing scheme for the pins that satisfy the interface need for a particular application.

Some interfaces with specific voltage levels/drivers/transceivers have dedicated pins, like PCIe, SATA, HDMI, MIPI and LVDS. i.MX 6SoloX pins carrying these signals do not have any functional multiplexing possibilities. These interfaces are fixed.

To keep compatibility between COM boards the EACOM specified pinning should be followed, but in general there are no restrictions to select alternative pin multiplexing schemes on the iMX6 SoloX COM Board. Note that all EACOM-defined pins are not connected on some COM boards, typically because an interface is not supported or there are not enough free pins in the SoC. Further, some COM board pins are *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using *type specific* pins may result in lost compatibility between EACOM boards, but not always. Always check details between EACOM boards of interest.

If switching between EACOM board is not needed, then pin multiplexing can be done without considering the EACOM pin allocation. A custom carrier board design is needed in this case.

Functional multiplexing is normally controlled via the Linux BSP. It can also be done directly via register `IOMUXC_SW_MUX_CTL_PAD_xxx` where `xxx` is the name of the iMX6SoloX pin. For more information about the register settings, see the *iMX6SoloX Reference Manual* from NXP.

Note that input functions that are available on multiple pins will require control of an input multiplexer. This is controlled via register `IOMUXC_xxx_SELECT_INPUT` where `xxx` is the name of the input function. Again, for more information about the register settings, see the *iMX6SoloX Reference Manual* from NXP.

4.1.1 Alternative I/O Function List

There is an accompanying Excel document that lists all alternative functions for each available I/O pin. Reset state (typically GPIO, ALT5 function, except for two pins) is shown as well as the EACOM function allocation.

4.2 I/O Pin Control

Each pin also has an additional control register for configuring input hysteresis, pull up/down resistors, push-pull/open-drain driving, drive strength and more. Also in this case, configuration is normally done via the Linux BSP but it is possible to directly access the control registers, which are called `IOMUXC_SW_PAD_CTL_PAD_xxx` where `xxx` is the name of the i.MX 6SoloX pin. For more information about the register settings, see the *iMX6SoloX Reference Manual* from NXP.

Note that most pins are configured as GPIO inputs, with a 100Kohm pull-down resistor, after reset. When the bootloader (typically u-boot) executes it is possible to reconfigure the pins.

5 Interface Description

This chapter lists details about all different interfaces. The **i.MX 6SoloX datasheet and user manual should always be consulted** for details about different functions and interfaces. Many interfaces are multiplexed on different pins and not available simultaneously.

5.1 Analogue Inputs

This section lists signals related to analog inputs.

The i.MX 6SoloX SoC has two 12-bit ADC modules with 4 dedicated single-ended inputs, which equals 8 analogue inputs in total. A sample rate of up to about 1.4MHz can be configured. Input voltage range is from ground to ADC_VREFH voltage.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S97/199	ADC_IN0	ADC1_IN0	AI	Analog input #0 to ADC#1	
S96/197	ADC_IN1	ADC1_IN1	AI	Analog input #1 to ADC#1	
S95/195	ADC_IN2	ADC1_IN2	AI	Analog input #2 to ADC#1	
S94/193	ADC_IN3	ADC1_IN3	AI	Analog input #3 to ADC#1	
S93/191	ADC_IN4	ADC2_IN0	AI	Analog input #0 to ADC#2	
S92/189	ADC_IN5	ADC2_IN1	AI	Analog input #1 to ADC#2	
S91/187	ADC_IN6	ADC2_IN2	AI	Analog input #2 to ADC#2	
S90/185	ADC_IN7	ADC2_IN3	AI	Analog input #3 to ADC#2	
S89/183	ADC_VREFH		AO	Positive reference voltage for ADC inputs (not related to VADC inputs)	Connected to an internal 3.0-3.3V supply, i.MX 6SoloX ball AA16. **Note**: this is not an input voltage, but rather an observation of internal reference voltage.

5.2 Analogue Video Interface

This section lists signals related to Video Analogue-to-Digital Converter (VADC) interface.

The i.MX 6SoloX SoC has one VADC input interface that consists of an analog video front end (AFE) and a digital video decoder. The AFE accepts NTSC or PAL input from a device such as an (inexpensive) analog camera and digitizes the analog video signal. The input video signal can be selected from one of four inputs, VIN0-VIN3.
The video decoder outputs YUV444-formatted data that can be routed to the CSI/LCDIF/PXP blocks for further processing.

The *EACOM Board specification* defines four general high-frequency analog in puts. The VADC signals are allocated to these pins. The table below lists the pin assignment according to *EACOM Board specification*.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S103/211	VADC_IN0	VADC_IN0	AI	Analogue video channel #0	
S102/209	VADC_IN1	VADC_IN1	AI	Analogue video channel #1	
S100/205	VADC_IN2	VADC_IN2	AI	Analogue video channel #2	
S99/203	VADC_IN3	VADC_IN3	AI	Analogue video channel #3	

5.3 CAN

This section lists signals related to the Controller Area Network (CAN) interface.

The i.MX6 SoloX SoC has two Flexible Controller Area Network (FlexCAN) interfaces that supports bitrates of up to 1Mbps each. The FlexCAN module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification, which supports both standard and extended message frames.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S12/23	CAN2_TX	QSPI1A_DQS	O	CAN port 2 transmit signal	Default location for EACOM Board spec.
S13/25	CAN2_RX	QSPI1B_SS1_B	I	CAN port 2 receive signal	Default location for EACOM Board spec.
S14/27	CAN1_TX	QSPI1B_DQS	O	CAN port 1 transmit signal	Default location for EACOM Board spec.
S15/29	CAN1_RX	QSPI1A_SS1_B	I	CAN port 1 receive signal	Default location for EACOM Board spec.
P129/266	UART3_TX	KEY_COL3	O	CAN port 2 transmit signal	Alternative location for CAN2_TX signal
P128/264	UART3_RX	KEY_ROW3	I	CAN port 2 receive signal	Alternative location for CAN2_RX signal
P2/4	GPIO5	KEY_COL2	O	CAN port 1 transmit signal	Alternative location for CAN1_TX signal
P1/2	GPIO6	KEY_ROW2	I	CAN port 1 receive signal	Alternative location for CAN1_RX signal

5.4 Display Interfaces

This section lists signals related to Enhanced LCD Interface (eLCDIF) and LVDS Display Bridge (LDB) functions.

The i.MX 6SoloX SoC has an advanced, feature rich display and graphics subsystem with several key components:

- PXP pixel pipeline
- Graphic Processing Unit (GPU) support for 2D/3D
- Dual LCD interfaces (LCDIF), which are 24-bit parallel RGB LCD interfaces
- LVDS interface
- Dual CSI interfaces, which are up to 24-bit parallel interface for image sensors
- Video ADC
- TV decoder

The picture below shows the high-level structure of the display and graphics subsystem in the i.MX 6SoloX.

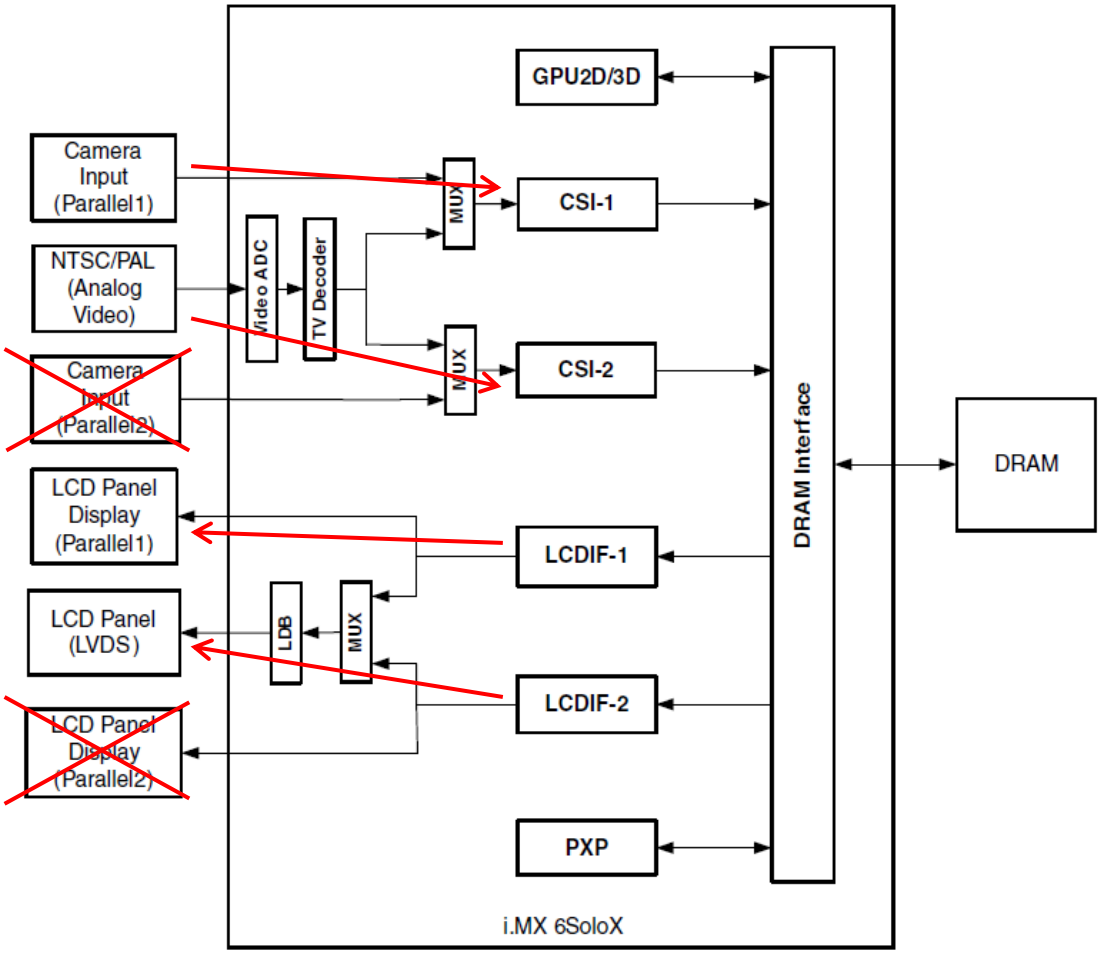


Figure 4 – Structure of Display and Graphics Subsystem

The iMX6 SoloX COM board has allocated pins (according to the *EACOM Board specification*) for one parallel camera input, analogue video inputs, one parallel LCD output and one LVDS output interface. There is no access to parallel camera input #2 or parallel LCD output #2. The data source for CSI-2 is the analogue video inputs. If two displays are needed, the output from LCDIF-2 is routed to the LVDS interface.

5.4.1 Parallel RGB LCD Interface

This section lists signals for the parallel RGB LCD interface.

The LCDIF supports one display with up to 1920x1200 pixel resolution (WUXGA) and 24-bit color. The parallel RGB LCD interface is ideal for smaller, lower resolution displays. Note that due to EMI, LVDS is a better choice of interface for high resolution displays.

The *EACOM Board specification* defines an 24-bit parallel LCD interface. The table below lists the pin assignment according to *EACOM Board specification*. For best portability it is recommended to always have the LCD interface running in 24-bit mode. If less bits are needed in a specific LCD implementation the LSB bits of each color is just ignored, see the three rightmost columns.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Color Config. for 16-bit 565RGB	Color Config. for 18-bit 666RGB	Color Config. for 16-bit 565RGB if interface set to 24-bit	Color Config. for 18-bit 666RGB if interface set to 24-bit	Color Config. for 24-bit 888RGB
S75/149	LCD_DATA00	LCD1_DATA00	O	B0	B0			B0
S76/157	LCD_DATA01	LCD1_DATA01	O	B1	B1			B1

S77/159	LCD_DATA02	LCD1_DATA02	O	B2	B2		B2	B2
S78/161	LCD_DATA03	LCD1_DATA03	O	B3	B3	B3	B3	B3
S79/163	LCD_DATA04	LCD1_DATA04	O	B4	B4	B4	B4	B4
S80/165	LCD_DATA05	LCD1_DATA05	O	G0	B5	B5	B5	B5
S81/167	LCD_DATA06	LCD1_DATA06	O	G1	G0	B6	B6	B6
S82/169	LCD_DATA07	LCD1_DATA07	O	G2	G1	B7	B7	B7
S66/131	LCD_DATA08	LCD1_DATA08	O	G3	G2			G0
S67/133	LCD_DATA09	LCD1_DATA09	O	G4	G3			G1
S68/135	LCD_DATA10	LCD1_DATA10	O	G7	G4	G2	G2	G2
S69/137	LCD_DATA11	LCD1_DATA11	O	R0	G5	G3	G3	G3
S70/139	LCD_DATA12	LCD1_DATA12	O	R1	R0	G4	G4	G4
S71/141	LCD_DATA13	LCD1_DATA13	O	R2	R1	G5	G5	G5
S72/143	LCD_DATA14	LCD1_DATA14	O	R3	R2	G6	G6	G6
S73/145	LCD_DATA15	LCD1_DATA15	O	R4	R3	G7	G7	G7
S58/115	LCD_DATA16	LCD1_DATA16	O		R4			R0
S59/117	LCD_DATA17	LCD1_DATA17	O		R5			R1
S60/119	LCD_DATA18	LCD1_DATA18	O				R2	R2
S61/121	LCD_DATA19	LCD1_DATA19	O			R3	R3	R3
S62/123	LCD_DATA20	LCD1_DATA20	O			R4	R4	R4
S63/125	LCD_DATA21	LCD1_DATA21	O			R5	R5	R5
S64/127	LCD_DATA22	LCD1_DATA22	O			R6	R6	R6
S65/129	LCD_DATA23	LCD1_DATA23	O			R7	R7	R7
S85/175	LCD_HSYNC	LCD1_HSYNC	O	Horizontal (line) synchronization				
S86/177	LCD_VSYNC	LCD1_VSYNC	O	Vertical (frame) synchronization				
S87/179	LCD_ENABLE	LCD1_ENABLE	O	Data enable				
S83/171	LCD_CLK	LCD1_CLK	O	Pixel (dot) clock				

The *EACOM Board specification* has allocated some additional signals that are typically needed to implement an LCD interface. The table below list these signals.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S56/111	BL_CRTL_PWM	USB_H_DATA	O	PWM signal to control backlight contrast.	Signal is connected to PWM2_OUT
S55/109	BL_PWR_EN	GPIO1_IO09	O	Power control for backlight. Active high	
S54/107	DISP_PWR_EN	ENET1_CRS	O	Power control for LCD power supply. Active high	Signal is connected to GPIO2_IO01
S53/105	TP_IRQ	KEY_ROW0	I	Interrupt from touch controller	Signal is connected to GPIO2_IO15
S52/103	TP_RST	QSPI1A_DATA3	O	Reset signal to touch controller. Active low	Signal is connected to GPIO4_IO19
S47/93	I2C-A_SCL	GPIO1_IO00	I/O	Clock signal of I2C channel A	It is recommended to connect the RGB LCD touch controller (if I2C interface) to this channel.
S46/91	I2C-A_SDA	GPIO1_IO01	I/O	Data signal of I2C channel A	It is recommended to connect the RGB LCD touch controller (if I2C interface)

					to this channel.
S49/97	I2C-B_SCL	GPIO1_IO02	I/O	Clock signal of I2C channel B	It is recommended to connect the LVDS touch controller (if I2C interface) to this channel.
S48/95	I2C-B_SDA	GPIO1_IO03	I/O	Data signal of I2C channel B	It is recommended to connect the LVDS touch controller (if I2C interface) to this channel.

5.4.2 LVDS Interface

This section lists signals for the LVDS interface.

The purpose of the LVDS interface is to serialize the parallel RGB and control signals to an external display. The parallel RGB data stream can be either 18 or 24 bits wide. The three control signals; HSYNC, VSYNC and ENABLE along with the pixel/dot clock are also serialized.

The LVDS interface supports resolutions up to WXGA 1366x768 pixels @ 60 frames per second (85MHz pixel clock maximum)

Two signal mappings are supported. Below is the so called *SPWG/PSWG/VESA 18/24 bpp Data Mapping*.

Serializer Input	Slot 0	Slot 1	Slot 2	Slot 3	Slot 4	Slot 5	Slot 6
LVDS_DATA0	G0	R5	R4	R3	R2	R1	R0
LVDS_DATA1	B1	B0	G5	G4	G3	G2	G1
LVDS_DATA2	DE	VS	HS	B5	B4	B3	B2
LVDS_DATA3 (only in 24-bit data)	N/A	B7	B6	G7	G6	R7	R6

The other signal mapping is called *JEIDA 24bpp Data Mapping*.

Serializer Input	Slot 0	Slot 1	Slot 2	Slot 3	Slot 4	Slot 5	Slot 6
LVDS_DATA0	G2	R7	R6	R5	R4	R3	R2
LVDS_DATA1	B3	B2	G7	G6	G5	G4	G3
LVDS_DATA2	DE	VS	HS	B7	B6	B5	B4
LVDS_DATA3	N/A	B1	B0	G1	G0	R1	R0

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S42/83	LVDS0_D0_N	LVDS_DATA0_N	O	Differential data pair #0, negative signal	
S41/81	LVDS0_D0_P	LVDS_DATA0_P	O	Differential data pair #0, positive signal	
S39/77	LVDS0_D1_N	LVDS_DATA1_N	O	Differential data pair #1, negative signal	
S38/75	LVDS0_D1_P	LVDS_DATA1_P	O	Differential data pair #1, positive signal	
S36/71	LVDS0_D2_N	LVDS_DATA2_N	O	Differential data pair #2, negative signal	
S35/69	LVDS0_D2_P	LVDS_DATA2_P	O	Differential data pair #2, positive signal	
S33/65	LVDS0_D3_N	LVDS_DATA3_N	O	Differential data pair #3, negative signal	Pair not used in 18-bit color depth.

S32/63	LVDS0_D3_P	LVDS_DATA3_P	O	Differential data pair #3, positive signal	Pair not used in 18-bit color depth.
S45/89	LVDS0_CLK_N	LVDS_CLK_N	O	Differential clock pair, negative signal	
S44/87	LVDS0_CLK_P	LVDS_CLK_P	O	Differential clock pair, positive signal	

LVDS interface #1 (as defined in the *EACOM Board specification*) is not utilized by the iMX6 SoloX COM Board since the i.MX 6SoloX only has one LVDS interface.

5.5 Digital Audio Interfaces: Synchronous Serial Interface and AUDMUX

This section lists signals related to the Synchronous Serial Interfaces (SSI) and Digital Audio Mux (AUDMUX) functions.

The i.MX 6SoloX SoC contains an audio subsystem. It consists of three Synchronous Serial Interfaces (SSI1-SSI3). The SSI block is a full-duplex serial port that allows communication with external devices using a variety of serial protocols (like SSI normal/network, I2S and AC-97), up to 24-bits per word and different clock/frame options.

The three SSI interfaces are not directly connected to the IOMUX, but instead to a block called Digital Audio Mux (AUDMUX). The AUDMUX routes audio data (it does not decode or process the data) and can be operational even when the SoC is in a low-power mode.

The picture below illustrates the programmable interconnect fabric that AUDMUX implements. There are four ports that are connected to IOMUX; AUD3, AUD4, AUD5, AUD6.

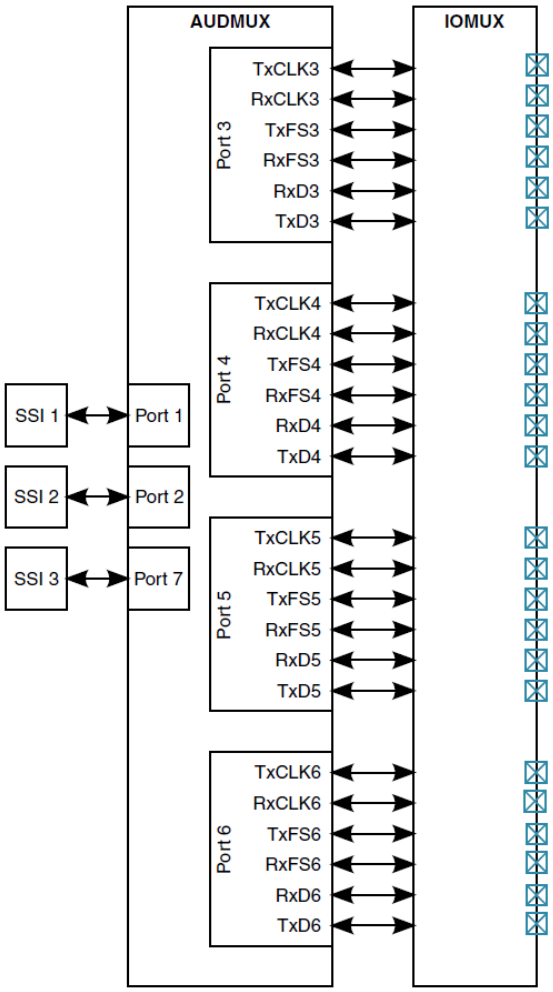


Figure 5 – iMX6SoloX AUDMUX System Block Diagram

The table below lists pins that have been allocated according to the *EACOM Board specification*. AUDMUX port 6 (AUD6) is used with **synchronous** transmit and receive sections (meaning that transmit and receive share the clock and frame synch signals). Note that all signals used are also routed to other pins (in the CSI interface). Ensure that both interfaces are not used simultaneous.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S5/9 S115/235	AUDIO_RXD CSI_VSYNC	CSI_VSYNC	I	Data receive signal Ch#6	Alternative function AUD6_RXD. Note that CSI_VSYNC is also available on pin S115/235.
S6/11 S119/243	AUDIO_TXC CSI_D0	CSI_DATA00	O	Transmit clock signal Ch#6. Also work as Receive clock signal Ch#6	Alternative function AUD6_TXC. Note that CSI_DATA00 is also available on pin S119/243.
S7/13 S114/233	AUDIO_TXD CSI_HSYNC	CSI_HSYNC	O	Data transmit signal Ch#6	Alternative function AUD6_TXD. Note that CSI_HSYNC is also available on pin S114/233.
S4/7 S120/245	AUDIO_TXFS CSI_D1	CSI_DATA01	O	Transmit Frame sync signal Ch#6. Also work as Receive Frame sync signal Ch#6	Alternative function AUD6_TXFS. Note that CSI_DATA01 is also available on pin S120/245.
S8/15 S117/239	AUDIO_MCLK CSI_PIXCLK	CSI_PIXCLK	O	Clock output signal	Alternative function AUDIO_CLK_OUT. Note that CSI_PIXCLK is also available on pin S117/239.

The signal AUDIO_MCLK is included in the digital audio interface since codecs often requires this clock (but not always). The table below lists alternative pins available for the AUDIO_CLK_OUT signal.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P135/278	UART-A_CTS	GPIO1_IO07	O	Clock output signal	Alternative function AUDIO_CLK_OUT
P4/8	GPIO3	SD4_RESET_B	O	Clock output signal	Alternative function AUDIO_CLK_OUT

The table below lists pins available for the AUDMUX port 3 (AUD3) interface.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S83/171	LCD_CLK	LCD1_CLK	I	Receive clock signal Ch#3	Alternative function AUD3_RXC
P18/36	MMC_CMD	SD4_CMD	I	Receive clock signal Ch#3	Alternative function AUD3_RXC
S84/173	GPIO7	LCD1_RESET	I	Data receive signal Ch#3	Alternative function AUD3_RXD
P13/26	MMC_D0	SD4_DATA0	I	Data receive signal Ch#3	Alternative function AUD3_RXD
P16/32	MMC_CLK	SD4_CLK	I	Receive Frame sync signal Ch#3	Alternative function AUD3_RXFS
S87/179	LCD_ENABLE	LCD1_ENABLE	O	Transmit clock signal Ch#3	Alternative function AUD3_TXC
P12/24	MMC_D1	SD4_DATA1	O	Transmit clock signal Ch#3	Alternative function AUD3_TXC
S85/175	LCD_HSYNC	LCD1_HSYNC	O	Data transmit signal Ch#3	Alternative function AUD3_TXD
P20/40	MMC_D3	SD4_DATA3	O	Data transmit signal Ch#3	Alternative function AUD3_TXD
S86/177	LCD_VSYNC	LCD1_VSYNC	O	Transmit Frame sync signal Ch#3	Alternative function AUD3_TXFS
P21/42	MMC_D2	SD4_DATA2	O	Transmit Frame sync signal Ch#3	Alternative function AUD3_TXFS

Several signals of the AUDMUX port 4 (AUD4) interface are not available due to internal pin assignment. It is not recommended to use this interface but for completeness, the available signals are listed below.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S10/19	SPDIF_IN	ENET2_COL	I	Receive clock signal Ch#4	Alternative function AUD4_RXC
S54/107	DISP_PWR_EN	ENET1_CRS	O	Data transmit signal Ch#4	Alternative function AUD4_TXD
S11/21	SPDIF_OUT	ENET1_RX_CLK	O	Transmit Frame sync signal Ch#4	Alternative function AUD4_TXFS

The table below lists pins available for the AUDMUX port 5 (AUD5) interface.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S51/101	I2C-C_SCL	KEY_COL4	I	Receive clock signal Ch#5	Alternative function AUD5_RXC
P139/286	GPIO2	SD1_CMD	I	Receive clock signal Ch#5	Alternative function AUD5_RXC
P130/268	UART-B_RXD	SD1_DATA0	I	Data receive signal Ch#5	Alternative function AUD5_RXD
P132/272	UART-B_RTS	SD1_DATA3	I	Data receive signal Ch#5	Alternative function AUD5_RXD
S50/99	I2C-C_SDA	KEY_ROW4	I	Receive Frame sync signal Ch#5	Alternative function AUD5_RXFS
P140/288	GPIO1	SD1_CLK	I	Receive Frame sync signal Ch#5	Alternative function AUD5_RXFS
P133/274	UART-B_TXD	SD1_DATA1	O	Transmit clock signal Ch#5	Alternative function AUD5_TXC
S53/105	TP_IRQ	KEY_ROW0	O	Data transmit signal Ch#5	Alternative function AUD5_TXD
P132/272	UART-B_RTS	SD1_DATA3	O	Data transmit signal Ch#5	Alternative function AUD5_TXD
P131/270	UART-B_CTS	SD1_DATA2	O	Transmit Frame sync signal Ch#5	Alternative function AUD5_TXFS

Besides the AUDMUX port 6 signals allocated in the *EACOM Board specification* there are more (alternative) pins for the AUDMUX port 6 (AUD6) interface. The table below lists these pins.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S115/235 S5/9	CSI_VSYNC AUDIO_RXD	CSI_VSYNC	I	Data receive signal Ch#6	Alternative function AUD6_RXD. Note that CSI_VSYNC is also available on pin S5/9.
P6/12	SD_D0	SD2_DATA0	I	Data receive signal Ch#6	Alternative function AUD6_RXD
S121/247	CSI_D2	CSI_DATA02	I	Receive clock signal Ch#6	Alternative function AUD6_RXC
P8/16	SD_CMD	SD2_CMD	I	Receive clock signal Ch#6	Alternative function AUD6_RXC
S122/249	CSI_D3	CSI_DATA03	I	Receive Frame sync signal Ch#6	Alternative function AUD6_RXFS
P7/14	SD_CLK	SD2_CLK	I	Receive Frame sync signal Ch#6	Alternative function AUD6_RXFS
S119/243 S6/11	CSI_D0 AUDIO_TXC	CSI_DATA00	O	Transmit clock signal Ch#6	Alternative function AUD6_TXC. Note that CSI_DATA00 is also available on pin S6/11.
P5/10	SD_D1	SD2_DATA1	O	Transmit clock signal Ch#6	Alternative function AUD6_TXC
S114/233 S7/13	CSI_HSYNC AUDIO_TXD	CSI_HSYNC	O	Data transmit signal Ch#6	Alternative function AUD6_TXD. Note that CSI_HSYNC is also available on pin S7/13.
P9/18	SD_D3	SD2_DATA3	O	Data transmit signal Ch#6	Alternative function AUD6_TXD
S120/245 S4/7	CSI_D1 AUDIO_TXFS	CSI_DATA01	O	Transmit Frame sync signal Ch#6	Alternative function AUD6_TXFS. Note that CSI_DATA01 is also available on pin S4/7.
P10/20	SD_D2	SD2_DATA2	O	Transmit Frame sync signal Ch#6	Alternative function AUD6_TXFS

5.6 Digital Audio Interfaces: ESAI

This section lists signals related to the Enhanced Serial Audio Interface (ESAI) function.

EASI is part of the i.MX 6SoloX SoC audio subsystem. provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, Sony/Phillips Digital Interface (SPDIF) transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator.

There are no specific ESAI pins defined in the *EACOM Board specification*. ESAI pins are only available as alternative functions on certain pins. The table below lists the available pins.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S121/247	CSI_D2	CSI_DATA02	I/O	RX serial bit clock	Alternative function ESAI_RX_CLK
P121/250	SPI-B_MISO	QSPI1B_DATA1	I/O	RX serial bit clock	Alternative function ESAI_RX_CLK
S122/249	CSI_D3	CSI_DATA03	I/O	RX frame sync signal	Alternative function ESAI_RX_FS
P120/248	SPI-B_MOSI	QSPI1B_DATA0	I/O	RX frame sync signal	Alternative function ESAI_RX_FS
S117/239 S8/15	CSI_PIXCLK AUDIO_MCLK	CSI_PIXCLK	I/O	RX high frequency clock	Alternative function ESAI_RX_HF_CLK
P122/252	SPI-B_CLK	QSPI1B_SCLK	I/O	RX high frequency clock	Alternative function ESAI_RX_HF_CLK
S114/233 S7/13	CSI_HSYNC AUDIO_TXD	CSI_HSYNC	I/O	ESAI_TX0 serial transmit data	Alternative function ESAI_TX0
S52/103	TP_RST	QSPI1A_DATA3	I/O	ESAI_TX0 serial transmit data	Alternative function ESAI_TX0
S123/251	CSI_D4	CSI_DATA04	I/O	ESAI_TX1 serial transmit data	Alternative function ESAI_TX1
P125/258	SPI-A_MISO	QSPI1A_DATA1	I/O	ESAI_TX1 serial transmit data	Alternative function ESAI_TX1
S125/255	CSI_D6	CSI_DATA06	I/O	ESAI_TX2 serial transmit data or ESAI_RX3 serial receive data	Alternative function ESAI_TX2_RX3
P126/260	SPI-A_CLK	QSPI1A_SCLK	I/O	ESAI_TX2 serial transmit data or ESAI_RX3 serial receive data	Alternative function ESAI_TX2_RX3
S126/257	CSI_D7	CSI_DATA07	I/O	ESAI_TX3 serial transmit data or ESAI_RX2 serial receive data	Alternative function ESAI_TX3_RX2
P123/254	SPI-A_SSEL	QSPI1A_SS0_B	I/O	ESAI_TX3 serial transmit data or ESAI_RX2 serial receive data	Alternative function ESAI_TX3_RX2
S124/253	CSI_D5	CSI_DATA05	I/O	ESAI_TX4 serial transmit data or ESAI_RX1 serial receive data	Alternative function ESAI_TX4_RX1
P124/256	SPI-A_MOSI	QSPI1A_DATA0	I/O	ESAI_TX4 serial transmit data or ESAI_RX1 serial receive data	Alternative function ESAI_TX4_RX1
S115/235 S5/9	CSI_VSYNC AUDIO_RXD	CSI_VSYNC	I/O	ESAI_TX5 serial transmit data or ESAI_RX0 serial receive data	Alternative function ESAI_TX5_RX0
S119/243 S6/11	CSI_D0 AUDIO_TXC	CSI_DATA00	I/O	TX serial bit clock	Alternative function ESAI_TX_CLK
P73/146	USB_OTG1_PWR	QSPI1A_DATA2	I/O	TX serial bit clock	Alternative function ESAI_TX_CLK
S120/245 S4/7	CSI_D1 AUDIO_TXFS	CSI_DATA01	I/O	TX frame sync (and RX if synchronous mode)	Alternative function ESAI_TX_FS
S116/237	CSI_MCLK	CSI_MCLK	I/O	TX high frequency clock	Alternative function ESAI_TX_HF_CLK
S117/239 S8/15	CSI_PIXCLK AUDIO_MCLK	CSI_PIXCLK	I/O	TX high frequency clock	Alternative function ESAI_TX_HF_CLK
P119/246	SPI-B_SSEL	QSPI1B_SS0_B	I/O	TX high frequency clock	Alternative function ESAI_TX_HF_CLK

5.7 Digital Audio Interfaces: S/PDIF

This section lists signals related to the Sony/Philips Digital Interface (SPDIF) function.

The i.MX 6SoloX SoC has one SPDIF interface, which is a stereo transceiver that allows the processor to receive and transmit digital audio according to the AES/EBU IEC 60958 standard.

The *EACOM Board specification* defines one input and one output SPDIF interface. The table below lists the pin assignment according to *EACOM Board specification*.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S10/19	SPDIF_IN	ENET2_COL	I	Input line	
S11/21	SPDIF_OUT	ENET1_RX_CLK	O	Output line signal	

There are alternative locations for the SPDIF pins as well as some clock signals that are not used very often. The table below lists these alternative pin locations.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S124/253	CSI_D5	CSI_DATA05	I	Input line	Alternative function SPDIF_IN
P76/160	USB_H1_OC	GPIO1_IO11	I	Input line	Alternative function SPDIF_IN
P9/18	SD_D3	SD2_DATA3	I	Input line	Alternative function SPDIF_IN
P17/34	MMC_D5	SD4_DATA5	I	Input line	Alternative function SPDIF_IN
S123/251	CSI_D4	CSI_DATA04	O	Output line signal	Alternative function SPDIF_OUT
P75/158	USB_H1_PWR	GPIO1_IO12	O	Output line signal	Alternative function SPDIF_OUT
P10/20	SD_D2	SD2_DATA2	O	Output line signal	Alternative function SPDIF_OUT
P19/38	MMC_D4	SD4_DATA4	O	Output line signal	Alternative function SPDIF_OUT
P66/132	USB_O1_ID	GPIO1_IO10	I	External clock signal	Alternative function SPDIF_EXT_CLK
S54/107	DISP_PWR_EN	ENET1_CRS	O	Lock signal	Alternative function SPDIF_LOCK

5.8 Digital Audio Interfaces: MQS

This section lists signals related to the Medium Quality Sound (MQS) function.

The i.MX 6SoloX SoC has one MQS block that can generate audio via PWM modulation on digital output pins. MQS provides only simple audio reproduction. No internal pop, click or distortion artifact reduction methods are provided

The *EACOM Board specification* defines a stereo output for MQS sound signals. The table below lists the pin assignment according to *EACOM Board specification*.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S2/3	MQS_LEFT	CSI_HSYNC	O	Left signal output	Signal CSI_HSYNC is also available on pin S114/233.
S1/1	MQS_RIGHT	CSI_VSYNC	O	Right signal output	Signal CSI_HSYNC is also available on pin S115/235.

The table below lists these the alternative pin locations are.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P8/16	SD_CMD	SD2_CMD	O	Left signal output	Alternative function MQS_LEFT
P7/14	SD_CLK	SD2_CLK	O	Right signal output	Alternative function MQS_RIGHT

5.9 Ethernet

This section lists signals related to the Ethernet interfaces.

The iMX6SoloX has two Gigabit Ethernet controllers (10/100/1000Mbps) that are IEEE1588 compliant. There are two 10/100/1000 Mbps Ethernet interfaces on the board. Atheros AR8031 Integrated 10/100/1000 Mbps Ethernet Transceiver is used as external PHY and is connected via the RGMII interface to the iMX6SoloX.

The Ethernet interface consists of 4 pairs of low voltage differential pair signals plus three link indicator activity signals. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

COM Board Pin	EACOM Board Name	AR8031 Pin	I/O	Description	Remarks
P39/78	ETH1_TRXP0	AR8031 #1 pin 11	I/O	Media Dependent Interface	
P40/80	ETH1_TRXN0	AR8031 #1 pin 12	I/O	Media Dependent Interface	
P36/72	ETH1_TRXP1	AR8031 #1 pin 14	I/O	Media Dependent Interface	
P37/74	ETH1_TRXN1	AR8031 #1 pin 15	I/O	Media Dependent Interface	
P48/96	ETH1_TRXP2	AR8031 #1 pin 17	I/O	Media Dependent Interface	
P47/94	ETH1_TRXN2	AR8031 #1 pin 18	I/O	Media Dependent Interface	
P45/90	ETH1_TRXP3	AR8031 #1 pin 20	I/O	Media Dependent Interface	
P44/88	ETH1_TRXN3	AR8031 #1 pin 21	I/O	Media Dependent Interface	
P42/84	ETH1_LED_ACT	AR8031 #1 pin 23	O	LED indicator output	Signal toggles during TX/RX activity.
P43/86	ETH1_LED_LINK	AR8031 #1 pin 26	O	LED indicator output	Signal high when 100M link is active.
P41/82	ETH1_LED_LINK1000	AR8031 #1 pin 24	O		Signal high when 1000M link is connected or active.
P53/106	ETH2_TRXP0	AR8031 #2 pin 11	I/O	Media Dependent Interface	
P54/108	ETH2_TRXN0	AR8031 #2 pin 12	I/O	Media Dependent Interface	
P50/100	ETH2_TRXP1	AR8031 #2 pin 14	I/O	Media Dependent Interface	
P51/102	ETH2_TRXN1	AR8031 #2 pin 15	I/O	Media Dependent Interface	
P62/124	ETH2_TRXP2	AR8031 #2 pin 17	I/O	Media Dependent Interface	
P61/122	ETH2_TRXN2	AR8031 #2 pin 18	I/O	Media Dependent Interface	
P59/118	ETH2_TRXP3	AR8031 #2 pin 20	I/O	Media Dependent Interface	
P58/116	ETH2_TRXN3	AR8031 #2 pin 21	I/O	Media Dependent Interface	
P56/112	ETH2_LED_ACT	AR8031 #2 pin 23	O	LED indicator output	Signal toggles during TX/RX activity.
P57/114	ETH2_LED_LINK100	AR8031 #2 pin 26	O	LED indicator output	Signal high when 100M link is active.
P55/110	ETH2_LED_LINK1000	AR8031 #2 pin 24	O		Signal high when 1000M link is connected or active.

The external PHYs can be powered down in order to lower the power consumption to a minimum.

If only fast Ethernet is required, 10/100Mbit magnetics with only 2 lanes are sufficient. In this case, MDI2 and MDI3 can be left unconnected.

Below is a list of suggested magnetics for 10/100/1000 Mbps Gigabit Ethernet operation:

Vendor	P/N	Package	Temp	Configuration
HanRun	HR911060C	Integrated RJ45	0 - 70° Celsius	HP Auto-MDIX
Halo	HFJ11-1G02E	Integrated RJ45	0 - 70° Celsius	HP Auto-MDIX
UDE	RB1-BA6BT9WA	Integrated RJ45	0 - 70° Celsius	HP Auto-MDIX
Pulse Electronics (Recommended by Atheros)	H5007	24-pin SOIC-W	0 - 70° Celsius	HP Auto-MDIX
Halo	TG1G-S002NZRL	24-pin SOIC-W	-40 - 85° Celsius	HP Auto-MDIX
UDE	RB1-BA6BT9WA	Integrated RJ45	-40 - 85° Celsius	HP Auto-MDIX
Halo	TG1G-E012NZRL	24-pin SOIC-W	-40 - 85° Celsius	HP Auto-MDIX

5.10 GPIOs

This section lists signals related to General Purpose Input/Output (GPIO) functionality.

Many pins have GPIO functionality that can be enabled (via pin multiplexing). All GPIO pins can be used to generate interrupts as well as be wakeup sources.

The *EACOM Board specification* defines only a few GPIOs and they are listed in the table below. The pins that cannot be configured as GPIOs are Ethernet, USB, PCIe, LVDS and Analogue inputs. I2C pins can be GPIOs but are unsuitable since I2C#0 is used on-board and I2C#1 and #2 has 2.2Kohm on-board pullup resistors.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P140/288	GPIO1	SD1_CLK	I/O	GPIO	GPIO1 controlled by alternative pin function GPIO6_IO00
P139/286	GPIO2	SD1_CMD	I/O	GPIO	GPIO2 controlled by alternative pin function GPIO6_IO01
P4/8	GPIO3	SD4_RESET	I/O	GPIO	GPIO3 controlled by alternative pin function GPIO6_IO22
P3/6	GPIO4	KEY_ROW1	I/O	GPIO	GPIO4 controlled by alternative pin function GPIO2_IO16
P2/4	GPIO5	KEY_COL2	I/O	GPIO	GPIO5 controlled by alternative pin function GPIO2_IO12
P1/2	GPIO6	KEY_ROW3	I/O	GPIO	GPIO6 controlled by alternative pin function GPIO2_IO18
S84/173	GPIO7	LCD1_RESET	I/O	GPIO	GPIO7 controlled by alternative pin function GPIO3_IO27

5.11 I2C

This section lists signals related to the Inter-Integrated Circuit (I2C) interface.

The i.MX 6SoloX SoC has four I2C interfaces. Three of these are assigned in the *EACOM Board Specification*. It is recommended not to change this assignment since the pins have 2.2Kohm pullup resistors. Pin assignment for I2C channel A cannot be changed since this channel is used on the i.MX 6SoloX COM board (for PMIC and E2PROM communication).

The table below lists the pin assignment as well as alternative pin locations.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S47/93	I2C-A_SCL	GPIO1_IO00	I/O	Clock signal of I2C channel A	Signal has on-board 2.2Kohm pullup resistor. Signal is connected to on-board I2C channel to PMIC and E2PROM.
S46/91	I2C-A_SDA	GPIO1_IO01	I/O	Data signal of I2C channel A	Signal has on-board 2.2Kohm pullup resistor. Signal is connected to on-board I2C channel to PMIC and E2PROM.

S49/97	I2C-B_SCL	GPIO1_IO02	I/O	Clock signal of I2C channel B	Signal has on-board 2.2Kohm pullup resistor.
S48/95	I2C-B_SDA	GPIO1_IO03	I/O	Data signal of I2C channel B	Signal has on-board 2.2Kohm pullup resistor.
S51/101	I2C-C_SCL	KEY_COL4	I/O	Clock signal of I2C channel C	Signal has on-board 2.2Kohm pullup resistor.
S50/99	I2C-C_SDA	KEY_ROW4	I/O	Data signal of I2C channel C	Signal has on-board 2.2Kohm pullup resistor.
S125/255	CSI_D6	CSI_DATA06	I/O	Clock signal of I2C channel #4	I2C4_SCL, signal will require a pullup resistor on carrier board.
S126/257	CSI_D7	CSI_DATA07	I/O	Data signal of I2C channel #4	I2C4_SDA, signal will require a pullup resistor on carrier board.
P5/10	SD_D1	SD2_DATA1	I/O	Clock signal of I2C channel #4	I2C4_SCL, signal will require a pullup resistor on carrier board.
P6/12	SD_D0	SD2_DATA0	I/O	Data signal of I2C channel #4	I2C4_SDA, signal will require a pullup resistor on carrier board.
P20/40	MMC_D3	SD4_DATA3	I/O	Clock signal of I2C channel #2	I2C2_SCL. Note that this location is not recommended since the EA COM Board specification has allocated this function on another pin (GPIO1_IO00).
P21/42	MMC_D2	SD4_DATA2	I/O	Data signal of I2C channel #2	I2C2_SDA. Note that this location is not recommended since the EA COM Board specification has allocated this function on another pin (GPIO1_IO01).

Note that the following two positions for I2C interfaces are not allowed:

- I2C1_SCL on i.MX 6SoloX pin CSI_DATA00 should not be used. EACOM I2C channel A is allocated on other pins.
- I2C1_SDA on i.MX 6SoloX pin CSI_DATA01 should not be used. EACOM I2C channel A is allocated on other pins.
- I2C4_SCL on i.MX 6SoloX pin USB_H_STROBE cannot be used due to an on-board voltage level translator where the pin is output only.
- I2C4_SDA on i.MX 6SoloX pin USB_H_DATA cannot be used due to an on-board voltage level translator where the pin is output only.

5.12 JTAG

This section lists signals related to the JTAG debug interface.

The i.MX 6SoloX SoC has a module called System JTAG Controller (SJC) that provides a JTAG interface to internal logic, including the two ARM Cortex cores (A9 and M4). The SJC complies with JTAG TAP standards. The i.MX 6SoloX processors use the JTAG port for production, testing, and system debugging.

The JTAG signals are not available on the MXM3 edge connector. Instead the signals are available via a 10 pos FPC connector, see picture below for location and orientation.

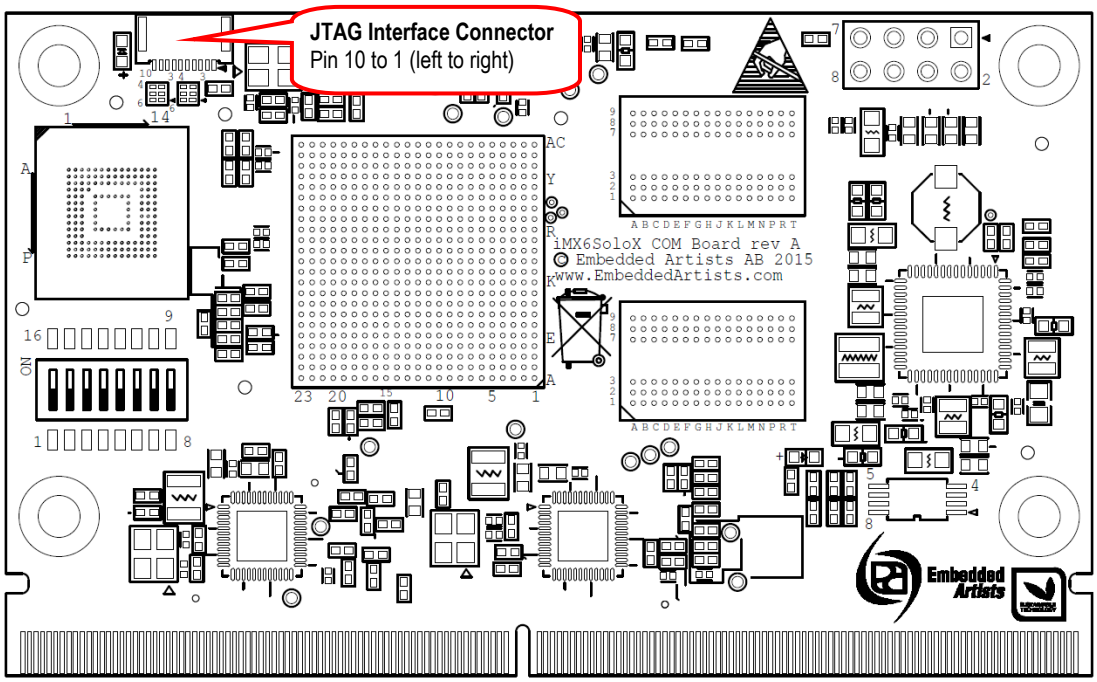


Figure 6 – iMX6 SoloX COM Board, Top Side

The table below lists the 10 signals on the JTAG connector.

J1 Pin Number	Connected to iMX6SoloX Ball Name	I/O	Description	Remarks
1	NVCC_JTAG	O	Logic level supply voltage	Used by external debugger to detect logic level to use for signaling. Typically 3.1V.
2	JTAG_TMS	I	JTAG signal TMS	
3			Ground	
4	JTAG_TCK	I	JTAG signal TCK	
5			Ground	
6	JTAG_TDO	O	JTAG signal TDO	
7	JTAG_MOD	I		Signal shall always be connected to ground. Signal has a 1Kohm pulldown resistor and can be left floating.
8	JTAG_TDI	I	JTAG signal TDI	
9	JTAG_TRST	I	JTAG signal TRST	Signal has a 10Kohm pullup resistor.
10	JTAG_SRST	I	System reset	Signal is active low and controls internal system, reset via buffer. Signal has a 10K ohm pullup resistor.

The *iMX6 SoloX Developer's Kit* contains an adapter board for connection to common debug connectors. The 10 pos connector is Molex 512811094 and has 0.5 mm (20 mil) pitch. FPC length should be kept less than 7 cm.

5.13 Matrix Keypad

This section lists signals related to the Matrix Keypad interface.

The i.MX 6SoloX SoC has a Key Pad Port (KPP) that can control a keyboard in an up to 8x8 matrix.

There are no specific matrix keypad pins defined in the *EACOM Board specification*. KPP pins are only available as alternative functions on certain pins. The table below lists the available pins.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P2/4	GPIO5	KEY_COL2	O	Keyboard matrix column 2	
P129/266	UART-C_TXD	KEY_COL3	O	Keyboard matrix column 3	
P7/14	SD_CLK	SD2_CLK	O	Keyboard matrix column 5	Alternative function is KEY_COL5
S121/247	CSI_D2	CSI_DATA02	O	Keyboard matrix column 5	Alternative function is KEY_COL5
P9/18	SD_D3	SD2_DATA3	O	Keyboard matrix column 6	Alternative function is KEY_COL6
S123/251	CSI_D4	CSI_DATA04	O	Keyboard matrix column 6	Alternative function is KEY_COL6
P5/10	SD_D1	SD2_DATA1	O	Keyboard matrix column 7	Alternative function is KEY_COL7
S125/255	CSI_D6	CSI_DATA06	O	Keyboard matrix column 7	Alternative function is KEY_COL7
S53/105	TP_IRQ	KEY_ROW0	I	Keyboard matrix row 0	
P3/6	GPIO4	KEY_ROW1	I	Keyboard matrix row 1	
P1/2	GPIO6	KEY_ROW2	I	Keyboard matrix row 2	
P128/264	UART-C_RXD	KEY_ROW3	I	Keyboard matrix row 3	
P8/16	SD_CMD	SD2_CMD	I	Keyboard matrix row 5	Alternative function is KEY_ROW5
S122/249	CSI_D3	CSI_DATA03	I	Keyboard matrix row 5	Alternative function is KEY_ROW5
P10/20	SD_D2	SD2_DATA2	I	Keyboard matrix row 6	Alternative function is KEY_ROW6
S124/253	CSI_D5	CSI_DATA05	I	Keyboard matrix row 6	Alternative function is KEY_ROW6
P13/26	SD_D0	SD2_DATA0	I	Keyboard matrix row 7	Alternative function is KEY_ROW7
S126/257	CSI_D7	CSI_DATA07	I	Keyboard matrix row 7	Alternative function is KEY_ROW7

The following KPP pins are not available due to allocation for on-board functionality;

- KEY_COL0 is used on-board by eMMC interface during booting.
- KEY_COL1 is used on-board by eMMC interface.
- KEY_COL4 is part of EACOM I2C-C (SCL) interface and has a 2.2Kohm pullup resistor.
- KEY_ROW4 is part of EACOM I2C-C (SDA) interface and has a 2.2Kohm pullup resistor.

5.14 PCI Express

This section lists signals related to the PCI Express interface.

The i.MX 6SoloX SoC has a single lane PCI Express (PCIe) interface. The interface is compliant with the PCIe 2.0 specification that supports 5Gbit/s data rate. PCIe 2.0 is backward compatible with the PCIe 1.1 standard that supports 2.5Gbit/s data rate.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S150/305	PCIE_CLK_P	CCM_CLK1_P	O	100 MHz reference clock, positive signal in differential pair	
S151/307	PCIE_CLK_N	CCM_CLK1_N	O	100 MHz reference clock, negative signal in differential pair	
S153/311	PCIE_TX_P	PCIE_TX_P	O	Transmit data, positive signal in differential pair	
S154/313	PCIE_TX_N	PCIE_TX_N	O	Transmit data, negative signal in differential pair	
S156/317	PCIE_RX_P	PCIE_RX_P	I	Receive data, positive signal in differential pair	
S157/319	PCIE_RX_N	PCIE_RX_N	I	Receive data, negative signal in differential pair	

A typical PCIe interface also has a USB Host, a I2C interface and (typically) three control signals; wakeup (input to iMX6), disable and reset (outputs from iMX6). These interfaces and control signals are not specifically defined in the *EACOM Board specification* and is up to each carrier board design to assign/allocate.

5.15 Parallel Camera Interface

This section lists signals related to CMOS Sensor Interface (CSI) functions.

The i.MX 6SoloX SoC has two CSI interfaces that allows direct connection to CMOS image sensors, or cameras for short. The interfaces provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/26-bit Bayer (also called "raw") data input.

Note that CSI2 is not available on the iMX 6SoloX COM board. CSI2 pins are allocated for the dual on-board Ethernet interfaces instead.

The *EACOM Board specification* defines an 8-bit parallel camera interface. Note the difference in pin numbering and internal data bus numbering. The table below lists the pin assignment according to *EACOM Board specification*.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S116/237	CSI_MCLK	CSI_MCLK	O	CMOS Sensor Master Clock	
S117/239	CSI_PIXCLK	CSI_PIXCLK	I	Pixel Clock	
S114/233	CSI_HSYNC	CSI_HSYNC	I	Horizontal Sync	
S115/235	CSI_VSYNC	CSI_VSYNC	I	Vertical Sync (Start Of Frame)	
S119/243	CSI_D0	CSI_DATA00	I	Data Sensor Signal	Signal called CSI1_DATA02 internally.
S120/245	CSI_D1	CSI_DATA01	I	Data Sensor Signal	Signal called CSI1_DATA03 internally.
S121/247	CSI_D2	CSI_DATA02	I	Data Sensor Signal	Signal called CSI1_DATA04 internally.

S122/249	CSI_D3	CSI_DATA03	I	Data Sensor Signal	Signal called CSI1_DATA05 internally.
S123/251	CSI_D4	CSI_DATA04	I	Data Sensor Signal	Signal called CSI1_DATA06 internally.
S124/253	CSI_D5	CSI_DATA05	I	Data Sensor Signal	Signal called CSI1_DATA07 internally.
S125/255	CSI_D6	CSI_DATA06	I	Data Sensor Signal	Signal called CSI1_DATA08 internally.
S126/257	CSI_D7	CSI_DATA07	I	Data Sensor Signal	Signal called CSI1_DATA09 internally.

The table below lists these the alternative pin locations are.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S59/117	LCD_DATA17	LCD1_DATA17	I	Data Sensor Signal	Alternative location for CSI1_DATA00
P123/254	SPI-A_SSEL	QSPI1A_SS0_B	I	Data Sensor Signal	Alternative location for CSI1_DATA00
S58/115	LCD_DATA16	LCD1_DATA16	I	Data Sensor Signal	Alternative location for CSI1_DATA01
P126/260	SPI-A_SCLK	QSPI1A_SCLK	I	Data Sensor Signal	Alternative location for CSI1_DATA01
S73/145	LCD_DATA15	LCD1_DATA15	I	Data Sensor Signal	Alternative location for CSI1_DATA02
S72/143	LCD_DATA14	LCD1_DATA14	I	Data Sensor Signal	Alternative location for CSI1_DATA03
S71/141	LCD_DATA13	LCD1_DATA13	I	Data Sensor Signal	Alternative location for CSI1_DATA04
S70/139	LCD_DATA12	LCD1_DATA12	I	Data Sensor Signal	Alternative location for CSI1_DATA05
S69/137	LCD_DATA11	LCD1_DATA11	I	Data Sensor Signal	Alternative location for CSI1_DATA06
S68/135	LCD_DATA10	LCD1_DATA10	I	Data Sensor Signal	Alternative location for CSI1_DATA07
S67/133	LCD_DATA09	LCD1_DATA09	I	Data Sensor Signal	Alternative location for CSI1_DATA08
S66/131	LCD_DATA08	LCD1_DATA08	I	Data Sensor Signal	Alternative location for CSI1_DATA09
S65/129	LCD_DATA23	LCD1_DATA23	I	Data Sensor Signal	Alternative location for CSI1_DATA10
S15/29	CAN1_RX	QSPI1A_SS1_B	I	Data Sensor Signal	Alternative location for CSI1_DATA10
S64/127	LCD_DATA22	LCD1_DATA22	I	Data Sensor Signal	Alternative location for CSI1_DATA11
S52/103	TP_RST	QSPI1A_DATA3	I	Data Sensor Signal	Alternative location for CSI1_DATA11
S63/125	LCD_DATA21	LCD1_DATA21	I	Data Sensor Signal	Alternative location for CSI1_DATA12
P73/146	USB_O1_PWR	QSPI1A_DATA2	I	Data Sensor Signal	Alternative location for CSI1_DATA12
S62/123	LCD_DATA20	LCD1_DATA20	I	Data Sensor Signal	Alternative location for CSI1_DATA13
P125/258	SPI-A_MISO	QSPI1A_DATA1	I	Data Sensor Signal	Alternative location for CSI1_DATA13
S61/121	LCD_DATA19	LCD1_DATA19	I	Data Sensor Signal	Alternative location for CSI1_DATA14
P124/256	SPI-A_MOSI	QSPI1A_DATA0	I	Data Sensor Signal	Alternative location for CSI1_DATA14
S60/119	LCD_DATA18	LCD1_DATA18	I	Data Sensor Signal	Alternative location for CSI1_DATA15
S12/23	CAN2_TX	QSPI1A_DQS	I	Data Sensor Signal	Alternative location for CSI1_DATA15
S83/171	LCD_CLK	LCD1_CLK	I	Data Sensor Signal	Alternative location for CSI1_DATA16
P122/252	SPI-B_SCLK	QSPI1B_SCLK	I	Data Sensor Signal	Alternative location for CSI1_DATA16
S87/179	LCD_ENABLE	LCD1_ENABLE	I	Data Sensor Signal	Alternative location for CSI1_DATA17
P119/246	SPI-B_SSEL	QSPI1B_SS0_B	I	Data Sensor Signal	Alternative location for CSI1_DATA17
S85/175	LCD_HSYNC	LCD1_HSYNC	I	Data Sensor Signal	Alternative location for CSI1_DATA18
S13/25	CAN2_RX	QSPI1B_SS1_B	I	Data Sensor Signal	Alternative location for CSI1_DATA18
S86/177	LCD_VSYNC	LCD1_VSYNC	I	Data Sensor Signal	Alternative location for CSI1_DATA19
S75/149	LCD_DATA00	LCD1_DATA00	I	Data Sensor Signal	Alternative location for CSI1_DATA20
S76/157	LCD_DATA01	LCD1_DATA01	I	Data Sensor Signal	Alternative location for CSI1_DATA21

P121/250	SPI-B_MISO	QSPI1B_DATA1	I	Data Sensor Signal	Alternative location for CSI1_DATA21
S77/159	LCD_DATA02	LCD1_DATA02	I	Data Sensor Signal	Alternative location for CSI1_DATA22
P120/248	SPI-B_MOSI	QSPI1B_DATA0	I	Data Sensor Signal	Alternative location for CSI1_DATA22
S78/161	LCD_DATA03	LCD1_DATA03	I	Data Sensor Signal	Alternative location for CSI1_DATA23
S14/27	CAN1_TX	QSPI1B_DQS	I	Data Sensor Signal	Alternative location for CSI1_DATA23
P66/132	USB_O1_ID	GPIO1_IO10	I	CSI Field Signal	Alternative location for CSI1_FIELD
S80/165	LCD_DATA05	LCD1_DATA05	I	Horizontal Sync	Alternative location for CSI1_HSYNC
P136/280	UART-A_RTS	GPIO1_IO06	O	CMOS Sensor Master Clock	Alternative location for CSI1_MCLK
S82/169	LCD_DATA07	LCD1_DATA07	I	CMOS Sensor Master Clock	Alternative location for CSI1_MCLK
S81/167	LCD_DATA06	LCD1_DATA06	I	Pixel Clock	Alternative location for CSI1_PIXCLK
S79/163	LCD_DATA04	LCD1_DATA04	I	Vertical Sync (Start Of Frame)	Alternative location for CSI1_VSYNC

The CSI can support connection with the sensor as follows.

- To connect with one 8-bit sensor, the sensor data interface should connect to CSI_DATA[9:2]. This is the method that is supported by the *EA COM Board specification*.
- To connect with one 10-bit sensor, the sensor data interface should connect to CSI_DATA[9:0].
- To connect with one 16-bit sensor, the sensor data interface should connect to CSI_DATA[15:0].
- To connect with one 24-bit data, either video pass-through or TV Decoder input, the sensor data interface should connect to CSI_DATA[23:0].

The CSI input data format mapping is shown in the table below.

Internal CSI Signal Name	EACOM Board Name	CCIR656	Generic 10 bit	YCbCr422 2 Cycle	YCbCr422 1 Cycle	RGB565 1 Cycle	RGB666 1 Cycle	RGB888/ YUV4444 3 Cycle	RGB888 1 Cycle	TVdecoder YCbCr 1 Cycle
CSI1_DATA00			Ge0		C0	B0	B4		B0	Cr0
CSI1_DATA01			Ge1		C1	B1	B5		B1	Cr1
CSI1_DATA02	**CSI_D0**	C0/Y0	Ge2	Y0/C0	C2	B2	B0	R0/G0/B0	B2	Cr2
CSI1_DATA03	**CSI_D1**	C1/Y1	Ge3	Y1/C1	C3	B3	B1	R1/G1/B1	B3	Cr3
CSI1_DATA04	**CSI_D2**	C2/Y2	Ge4	Y2/C2	C4	B4	B2	R2/G2/B2	B4	Cr4
CSI1_DATA05	**CSI_D3**	C3/Y3	Ge5	Y3/C3	C5	G0	B3	R3/G3/B3	B5	Cr5
CSI1_DATA06	**CSI_D4**	C4/Y4	Ge6	Y4/C4	C6	G1	B4	R4/G4/B4	B6	Cr6
CSI1_DATA07	**CSI_D5**	C5/Y5	Ge7	Y5/C5	C7	G2	B5	R5/G5/B5	B7	Cr7
CSI1_DATA08	**CSI_D6**	C6/Y6	Ge8	Y6/C6	Y0	G3	G4	R6/G6/B6	G0	Cb0
CSI1_DATA09	**CSI_D7**	C7/Y7	Ge9	Y7/C7	Y1	G4	G5	R7/G7/B7	G1	Cb1
CSI1_DATA10					Y2	G5	G0		G2	Cb2
CSI1_DATA11					Y3	R0	G1		G3	Cb3
CSI1_DATA12					Y4	R1	G2		G4	Cb4
CSI1_DATA13					Y5	R2	G3		G5	Cb5
CSI1_DATA14					Y6	R3	G4		G6	Cb6
CSI1_DATA15					Y7	R4	G5		G7	Cb7
CSI1_DATA16							R4		R0	Y0
CSI1_DATA17							Y5		R1	Y1

CSI1_DATA18	R0	R2	Y2
CSI1_DATA19	R1	R3	Y3
CSI1_DATA20	R2	R4	Y4
CSI1_DATA21	R3	R5	Y5
CSI1_DATA22	R4	R6	Y6
CSI1_DATA23	R5	R7	Y7

5.16 Power Management

This section lists signals related to power management, i.e., reset and external power supplies.

COM Board Pin	EACOM Board Name	I/O	Description	Remarks
P143/294	RESET_OUT	O	Reset output, active low	Open drain output. Driven low during reset. 1.5K pull-up resistor to VIN.
P142/292	RESET_IN	I	Reset input, active low	Pull signal low to activate reset. No need to pull signal high externally. Connected to cathode of series diode, so logic level of driving signal can be anywhere between 1.5-5 V.
P141/290	PERI_PWR_EN	O	Enable signal (active high) for carrier board peripheral power supplies.	Uses pin GPIO4_IO26 on the iMX6SoloX. More information about carrier board design can be found in *EA COM Board specification*.

5.17 Power Supply Signals

This section lists signals related to power supply.

COM Board Pin	EACOM Board Name	I/O	Description	Remarks
P147/302, P148/304, P149/306, P150/308, P151/310, P152/312, P153/314, P154/316, P155/318, P156/320	VIN	A	3.3V supply voltage	See technical specification for details about valid range.
P22/44, P25/50, P31/62, P35/70, P38/76, P46/92, P49/98, P52/104, P60/120, P63/126, P69/138, P77/162, P82/172, P88/184, P91/190, P118/244, P127/262, P144/296, S3/5, S9/17, S16/31, S22/43, S25/49, S28/55, S31/61, S37/73, S40/79, S43/85, S57/113, S74/147, S88/181, S98/201, S101/207, S104/213, S118/241, S127/259, S130/265, S133/271, S136/277, S139/283, S142/289, S145/295, S148/301, S149/303, S152/309, S155/315, S158/321	GND	A	Ground	
P145/298	VBAT	AI/AO	Power supply for MMPF0200 PMIC and iMX6SoloX on-chip RTC. Connect to external primary (= non rechargeable) or secondary (= rechargeable) coin	Connected to MMPF0200 PMIC, pin 42, LICELL. PMIC can be programmed to charge a secondary coin cell.

cell battery.

5.18 PWM

This section lists signals related to Pulse Wide Modulators (PWM).

The i.MX 6SoloX SoC has eight PWM channels that are available via pin multiplexing. The generated signals has 16-bit resolution. PWM signals can be used to generate analogue signals (emulate a DAC) and also control intensity / brightness in display applications.

There are two PWM signals defined in the *EACOM Board specification*. One general PWM signal and one that is intended for backlight intensity control for displays. The latter can however be used as a general PWM signals also if backlight intensity control is not needed or control is arranged differently. The remaining PWM signals are available as alternative functions on certain pins.

The table below lists the pin assignment as well as alternative pin locations.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P138/284	PWM1	USB_H_STROBE	O	PWM1_OUT signal	
S56/111	LCD_BL_CTRL	USB_H_DATA	O	PWM2_OUT signal	
P66/132	USB_O1_ID	GPIO1_IO10	O	PWM1_OUT signal	Available as alternative signal. Note that PWM1_OUT is assigned by the EA COM Board specification to another location.
P6/12	SD_D0	SD2_DATA0	O	PWM1_OUT signal	Available as alternative signal. Note that PWM1_OUT is assigned by the EA COM Board specification to another location.
P76/160	USB_H1_OC	GPIO1_IO11	O	PWM2_OUT signal	Available as alternative signal. Note that PWM2_OUT is assigned by the EA COM Board specification to another location.
P5/10	SD_D1	SD2_DATA1	O	PWM2_OUT signal	Available as alternative signal. Note that PWM2_OUT is assigned by the EA COM Board specification to another location.
P131/270	UART-B_CTS	SD1_DATA2	O	PWM3_OUT signal	Available as alternative signal.
P75/158	USB_H1_PWR	GPIO1_IO12	O	PWM3_OUT signal	Available as alternative signal.
P133/274	UART-B_RXD	SD1_DATA1	O	PWM4_OUT signal	Available as alternative signal.
S65/129	LCD1_DATA23	LCD1_DATA23	O	PWM5_OUT signal	Available as alternative signal.
S123/251	CSI_D4	CSI_DATA04	O	PWM5_OUT signal	Available as alternative signal.
S124/253	CSI_D5	CSI_DATA05	O	PWM6_OUT signal	Available as alternative signal.
S64/127	LCD1_DATA22	LCD1_DATA22	O	PWM6_OUT signal	Available as alternative signal.
S63/125	LCD1_DATA21	LCD1_DATA21	O	PWM7_OUT signal	Available as alternative signal.
S62/123	LCD1_DATA20	LCD1_DATA20	O	PWM8_OUT signal	Available as alternative signal.

5.19 SD/MMC

This section lists signals related to Ultra Secured Digital Host Controller (uSDHC) functions.

The i.MX 6SoloX SoC has 4 uSDHC interfaces. One, uSDHC3, is allocated (on-board) for interface to eMMC Flash. The interfaces are capable of interfacing with SD Memory Cards, SDIO, MMC, CE-ATA cards and eMMC devices. The features of the uSDHC module include the following:

- Conforms to the SD Host Controller Standard Specification version 3.0
- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.41

- Compatible with the SD Memory Card Specification version 3.0 and supports the Extended Capacity SD Memory Card
- Compatible with the SDIO Card Specification version 3.0
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Card bus clock frequency up to 208 MHz
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes

The *EACOM Board specification* defines one 4-databit uSDHC interface (uSDHC2) and one 8-databit uSDHC interface (uSDHC4). The remaining uSDHC signals are available as alternative functions on certain pins.

The table below lists the pin assignment according to *EACOM Board specification*.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P7/14	SD_CLK	SD2_CLK	O	Clock for MMC/SD/SDIO card	
P8/16	SD_CMD	SD2_CMD	I/O	CMD line connect to card	
P6/12	SD_D0	SD2_DATA0	I/O	DATA0 line in all modes. Also used to detect busy status	
P5/10	SD_D1	SD2_DATA1	I/O	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4-bit mode	
P10/20	SD_D2	SD2_DATA2	I/O	DATA2 line or Read Wait in 4-bit mode, Read Wait in 1-bit mode	
P9/18	SD_D3	SD2_DATA3	I/O	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode	
P16/32	MMC_CLK	SD4_CLK	O	Clock for MMC/SD/SDIO card	
P18/36	MMC_CMD	SD4_CMD	I/O	CMD line connect to card	
P13/26	MMC_D0	SD4_DATA0	I/O	DATA0 line in all modes. Also used to detect busy status	
P12/24	MMC_D1	SD4_DATA1	I/O	DATA1 line in 4/8-bit mode Also used to detect interrupt in 1/4-bit mode	
P10/20	MMC_D2	SD4_DATA2	I/O	DATA2 line or Read Wait in 4-bit mode, Read Wait in 1-bit mode	
P20/40	MMC_D3	SD4_DATA3	I/O	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode	
P19/38	MMC_D4	SD4_DATA4	I/O	DATA4 line in 8-bit mode, not used in other modes	
P17/34	MMC_D5	SD4_DATA5	I/O	DATA5 line in 8-bit mode, not used in other modes	
P15/30	MMC_D6	SD4_DATA6	I/O	DATA6 line in 8-bit mode, not used in other modes	
P14/28	MMC_D7	SD4_DATA7	I/O	DATA7 line in 8-bit mode, not used in other modes	

The table below lists of alternative pin locations for uSDHC1 signals. Note that it is not possible to access all data bits so 8-bit mode is not possible to use.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P140/288	GPIO1	SD1_CLK	O	Clock for MMC/SD/SDIO card	Alternative function SD1_CLK.
P139/286	GPIO2	SD1_CMD	I/O	CMD line connect to card	Alternative function SD1_CMD
P130/268	UART-B_RXD	SD1_DATA0	I/O	DATA0 line in all modes. Also used to detect busy status	Alternative function SD1_DATA0
P133/274	UART-B_TXD	SD1_DATA1	I/O	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4-bit mode	Alternative function SD1_DATA1

P131/270	UART-B_CTS	SD1_DATA2	I/O	DATA2 line or Read Wait in 4-bit mode, Read Wait in 1-bit mode	Alternative function SD1_DATA2
P132/272	UART-B_RTS	SD1_DATA3	I/O	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode	Alternative function SD1_DATA3
S49/97	I2C-B_SCL	GPIO1_IO02	I	Card detection pin	Alternative function SD1_CD_B. Note that the pin is pre-allocated as I2C2_SCL and has on-board 2.2Kohm pullup resistor. It is possible to use this pin but not recommended.
S87/179	LCD1_ENABLE	LCD1_ENABLE	I	Card detection pin	Alternative function SD1_CD_B
S50/99	I2C-C_SDA	KEY_ROW4	O	LED control used to drive an external LED Active high	Alternative function SD1_LCTL. Note that the pin is pre-allocated as I2C3_SDA and has on-board 2.2Kohm pullup resistor. It is possible to use this pin but not recommended.
S48/95	I2C-B_SDA	GPIO1_IO03	I	Card write protect detect	Alternative function SD1_WP. Note that the pin is pre-allocated as I2C2_SDA and has on-board 2.2Kohm pullup resistor. It is possible to use this pin but not recommended.
S83/171	LCD1_CLK	LCD1_CLK	I	Card write protect detect	Alternative function SD1_WP

The table below lists of alternative pin locations for uSDHC2 signals.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P136/280	UART-A_RTS	GPIO1_IO06	I	Card detection pin	Alternative function SD2_CD_B
S86/177	LCD1_VSYNC	LCD1_VSYNC	I	Card detection pin	Alternative function SD2_CD_B
S51/101	I2C-C_SCL	KEY_COL4	O	LED control used to drive an external LED Active high	Alternative function SD2_LCTL. Note that the pin is pre-allocated as I2C3_SCL and has on-board 2.2Kohm pullup resistor. It is possible to use this pin but not recommended.
P137/282	UART-A_TXD	GPIO1_IO04	O	Card hardware reset signal, active LOW	Alternative function SD2_RESET_B
P134/276	UART-A_RXD	GPIO1_IO05	O	IO power voltage selection signal	Alternative function SD2_VSELECT
P135/278	UART-A_CTS	GPIO1_IO07	I	Card write protect detect	Alternative function SD2_WP
S85/175	LCD1_HSYNC	LCD1_HSYNC	I	Card write protect detect	Alternative function SD2_WP

There are no accessible pins for uSDHC3 signals since these are connected to the on-board eMMC Flash.

The table below lists of alternative pin locations for uSDHC4 signals.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P2/4	GPIO5	KEY_COL2	I	Card detection pin	Alternative function SD4_CD_B
P14/28	MMC_D7	SD4_DATA7	I	Card detection pin	Alternative function SD4_CD_B
P129/266	UART-C_TXD	KEY_COL3	O	LED control used to drive an external LED Active high	Alternative function SD4_LCTL
P4/8	GPIO3	SD4_RESET_B	O	Card hardware reset signal, both active LOW and HIGH version of the signal exist	Alternative function SD4_RESET_B

P3/6	GPIO4	KEY_ROW1	O	IO power voltage selection signal	Alternative function SD4_VSELECT
P1/2	GPIO6	KEY_ROW2	I	Card write protect detect	Alternative function SD4_WP
P15/30	MMC_D6	SD4_DATA6	I	Card write protect detect	Alternative function SD4_WP

5.20 SPI

This section lists signals related to Enhanced Configurable Serial Peripheral Interface (ECSPI) functions.

The i.MX 6SoloX SoC has 5 ECSPI block that are capable of full-duplex, synchronous, four-wire serial communication. The *EACOM Board specification* defines two 4-signal ECSPI interfaces. The remaining ECSPI signals are available as alternative functions on certain pins.

The table below lists the pin assignment according to *EACOM Board specification*.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P125/258	SPI-A_MISO	QSPI1A_DATA1	I/O	Master data in, slave data out	ECSPI1_MISO
P124/256	SPI-A_MOSI	QSPI1A_DATA0	I/O	Master data out, slave data in	ECSPI1_MOSI
P126/260	SPI-A_SCLK	QSPI1A_SCLK	I/O	SPI clock signal	ECSPI1_SCLK
P123/254	SPI-A_SS0	QSPI1A_SS0_B	I/O	Chip select signal	ECSPI1_SS0
P121/250	SPI-B_MISO	QSPI1B_DATA1	I/O	Master data in, slave data out	ECSPI3_MISO. Note difference in SPI numbering between iMX6SoloX SoC and *EACOM Board specification*.
P120/248	SPI-B_MOSI	QSPI1B_DATA0	I/O	Master data out, slave data in	ECSPI3_MOSI. Note difference in SPI numbering between iMX6SoloX SoC and *EACOM Board specification*.
P122/252	SPI-B_SCLK	QSPI1B_SCLK	I/O	SPI clock signal	ECSPI3_SCLK. Note difference in SPI numbering between iMX6SoloX SoC and *EACOM Board specification*.
P119/246	SPI-B_SS0	QSPI1B_SS0_B	I/O	Chip select signal	ECSPI3_SS0. Note difference in SPI numbering between iMX6SoloX SoC and *EACOM Board specification*.

The table below lists of alternative pin locations for ECSPI1 signals.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S53/105	TP_IRQ	KEY_ROW0	I/O	Master data out, slave data in	ECSPI1_MOSI
P2/4	GPIO5	KEY_COL2	I/O	SPI data ready signal	ECSPI1_RDY
P3/6	GPIO4	KEY_ROW1	I/O	Chip select signal	ECSPI1_SS0
P128/264	UART-C_RXD	KEY_ROW3	I/O	Chip select signal	ECSPI1_SS1
P129/266	UART-C_TXD	KEY_COL3	I/O	Chip select signal	ECSPI1_SS2
P1/2	GPIO6	KEY_ROW2	I/O	Chip select signal	ECSPI1_SS3

There are no accessible pins for ECSPI2 signals due to on-board allocation conflicts.

No additional alternative pins exist for ECSPI3 signals.

The table below lists of alternative pin locations for ECSPI4 signals.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P9/18	SD_D3	SD2_DATA3	I/O	Master data in; slave data out	ECSPI4_MISO
P8/16	SD_CMD	SD2_CMD	I/O	Master data out; slave data in	ECSPI4_MOSI
P21/42	MMC_D2	SD1_DATA2	I/O	SPI data ready signal	ECSPI4_RDY
P7/14	SD_CLK	SD2_CLK	I/O	SPI clock signal	ECSPI4_SCLK
P10/20	SD_D2	SD2_DATA2	I/O	Chip select signal	ECSPI4_SS0
P20/40	MMC_D3	SD1_DATA3	I/O	Chip select signal	ECSPI4_SS1
P5/10	SD_D1	SD2_DATA1	I/O	Chip select signal	ECSPI4_SS2
P6/12	SD_D0	SD2_DATA0	I/O	Chip select signal	ECSPI4_SS3

The table below lists of alternative pin locations for ECSPI5 signals.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P73/146	USB_O1_PWR	QSPI1A_DATA2	I/O	Chip select signal	ECSPI5_SS1
S52/103	TP_RST	QSPI1A_DATA3	I/O	Chip select signal	ECSPI5_SS2

5.21 UART

This section lists signals related to Universal Asynchronous Receiver/Transmitter (UART) functions.

The i.MX 6SoloX SoC has six UARTs, supporting bitrates up to 5Mbps each. The *EACOM Board specification* defines two 4-signal UARTs and one 2-signal UART. The remaining UART signals are available as alternative functions on certain pins.

The table below lists the pin assignment according to *EACOM Board specification*.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P137/282	UART-A_TXD	GPIO1_IO04	O	UART1 Transmit Data	
P134/276	UART-A_RXD	GPIO1_IO05	I	UART1 Receive Data	
P136/280	UART-A_RTS	GPIO1_IO06	O	UART1 Request to Send	
P135/278	UART-A_CTS	GPIO1_IO07	I	UART1 Clear to Send	
P133/274	UART-B_TXD	SD1_DATA1	O	UART2 Transmit Data	
P130/268	UART-B_RXD	SD1_DATA0	I	UART2 Receive Data	
P132/272	UART-B_RTS	SD1_DATA3	O	UART2 Request to Send	
P131/270	UART-B_CTS	SD1_DATA2	I	UART2 Clear to Send	
P129/266	UART-C_TXD	KEY_COL3	O	UART5 Transmit Data	
P128/264	UART-C_RXD	KEY_ROW3	I	UART5 Receive Data	

Note that all eight (modem) signals for UART1 are not available due to conflicting on-board pin assignment. UART6 has however all eight modem signals available (on alternative pins).

The table below lists of alternative pin locations for UART2 signals.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P136/280	UART-A_RTS	GPIO1_IO06	O	UART2 Transmit Data	Alternative function is UART2_TXD.
P135/278	UART-A_CTS	GPIO1_IO07	I	UART2 Receive Data	Alternative function is UART2_RXD.
P74/148	USB_O1_OC	GPIO1_IO08	O	UART2 Request to Send	Alternative function is UART2_RTS_B.
S55/109	LCD_BL_PWR	GPIO1_IO09	I	UART2 Clear to Send	Alternative function is UART2_CTS_B.

The table below lists of alternative pin locations for UART3 signals.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P119/246	SPI-B_SSEL	QSPI1B_SS0_B	O	UART3 Transmit Data	Alternative function is UART3_TXD.
P122/252	SPI-B_SCLK	QSPI1B_SCLK	I	UART3 Receive Data	Alternative function is UART3_RXD.
P121/250	SPI-B_MISO	QSPI1B_DATA1	O	UART3 Request to Send	Alternative function is UART3_RTS_B.
P120/248	SPI-B_MOSI	QSPI1B_DATA0	I	UART3 Clear to Send	Alternative function is UART3_CTS_B.

The table below lists of alternative pin locations for UART4 signals.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S117/239	CSI_PIXCLK	CSI_PIXCLK	O	UART4 Transmit Data	Alternative function is UART4_TXD.
S116/237	CSI_MCLK	CSI_MCLK	I	UART4 Receive Data	Alternative function is UART4_RXD.
S114/233	CSI_HSYNC	CSI_HSYNC	O	UART4 Request to Send	Alternative function is UART4_RTS_B.
S115/235	CSI_VSYNC	CSI_VSYNC	I	UART4 Clear to Send	Alternative function is UART4_CTS_B.
P12/24	SD_D1	SD2_DATA1	O	UART4 Transmit Data	Alternative function is UART4_TXD.
P13/26	SD_D0	SD2_DATA0	I	UART4 Receive Data	Alternative function is UART4_RXD.

The table below lists of alternative pin locations for UART5 signals.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P17/34	MMC_D5	SD4_DATA5	O	UART5 Transmit Data	Alternative function is UART5_TXD.
P19/38	MMC_D4	SD4_DATA4	I	UART5 Receive Data	Alternative function is UART5_RXD.
P15/30	MMC_D6	SD4_DATA6	O	UART5 Request to Send	Alternative function is UART5_RTS_B.
P2/4	GPIO5	KEY_COL2	O	UART5 Request to Send	Alternative function is UART5_RTS_B.
P14/28	MMC_D7	SD4_DATA7	I	UART5 Clear to Send	Alternative function is UART5_CTS_B.
P1/2	GPIO6	KEY_ROW2	I	UART5 Clear to Send	Alternative function is UART5_CTS_B.

The table below lists of alternative pin locations for UART6 signals.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
S124/253	CSI_D5	CSI_DATA05	O	UART6 Transmit Data	Alternative function is UART6_TXD.
P9/18	SD_D3	SD2_DATA3	O	UART6 Transmit Data	Alternative function is UART6_TXD.
S123/251	CSI_D4	CSI_DATA04	I	UART6 Receive Data	Alternative function is UART6_RXD.
P10/20	SD_D2	SD2_DATA2	I	UART6 Receive Data	Alternative function is UART6_RXD.

P3/6	GPIO4	KEY_ROW1	I	UART6 Receive Data	Alternative function is UART6_RXD.
S125/255	CSI_D6	CSI_DATA06	O	UART6 Request to Send	Alternative function is UART6_RTS_B.
S126/257	CSI_D7	CSI_DATA07	I	UART6 Clear to Send	Alternative function is UART6_CTS_B.
S53/105	TP_IRQ	KEY_ROW0	I	UART6 Clear to Send	Alternative function is UART6_CTS_B.
S119/243	CSI_D0	CSI_DATA00	I/O	UART6 Ring Indicator	Alternative function is UART6_RI_B.
S120/245	CSI_D1	CSI_DATA01	I/O	UART6 Data Set Ready	Alternative function is UART6_DSR_B.
S121/247	CSI_D2	CSI_DATA02	I/O	UART6 Data Terminal Ready	Alternative function is UART6_DTR_B.
S122/249	CSI_D3	CSI_DATA03	I/O	UART6 Data Carrier Detect	Alternative function is UART6_DCD_B.

5.22 USB

This section lists signals related to the USB interfaces.

The *EACOM Board specification* has one USB 3.0 OTG port, one USB 3.0 Host port and one USB 2.0 Host port. The iMX6SoloX has two USB 2.0 OTG ports and USB 3.0 is backward compatible with USB 2.0. The pins that are specific for USB 3.0 are just left unconnected and are for future upgrade.

The carrier board must provide a +5V supply (with enable and over-current functionality) for USB Host interfaces.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P64/128	USB_O1_DN	USB_OTG1_DN	I/O	Negative Differential USB Signal, OTG compatible	
P65/130	USB_O1_DP	USB_OTG1_DP	I/O	Positive Differential USB Signal, OTG compatible	
P66/132	USB_O1_ID	GPIO1_IO10	I	USB OTG ID pin	
P67/134	USB_O1_SSTXN			Not connected	
P68/136	USB_O1_SSTXP			Not connected	
P70/140	USB_O1_SSRXN			Not connected	
P71/142	USB_O1_SSRXP			Not connected	
P72/144	USB_O1_VBUS	USB_OTG1_VBUS	I	+5V USB VBUS detect input	This pin is +5V tolerant.
P73/146	USB_O1_PWR_EN	QSPI1A_DATA2	O	Enable external USB voltage supply. Active high output.	
P74/148	USB_O1_OC	GPIO1_IO08	I	Signals an over-current condition on the USB voltage supply. Active low input.	
P75/158	USB_H1_PWR_EN	GPIO1_IO12	O	Enable external USB voltage supply. Active high output.	
P76/160	USB_H1_OC	GPIO1_IO11	I	Signals an over-current condition on the USB voltage supply. Active low input.	
P78/164	USB_H1_DN	USB_OTG2_DN	I/O	Negative Differential USB Signal	
P79/166	USB_H1_DP	USB_OTG2_DP	I/O	Positive Differential USB Signal	
P80/168	USB_H1_SSTXN			Not connected	
P81/170	USB_H1_SSTXP			Not connected	
P83/174	USB_H1_SSRXN			Not connected	
P84/176	USB_H1_SSRXP			Not connected	
P85/178	USB_H1_VBUS	USB_OTG2_VBUS	I	+5V USB VBUS detect input	This pin is +5V tolerant.

The table below lists of alternative pin locations for USB signals.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P125/258	SPI-A_MISO	QSPI1A_DATA1	I	USB OTG1 ID	
S52/103	TP_RST	QSPI1A_DATA3	I	USB OTG1 OC	Signals an over-current condition on the USB voltage supply. Active low input.
S55/109	BL_PWR_EN	GPIO1_IO09	O	USB OTG1 PWR EN	Enable external USB voltage supply. Active high output.
P126/260	SPI-A_CLK	QSPI1A_SCLK	I	USB OTG2 ID	
P124/256	SPI-A_MOSI	QSPI1A_DATA0	I	USB OTG2 OC	Signals an over-current condition on the USB voltage supply. Active low input.
P123/254	SPI-A_SSEL	QSPI1A_SS0_B	O	USB OTG2 PWR EN	Enable external USB voltage supply. Active high output.

Note that EACOM USB Host port#2 is not connected to a USB port on the i.MX 6SoloX. Some other signals are connected to these pins in a non-standard way, see table below.

COM Board Pin	EACOM Board Name	iMX6SoloX Ball Name	I/O	Description	Remarks
P86/180	USB_H2_PWR_EN	SNVS_TAMPER signal, iMX6SoloX ball V14		Not connected for USB functionality	
P87/182	USB_H2_OC	ONOFF signal, iMX6SoloX ball W17		Not connected for USB functionality	
P89/186	USB_H2_DN	KEY_COL0 signal, iMX6SoloX ball C23, During boot from eMMC, this pin carry signal SD3_CD_B. The signal has a 10K pulldown resistor to ground.		Not connected for USB functionality	Signal can be used if it does not interfere with booting (not driving the signal high before eMMC boot is complete).
P90/188	USB_H2_DP	CCM_CLK2 signal, iMX6SoloX ball W18		Not connected for USB functionality	

6 Boot Options

This chapter presents the different boot settings that the iMX6 SoloX COM Board supports. This chapter will only present how the different options are controlled. Other documents discuss the pros and cons with different options and what general system architectures (with different booting phases) that are suitable in different situations.

The iMX6 SoloX COM Board supports booting (i.e., from where the i.MX 6SoloX SoC starts downloading code to start executing from) from different sources:

- On-board eMMC Flash (signal E2PROM_WP high/floating - default)
- USB OTG download (also called 'serial download'), (signal E2PROM_WP low)
- Other sources, like QSPI and external SD/MMC memory cards.
  Note that the OTP fuses must be programmed to set these sources, see below.

Signal E2PROM_WP controls the booting source. If signal E2PROM_WP is high/floating, which is the default, booting takes place from eMMC. If Signal EPROM_WP is low, the i.MX 6SoloX SoC boots into USB OTG mode. This latter mode it typically only used during production when the program images shall be downloaded the first time.

There are three main boot **modes** that controls which boot **source** to use.

- Boot according to on-board configuration pull-up/pull-down resistors
  - eMMC is set as default boot source.
  - On rev A boards, it is possible to select other boot sources via a slider switch.
    On rev B boards (and further), boot source is fixed to eMMC.
  - **Note that signals LCD1_DATA00 - LCD1_DATA16 (EACOM pins LCD_B0-B7, LCD_G0-G7) must not be driven externally**. This is normally not a problem since these signals are typically used for a parallel RGB display output. There are often driving buffers between these pins and an external display.
    The reason why the pins must not be driven externally is that on-board resistors pull these signals high/low to select eMMC booting. Driving any of these signals can change this default behavior.
    If any of the signals are driven externally the on-chip OTP fuses must be programmed to force eMMC booting instead.
- Boot according to how internal (i.MX 6SoloX on-chip) OTP fuses have been programmed
  - Any boot mode supported by the i.MX 6SoloX SoC and the hardware connected to it can be selected. See i.MX 6SoloX Reference Manual for details about available sources and OTP fuse settings.
  - Note that OTP fuse BT_FUSE_SEL must be set to 1 in order to override the default setting to boot from eMMC and to have OTP fuse settings controlling boot source instead.
  - Note that the **iMX6 SoloX COM Boards have not programmed the on-chip OTP fuses**. Users have full control over these. This mode can only be used after having programmed the OTP fuses.
  - Programming OTP fuses is a critical operation. If wrong fuses are programmed boards will likely become unusable and there is no recovery.
- Boot from USB OTG interface

- This mode is used in production to download the first stage bootloader and is typically not used by iMX6 SoloX COM Board integrators. Sometimes this mode is called "Recovery mode".
- This mode is activated by pulling signal E2PROM_WP low. Note that this does not apply for rev A boards.

To summarize, the iMX6 SoloX COM board is setup to boot from eMMC as default. If another source is needed, program the OTP fuses.

If using the default setup (boot from eMMC), make sure the boot control pins (LCD1_DATA00 - LCD1_DATA16, which are the EACOM pins LCD_B0-B7, LCD_G0-G7) are not driven externally.

An optional USB OTG boot mode can be enables by pulling signal E2PROM_WP low.

6.1 iMX6 SoloX COM Board, rev A, Boot Control Differences

While revision B of the iMX6 SoloX COM Board has fixed booting from eMMC (or USB OTG, if signal E2PROM_WP is pulled low) , revision A boards have an 8-pos slider switch to select between more boot source (than eMMC and USB OTG).

Note that on rev A boards, signal E2PROM_WP does not control selected boot mode. Only the slider switch controls it.

The picture below illustrates the location of the slider switch.

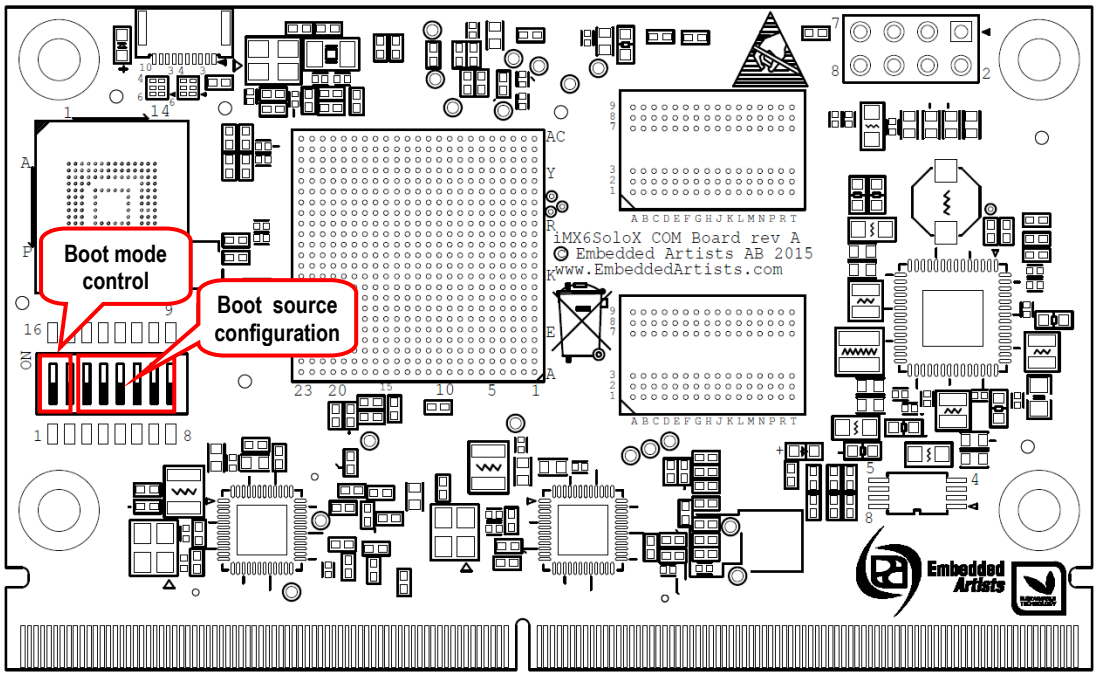
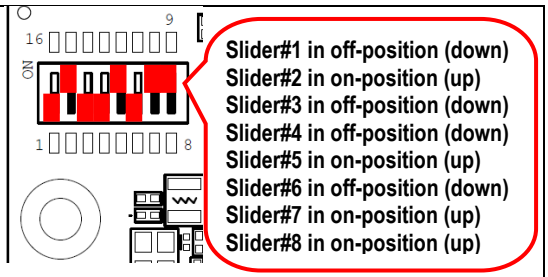
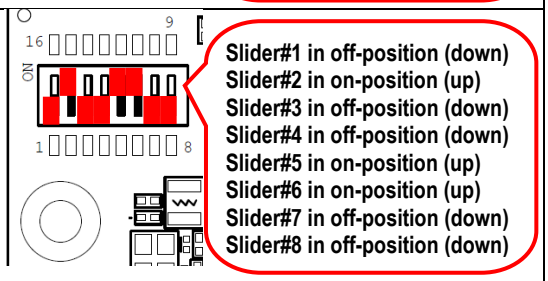
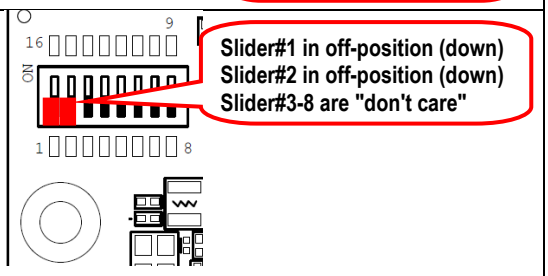
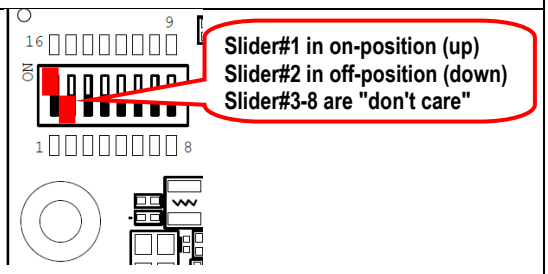


Figure 7 – iMX6 SoloX COM Board Rev A Boot Control Slider Switches Location

The table below presents how to set the slider switches for different boot modes and boot sources.

Boot Modes	Slider Settings
Boot according to slider switches - eMMC Flash Note that if OTP fuse BT_FUSE_SEL = 1 then the system will boot according to OTP fuses, i.e., it overrides this setting.	
Boot according to slider switches - QSPI Flash Note that if OTP fuse BT_FUSE_SEL = 1 then the system will boot according to OTP fuses, i.e., it overrides this setting.	
Boot according to OTP fuses Note that OTP fuses must be programmed first, including setting BT_FUSE_SEL = 1. If not (i.e. OTP fuse BT_FUSE_SEL = 0), the system will boot from USB OTG (Serial load).	
Boot via USB OTG	

7 Technical Specification

7.1 Absolute Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Stress above these limits may cause malfunction or permanent damage to the board.

Symbol	Description	Min	Max	Unit
VIN	Main input supply voltage	-0.3	3.6	V
VBAT	Coin cell voltage	-0.3	3.6	V
VIO	Vin/Vout (I/O VDD + 0.3)	-0.5	3.4	V
VADCIN	Analog input voltage on ADC inputs	-0.3	3.4	V
USB_xx_VBUS	USB VBUS signals	-0.3	5.25	V
USB_xx_DP/DN	USB data signal pairs	-0.3	3.63	V

7.2 Recommended Operating Conditions

All voltages are with respect to ground, unless otherwise noted.

Symbol	Description	Min	Typical	Max	Unit
VIN	Main input supply voltage Ripple with frequency content < 10 MHz Ripple with frequency content ≥ 10 MHz	3.2	3.3	3.4 50 10	V mV mV
VBAT	Coin cell voltage **Note:** This voltage must remain valid at all times for correct operation of the board (including, but not limited to the RTC). **Note:** if the backup battery is rechargeable, the board provides a backup battery charger function.	2.8	3.3	3.6	V
USB_xx_VBUS	USB VBUS signals	4.4	5	5.25	V

7.3 Power Ramp-Up Time Requirements

Input supply voltages (VIN and VBAT) shall have smooth and continuous ramp from 10% to 90% of final set-point. Input supply voltages shall reach recommended operating range in 1-20 ms.

7.4 Electrical Characteristics

For DC electrical characteristics, see iMX6SoloX Datasheet. Depending on internal VDD operating point, OVDD is either 3.25V (50 mV under typical recommended VIN, 3.3V) or 3.1V. In the latter case, the on-board PMIC (MMPF0200) regulates VIN to 3.1V.

7.4.1 Reset Output Voltage Range

The reset output is an open drain output with a 1500 ohm pull-up resistor to VIN.

7.4.2 Reset Input

The reset input is triggered by pulling the reset input low (0.2 V max) for 20 uS minimum. The internal reset pulse will be 140-280 mS long, before the i.MX 6SoloX SoC boot process starts.

7.4.3 ADC_VREFH

ADC_VREFH in an output that specific the upper reference voltage for the ADC inputs. Note that the voltage is not fixed, but rather follows VIN - TBD mV.

7.5 Power Consumption

There are several factors that determine power consumption of the *iMX6 SoloX COM Board*, like input voltage, operating temperature, DDR3 activity, operating frequencies for the different cores, DVFS levels and software executed (i.e., Linux distribution).

The values presented are typical values and should be regarded as an estimate. Always measure current consumption in the real system to get a more accurate estimate.

Symbol	Description (VIN = 3.3V, Toperating = 25°C)	Typical	Max Observed	Unit
I_{VIN}_MAX	Maximum CPU load, 996MHz ARM frequency, without Ethernet		550	mA
I_{VIN}_IDLE	System idle state, uBoot prompt Linux prompt, without Ethernet Linux prompt, with Ethernet		261 170 300	mA
I_{VIN}_DSM	Deep-Sleep mode (DSM), aka "Dormant mode" or "Suspend-to-RAM" in Linux BSP	37		mA
I_{VIN}_STB	Linux standby	64		mA
I_{VBAT}_BACKUP	Current consumption to keep internal RTC running	TBD		uA
I_{VIN}_A7ACT	Android 7 Desktop active	250	626	mA
I_{VIN}_A7OFF	Android 7 Display off	37		mA

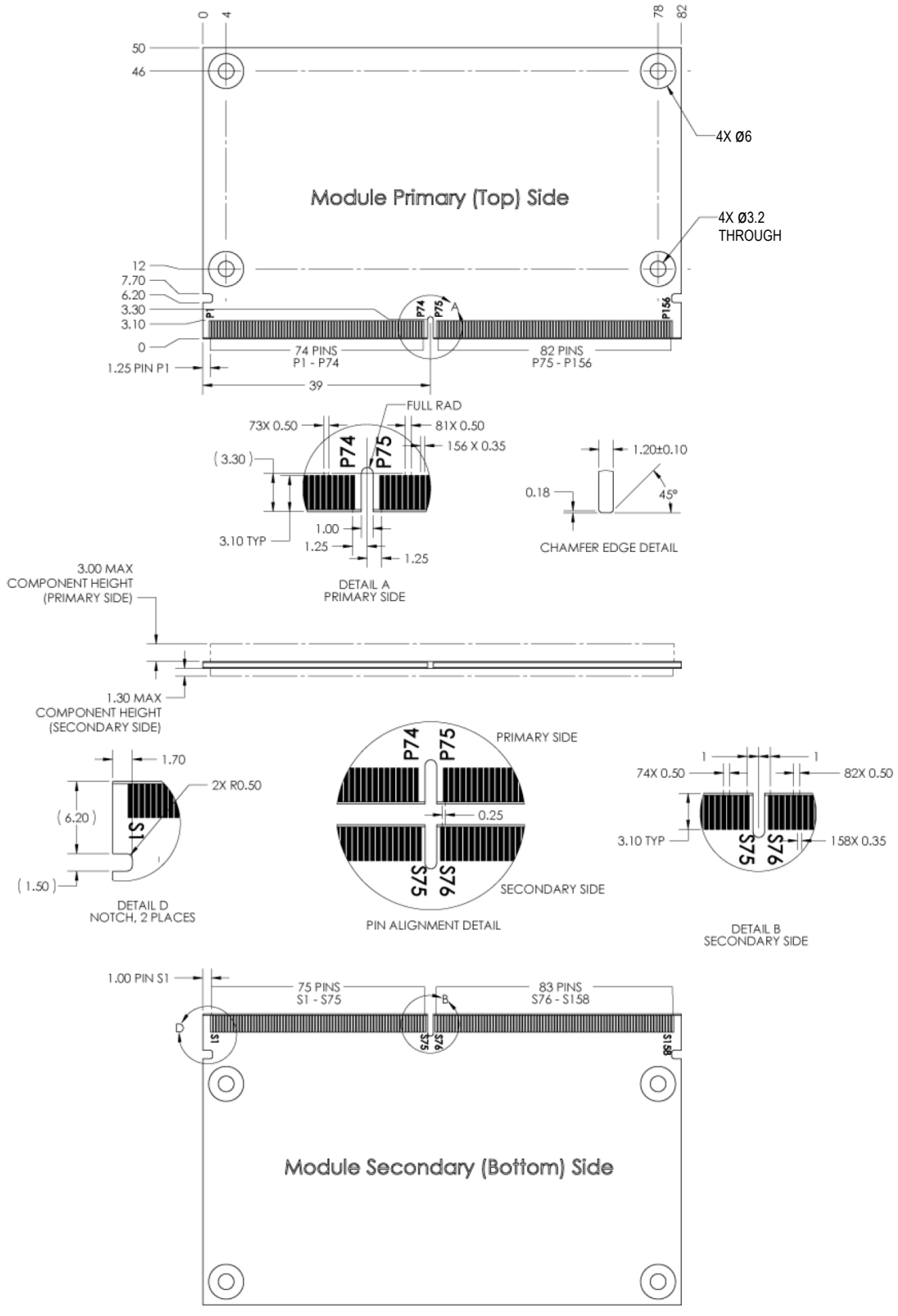
7.6 Mechanical Dimensions

The board use the SMARC mechanical form factor.

Dimension	Value (±0.1 mm)	Unit
Module width	82	mm
Module height	50	mm
Module top side height	3.0	mm
Module bottom side height	1.3	mm
PCB thickness	1.2	mm
Mounting hole diameter **Note:** This measurement is not identical with SMARC specification.	3.2	mm

Module weight	16 ±1 gram	gram

The picture below show the mechanical details of the 82 x 50 mm module, including the pin numbering and edge finger pattern. The picture comes from the SMARC HW specification and show pin numbering in the Px and Sx format.



Picture source: SMARC HW Specification V1.1 © 2014 SGeT e.V.

Figure 8 – iMX6SoloX COM Board Mechanical Outline

7.6.1 MXM3 Socket

The board has 314 edge fingers that mates with an MXM3 connection, which is a low profile 314 pos 0.5mm pitch right angle connector on the carrier board. This connector is available from different manufacturers in different board to board stacking heights, starting from 1.5 mm.

The AS0B821 and AS0B826 connector families from Foxconn are recommended.

Note that connector series MM70 (e.g., MM70-314-310B1) from JAE cannot be used since this specific connector lack some of the pins.

Embedded Artists use connector AS0B826-S78B from Foxconn on the COM Carrier board. This connector gives a board to board stacking height of 5.0 mm. This space allows some components to also be placed right under the COM board.

Always check available component height before placing components on the carrier board under the COM board, see picture below.

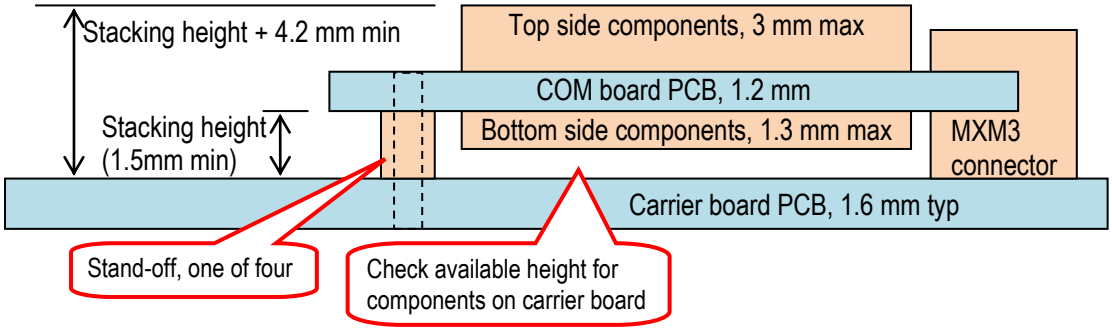


Figure 9 – COM Board Mounting in MXM3 Connector, Stacking Height

7.6.2 Module Assembly Hardware

The carrier board shall have four M3 threaded stand-offs for securing the COM board to the MXM3 connector and carrier board. Penn Engineering and Manufacturing (PEM, http://www.pemnet.com) makes surface mount spacers with M3 internal threads. Their product line is called "SMTSO". 5 mm height is standard so for simplicity select an MXM3 connector with 5 mm stacking height.

6-8 mm M3 screws are typically used.

7.7 Environmental Specification

7.7.1 Operating Temperature

Ambient temperature (T_A)

Parameter		Min	Max	Unit
Operating temperature range	commercial temperature range industrial temperature range	0 -40	70[1] 85[1]	°C °C
Storage temperature range		-40	85	°C

Junction temperature iMX6SoloX SoC, operating	0	105	°C

[1] Depends on cooling solution.

7.7.2 Relative Humidity (RH)

Parameter	Min	Max	Unit
Operating: 0°C ≤ T_A ≤ 60°C, non-condensing	10	90	%
Non-operating/Storage: -40°C ≤ T_A ≤ 85°C, non-condensing	5	90	%

7.8 Thermal Design Considerations

Heat dissipation from the i.MX 6SoloX SoC depending on many operating conditions, like operating frequency, operating voltage, activity type, activity cycle duration and duty cycle. Dissipated heat is in the region of 1.2 Watt max. DDR3L memories can account for another 0.3 Watt, also increasing ambient temperature.

If external cooling is needed, or not, depends on dissipated heat and ambient temperature range. In many cases it is possible to operate the iMX6 SoloX COM board without external cooling, at least with ambient temperature up to +50° Celsius. Above this, care must be taken not to exceed max junction temperature of the i.MX 6SoloX.

The i.MX 6SoloX SoC and PMIC (MMPF0200) together implement DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling. This enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature. In general this result in higher performance at lower average power consumption.

The .iMX 6SoloX SoC has an integrated temperature sensor for monitoring the junction (i.e., die) temperature, which affect several factors:

- A lower junction temperature, Tj, will result in longer SoC lifetime. See the following document for details: AN5062 i.MX 6SoloX Product Lifetime Usage Estimates.
- A lower die temperature will result in lower power consumption due to lower leakage current.

7.8.1 Thermal Management

Embedded Artists provides a general heat spreader solution for EACOM boards. Note that a heat spreader is not a complete thermal solution. It provides a standardized surface for mounting a heat sink or for transporting heat to the housing.

The cooling solution must maintain an ambient air and heat spreader temperature of 60° Celsius, or less.

7.8.2 Thermal Parameters

The i.MX 6SoloX SoC thermal parameters are listed in the table below.

Parameter	Typical	Unit
Thermal Resistance, CPU Junction to ambient ($R_{\theta JA}$)	28	°C/W
Thermal Resistance, CPU Junction to case ($R_{\theta JC}$)	7.8	°C/W
Thermal Resistance, CPU case to heat spreader far surface (θcs)	0.2	°C/W

7.9 Product Compliance

Visit Embedded Artists' website at http://www.embeddedartists.com/product_compliance for up to date information about product compliances such as CE, RoHS2, Conflict Minerals, REACH, etc.

8 Functional Verification and RMA

There is a separate document that presents a number of functional tests that can be performed on the iMX6 SoloX COM Board to verify correct operation on the different interfaces. Note that these tests must be performed on the carrier board that is supplied with the *iMX6 SoloX Developer's Kit* and with a precompiled kernel from Embedded Artists.

The tests can also be done to troubleshoot a board that does not seem to operate properly. It is strongly advised to read through the list of tests and actions that can be done before contacting Embedded Artists. The different tests can help determine if there is a problem with the board, or not. For return policy, please read Embedded Artists' General Terms and Conditions document (http://www.embeddedartists.com/sites/default/files/docs/General_Terms_and_Conditions.pdf).

9 Things to Note

This chapter presents a number of issues and considerations that users must note.

9.1 Shared Pins and Multiplexing

The i.MX6 SoloX SoC has multiple on-chip interfaces that are multiplexed on the external pins. It is not possible to use all interfaces simultaneously and some interface usage is prohibited by the i.MX 6SoloX on-board design. Check if the needed interfaces are available to allocation before starting a design. See section 3.2 and chapter 5 for details.

9.2 Only Use EA Board Support Package (BSP)

The iMX6 SoloX COM board use multiple on-board interfaces for the internal design, for example PMIC, eMMC, QSPI, Ethernet and watchdog. Only use the BSP that is delivered from Embedded Artists. Do not change interface initialization and/or pin assignment for the on-board interfaces. Changing BSP settings can result in permanent board failure.

Note that Embedded Artists does not replace iMX6 SoloX COM Boards because of improper interface initialization and/or improper pin assignment.

9.3 OTP Fuse Programming

The i.MX 6SoloX SoC has on-chip OTP fuses that can be programmed, see NXP documents *iMX 6SoloX Datasheet* and *iMX 6SoloX Reference Manual* for details. Once programmed, there is no possibility to reprogram them.

iMX6 SoloX COM Boards are delivered without any OTP fuse programming. It is completely up to the COM board user to decide if OTP fuses shall be programmed and in that case, which ones.

Note that Embedded Artists does not replace iMX6 SoloX COM Boards because of wrong OTP programming. It's the user's responsibility to be absolutely certain before OTP programming and not to program the fuses by accident.

9.4 Write Protect on Parameter Storage E2PROM

The parameter storage E2PROM contains important system data like DDR memory calibration settings and Ethernet MAC addresses. The content should not be erased or overwritten. The E2PROM is write protected if signal E2PROM_WR (pin P146/300) is left unconnected, i.e. floating. This should always be the case.

Note that all carrier board design should include the possibility to ground this pin.

On rev B boards, the signal E2PROM_WR has dual functions. By pulling the signal low, the i.MX 6SoloX SoC will boot into USB OTG boot mode (also called 'serial download').

9.5 Integration - Contact Embedded Artists

It is strongly recommended to contact Embedded Artists at an early stage in your project. A wide range of support during evaluation and the design-in phase are offered, including but not limited to:

- Developer's Kit to simplify evaluation
- Custom Carrier board design, including 'ready-to-go' standard carrier boards

- Display solutions
- Mechanical solutions
- Schematic review of customer carrier board designs
- Driver and application development

The *iMX6 SoloX COM Board* targets a wide range of applications, such as:

- Industrial controllers and HMI systems
- Home automation and facility management
- Audiovisual equipment
- Instrumentation and measuring equipment
- Vending machines
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- HMI/GUI solutions
- Smart Toll Systems
- Connected vending machines
- Digital signage
- Point-of-Sale (POS) applications
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- Portable systems
- ...and much more

For more harsh use and environments, and where fail-safe operation, redundancy or other strict reliability or safety requirements exists, always contact Embedded Artists for a discussion about suitability.

There are application areas that the *iMX6 SoloX COM Board* is not designed for (and such usage is strictly prohibited), for example:

- Military equipment
- Aerospace equipment
- Control equipment for nuclear power industry
- Medical equipment related to life support, etc.
- Gasoline stations and oil refineries

If not before, **it is essential to contact Embedded Artists before production begins**. In order to ensure a reliable supply for you, as a customer, we need to know your production volume estimates and forecasts. Embedded Artists can typically provide smaller volumes of the *iMX6 SoloX COM Board* directly from stock (for evaluation and prototyping), but **larger volumes need to be planned**.

The more information you can share with Embedded Artists about your plans, estimates and forecasts the higher the likelihood is that we can provide a reliable supply to you of the *iMX6 SoloX COM Board*.

9.6 ESD Precaution when Handling iMX6 SoloX COM Board

Please note that the *iMX6 SoloX COM Board* come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel shall handle the product.

Make it a habit always to first touch one of the four mounting holes (these are grounded) for a few seconds with both hands before touching any other parts of the boards. That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general touch as little as possible on the boards in order to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board, connecting the JTAG cable or when changing boot slider switches.

Note that Embedded Artists does not replace boards that have been damaged by ESD.

9.7 EMC / ESD

The *iMX6 SoloX COM Board* has been developed according to the requirements of electromagnetic compatibility (EMC). Nevertheless depending on the target system, additional anti-interference measurement may still be necessary to adherence to the limits for the overall system.

The *iMX6 SoloX COM Board* must be mounted on carrier board (typically an application specific board) and therefore EMC and ESD tests only makes sense on the complete solution.

No specific ESD protection has been implemented on the *iMX6 SoloX COM Board*, except on the JTAG interface signals, which all have suppressor diodes. ESD protection on board level is the same as what is specified in the iMX6 SoloX SoC datasheet. **It is strongly advised to implement protection against electrostatic discharges (ESD) on the carrier board** on all signals to and from the system. Such protection shall be arranged directly at the inputs/outputs of the system.

10 Custom Design

This document specify the standard *iMX6 SoloX COM Board* design. Embedded Artists offers many custom design services. Contact Embedded Artists for a discussion about different options.

Examples of custom design services are:

- Different memory sizes on DDR3L SDRAM, eMMC Flash and QSPI Flash.
- Different mounting options, for example remove QSPI and one Ethernet interface.
- Different pinning on MXM3 edge pins, including but not limited to, SMARC compatible pinning.
- Different I/O voltage levels on all or parts of the pins.
- Different board form factor, for example SODIMM-200, high-density connectors on bottom side or MXM3 compatible boards that are higher (>50 mm).
- Different input supply voltage range, for example 5V input.
- Single Board Computer solutions, where the core design of the *iMX6 SoloX COM Board* is integrated together with selected interfaces.
- Replace eMMC Flash with (unmanaged) MLC/SLC NAND Flash.
- Changed internal pinning to make certain pins available.

Embedded Artists also offers a range of services to shorten development time and risk, such as:

- Standard Carrier boards ready for integration
- Custom Carrier board design
- Display solutions
- Mechanical solutions

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