XDPL8219 Digital Flyback Controller IC

XDP™ Digital Power

Features

- Flyback controller with ***Power Factor Correction (PFC)***
- ***Secondary Side Regulated (SSR) Constant Voltage (CV)*** output
- Integrated 600 V high voltage startup cell
- Supports universal AC input (90 V_{rms} to 305 V_{rms}) and DC input (127 V to 431 V)
- Enhanced ***Total Harmonic Distortion (THD)*** correction
- Enhanced ***Power Factor (PF)*** correction
- PF > 0.9 and THD < 10% across a wide load range, for AC input up to 277 V_{rms}
- High efficiency and low ***Electro-Magnetic Interference (EMI)***, with ***Quasi-Resonant Mode, switching in valley n (QRMn)***
- No-load standby power as low as < 100 mW and low audible noise, with ***Active Burst Mode (ABM)***
- Low EMI with switching frequency dithering for constant DC input
- Reporting of the input voltage, line frequency, controller temperature, input voltage loss, and error code of last triggered protection, via uni-directional ***Universal Asynchronous Receiver Transmitter*** communication
- Protection features: input over-voltage, input under-voltage, output over-voltage, output short, *VCC* over-voltage, *VCC* under-voltage and ***Integrated Circuit (IC)*** over-temperature protections
- UL1310 safety feature: Adaptive *CS* pin maximum voltage and QRMn minimum valley number limits based on estimated input voltage, to prevent excessive output power at higher input voltage
- Digitally configurable parameters: maximum switching frequency, ABM burst frequency, protection threshold and reaction (auto-restart/latch), etc.

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Potential applications

- Front-stage ***PFC*** converter of the Electronic Control Gear for LED luminaires

Description

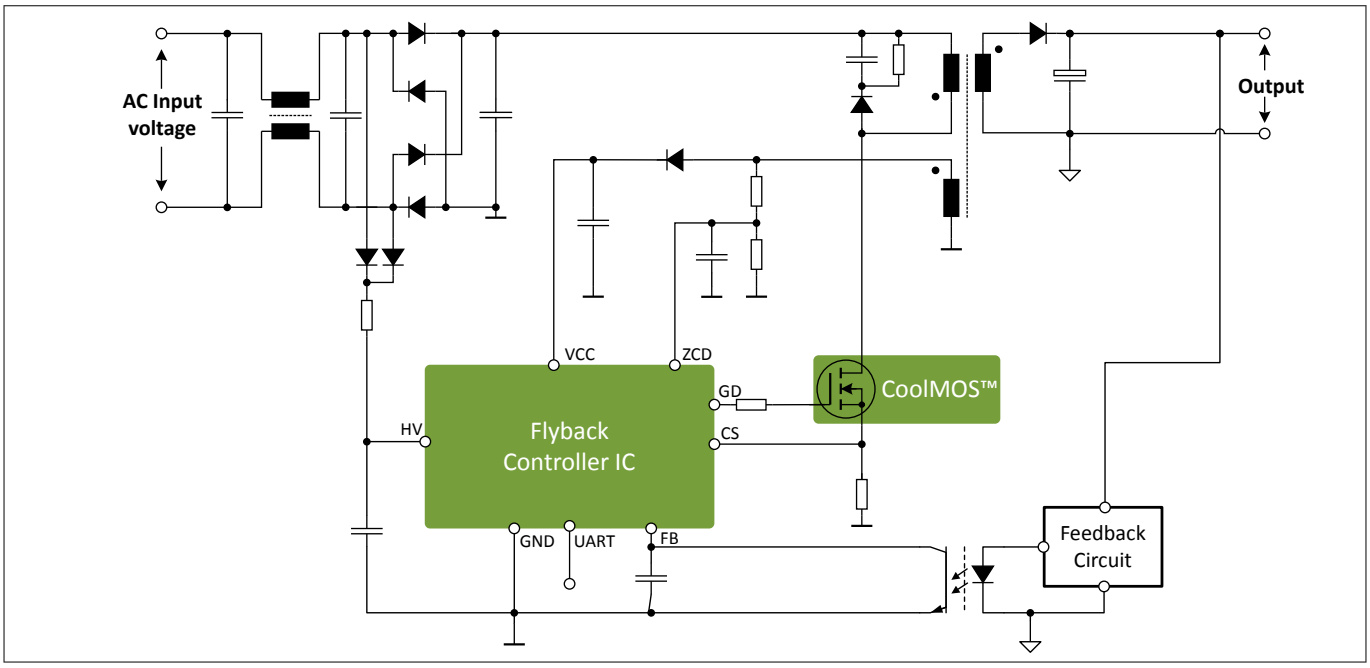

Figure 1 Typical Application for XDPL8219

*Note: The **SSR CV** output in **Figure 1** should not be used to directly drive the LEDs. For LED lighting application, it should be converted to constant current output by a second-stage DC-DC switching or linear regulator.*

Product type	Package	Marking	Firmware version	Ordering code
XDPL8219	PG-DSO-8	L8219	0.0.1.1	SP002990946

Description

The XDPL8219 is a high performance ***SSR CV*** controller for the high power factor flyback converter. The device operates in ***QRMn*** to maximize the efficiency and minimize the ***EMI***, across a wide load range. It enters ***ABM*** at light load to prevent audible noise and at the same time achieving no-load standby power as low as < 100 mW.

The XDPL8219 detects the input voltage type (AC or constant DC) and adapts its proprietary voltage mode pulse modulator accordingly to enhance the system performance. For AC input, it adapts the pulse modulation to achieve high ***PF*** (>0.9) and low ***THD*** (<10%) over wide input and load range. For constant DC input, it adapts the pulse modulation which dithers the switching frequency to lower the EMI over the entire operating range.

Infineon's innovative digital power platform maximizes the XDPL8219 performance in a standard DSO-8 package. The XDPL8219 transmits ***UART*** signals to report the estimated input voltage, estimated line frequency, controller temperature, last error code and input voltage loss indication. In addition, it provides the maximum design flexibility and performance optimization with parameter configuration via UART. Infineon offers the programming tools including an user friendly ***Graphic User Interface*** for ***Personal Computer***s, to configure the XDPL8219 parameters.

The device has a built-in 600 V *HV* start-up cell and also a proprietary start-up sequence to ensure a fast output voltage rise with minimal overshoot.

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1 Pin configuration

Pin assignments and basic pin description information are shown below.

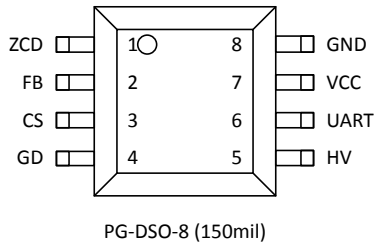


Figure 2 Pinning of XDPL8219

Table 1 Pin definitions and functions

Name	Pin	Type	Function
ZCD	1	I	Zero-crossing detection: The *ZCD* pin is connected to the transformer auxiliary winding via external resistors divider. It is used for zero-crossing detection, primary-side output voltage sensing and input voltage sensing.
FB	2	I	Secondary Side Feedback: The *FB* pin is used as a feedback pin for ***SSR***.
CS	3	I	Current sensing: The *CS* pin is used for Flyback MOSFET current sensing via external shunt resistor.
GD	4	O	Gate driver: The *GD* pin is used for Flyback MOSFET gate drive control via external series resistor.
HV	5	I	High voltage: The *HV* pin is connected to the rectified input voltage via external series resistor. The *HV* pin is used to charge *VCC* pin voltage during startup and protection, via an internal 600 V startup cell. In addition, it is also used for line synchronization.
UART	6	I/O	***UART*** configuration: The *UART* pin is used as the digital interface for IC parameter configuration. It can also be used for the information reporting based on the uni-directional *UART* communication (when *UART* reporting is enabled).
VCC	7	I	Operating voltage supply and sensing
GND	8	-	***IC*** grounding

2 Functional block diagram

The functional block diagram shows the basic data flow from input pins via signal processing to the output pins.

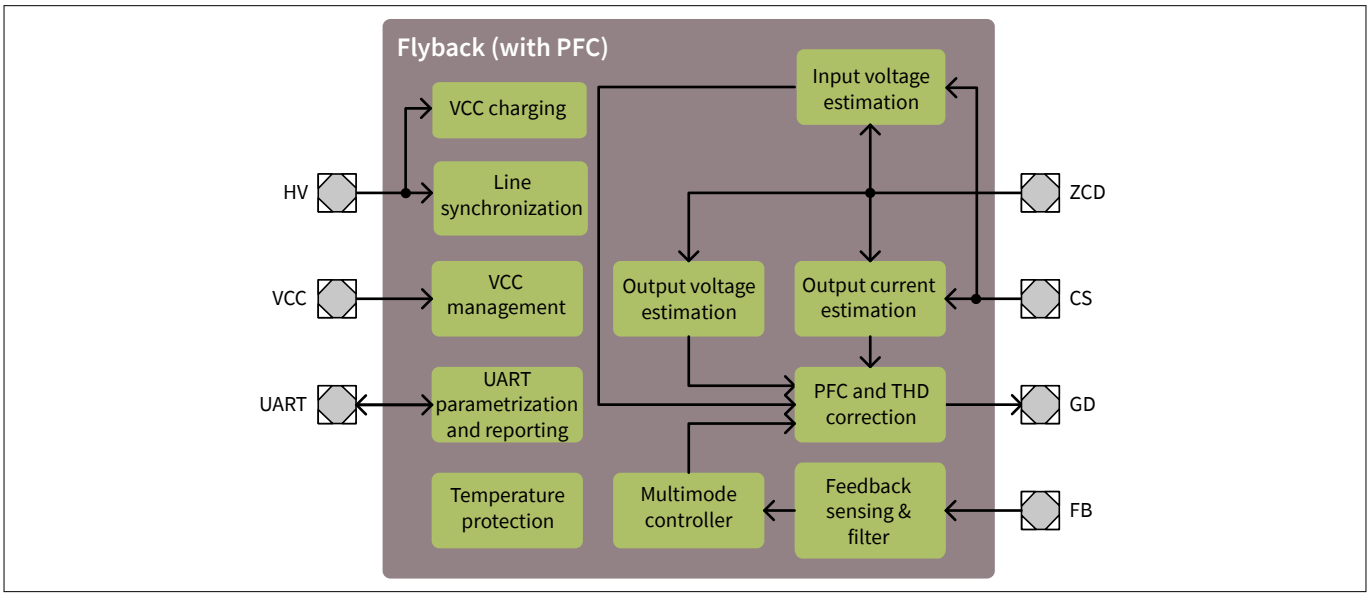


Figure 3 XDPL8219 functional block diagram

3 Functional description

The functional description provides an overview about the integrated functions and features as well as their relationship. The mentioned parameters and equations are based on typical values at T_A = 25°C. The corresponding min. and max. values are shown in the electrical characteristics.

3.1 Startup

The XDPL8219 enters startup phase upon checking the pre-startup conditions (e.g. estimated input voltage, ***IC*** temperature) are within limits. During the startup phase, the soft start phase is initiated and followed by the output charging phase. The soft start phase is to minimize the component stress during startup, while the output charging phase is to fast charge the output voltage to $V_{out,start}$ parameter for fast *VCC* voltage self supply takeover from the primary auxiliary winding.

After the startup phase is ended without any protection triggering, the regulated mode will be entered for output regulation based on the feedback voltage mapping.

3.2 Regulated mode

In regulated mode, the *FB* pin voltage signal is periodically sampled and digitally filtered. Based on the filtered feedback voltage $V_{FB,filtered}$ mapping in ***Figure 4***, the mode of operation (***QRMn***, ***Discontinuous Conduction Mode (DCM)*** or ***ABM***) and the respective switching parameters (on-time t_{on}, valley number N_{valley}, minimum switching period $t_{sw,min}$, pulse number n_{ABM}) are periodically updated in each ***Operation cycle***. The update rate of each switching parameter is independent, and can differ based on the operating mode and conditions.

FB pin voltage pull-up and sampling

The controller has a typical voltage reference V_{REF} of 2.428 V, which is internally connected to its *FB* pin via an internal pull-up resistor. The internal pull-up resistor value is configurable between 2.25 kohm and 7.5 kohm, based on the $R_{FB,pull,up}$ parameter. For the power savings in ABM, the controller disables the internal pull-up during sleep.

To have a high signal-to-noise ratio, the *FB* pin voltage is periodically sampled, at the end of the *CS* leading edge blanking time $t_{CS,LEB}$.

Feedback voltage filtering

The filtering of the sampled feedback voltage depends on the operating mode and conditions:

- QRMn/DCM:

  When the *HV* pin ***Line synchronization*** is properly in place with an AC input, or when a constant DC input voltage is detected by the controller, for a duration more than the $n_{notch,blank}$ parameter, a digital notch filter is enabled. Otherwise, the sampled feedback voltage is processed by a digital low pass filter, to reduce the high frequency component.

  The digital notch filter suppresses either the double-line-frequency sine-wave component of an AC input, or the sine-wave component generated by the ***Switching frequency dithering for constant DC input voltage***, to stabilize the filtered feedback voltage $V_{FB,filtered}$.

- ABM:

  The sampled feedback voltage is processed by a digital low pass filter during the burst pulsing, to reduce the high frequency component.

Filtered feedback voltage mapping

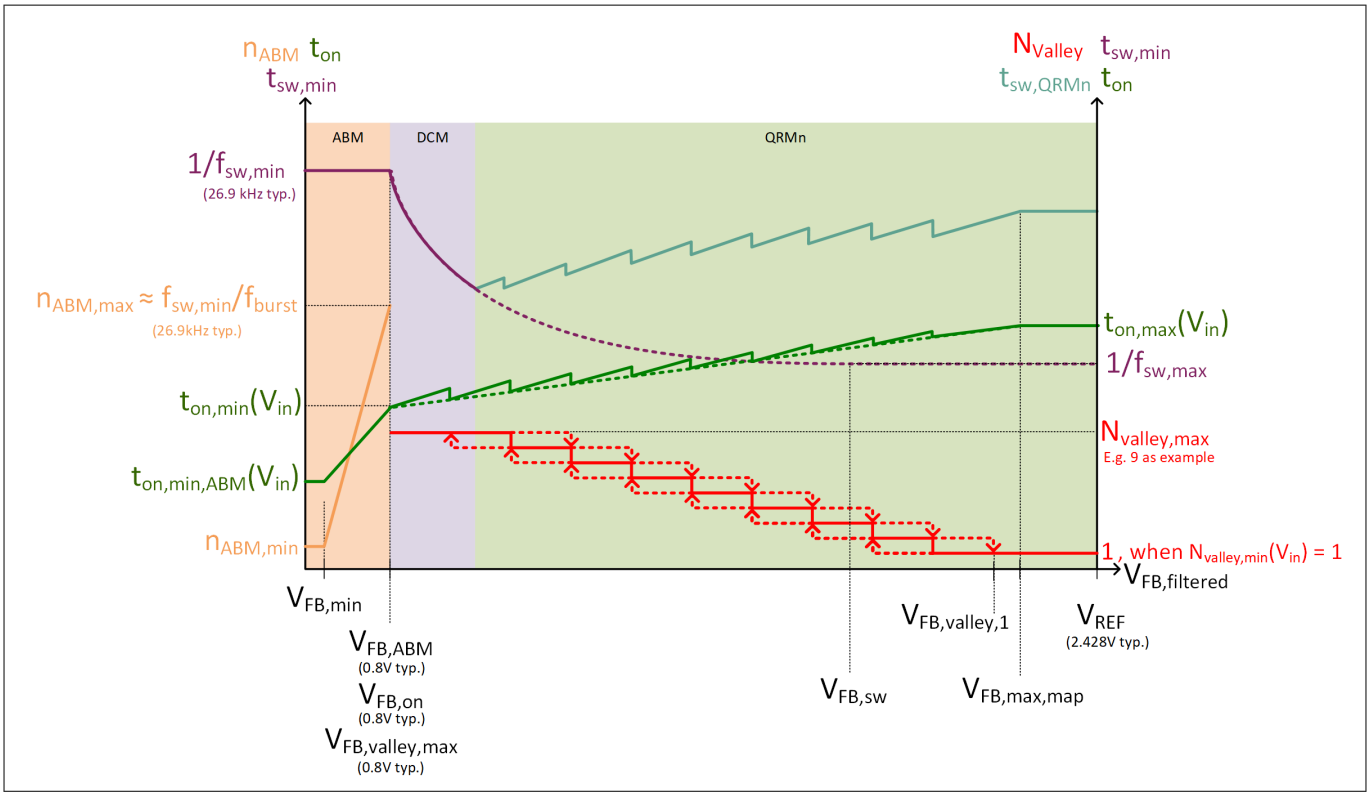


Figure 4 Filtered feedback voltage mapping

- QRMn/DCM:

  The t_{on}, $t_{sw,min}$ and N_{valley} in ***Figure 4*** are mapped from the filtered feedback voltage $V_{FB,filtered}$.

  In QRMn, to switch on the MOSFET at the N_{valley} of the drain voltage, the system-dependent QRMn switching period $t_{sw,QRMn}$ has to be more than $t_{sw,min}$. If the drain voltage valley of N_{valley} happens before $t_{sw,min}$ is reached, the controller operates in DCM and the DCM switching period $t_{sw,DCM}$ follows $t_{sw,min}$.

  For a smoother transition when the N_{valley} changes, the device can compensate the t_{on} curve using $c_{valley,comp}$ parameter. To stabilize the N_{valley} in steady state operation, a hysteresis on N_{valley} change is applied, and the N_{valley} is only updated once in each ***Operation cycle***. If the N_{valley} change is more than a $N_{valley,fast}$ parameter, the controller can speed up the N_{valley} update for a better dynamic load response.

  *Note: Either t_{on} or $t_{sw,min}$, or both can be modulated over every **Operation cycle** to achieve either the **Enhanced power quality** for AC input, or the **Switching frequency dithering for constant DC input voltage**.*

- ABM:

  t_{on} and n_{burst} are mapped from $V_{FB,filtered}$ taken at the last pulse of previous burst cycle.

  Typically, the controller has a burst interval which is approximately the configured $1/f_{burst}$ and enters the sleep mode for power saving after completing the last pulse of each burst cycle, as shown in ***Figure 5***.

  However, if the UART reporting feature is enabled with $EN_{UART,reporting}$ parameter, either a longer than typical burst interval or a delayed sleep mode entry, or both can occur occasionally, for instance when the UART signal transmission can not be completed within the typical burst interval or before the last pulse of a burst cycle.

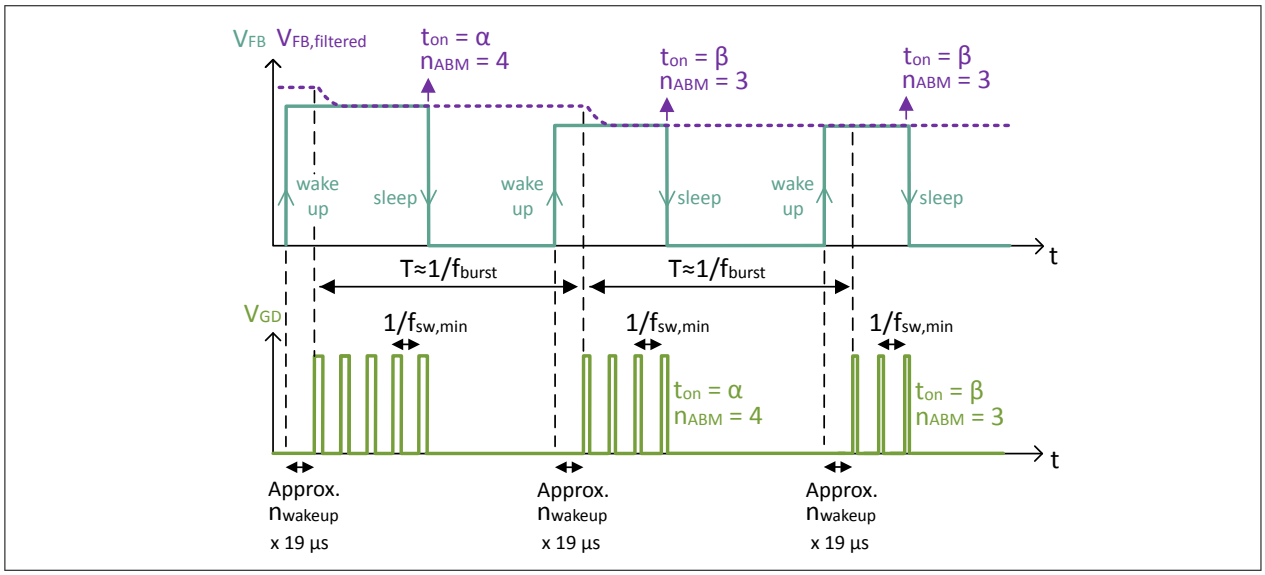


Figure 5 Typical ABM switching waveforms

*Note: The ABM switching pulse frequency typically follows the minimum switching frequency parameter $f_{sw,min}$ (26.9 kHz typ.) but it can be modulated over every **Operation cycle** to achieve the **Switching frequency dithering for constant DC input voltage**.*

Regualted mode *CS* pin maximum voltage and minimum valley number limits

In regulated mode, the minimum valley number limit $N_{valley,min}(V_{in})$ and *CS* pin maximum voltage limit $V_{OCP1}(V_{in})$ are both adaptive based on the estimated input voltage V_{in}, as shown in ***Figure 6***, to prevent excessive output power at higher input voltage. The effective on-time is lower than the mapped t_{on} in ***Figure 4***, if the conducting MOSFET current rises to a level of $V_{OCP1}(V_{in})$ after the *CS* leading edge blanking time $t_{CS,LEB}$ (480 ns typ.).

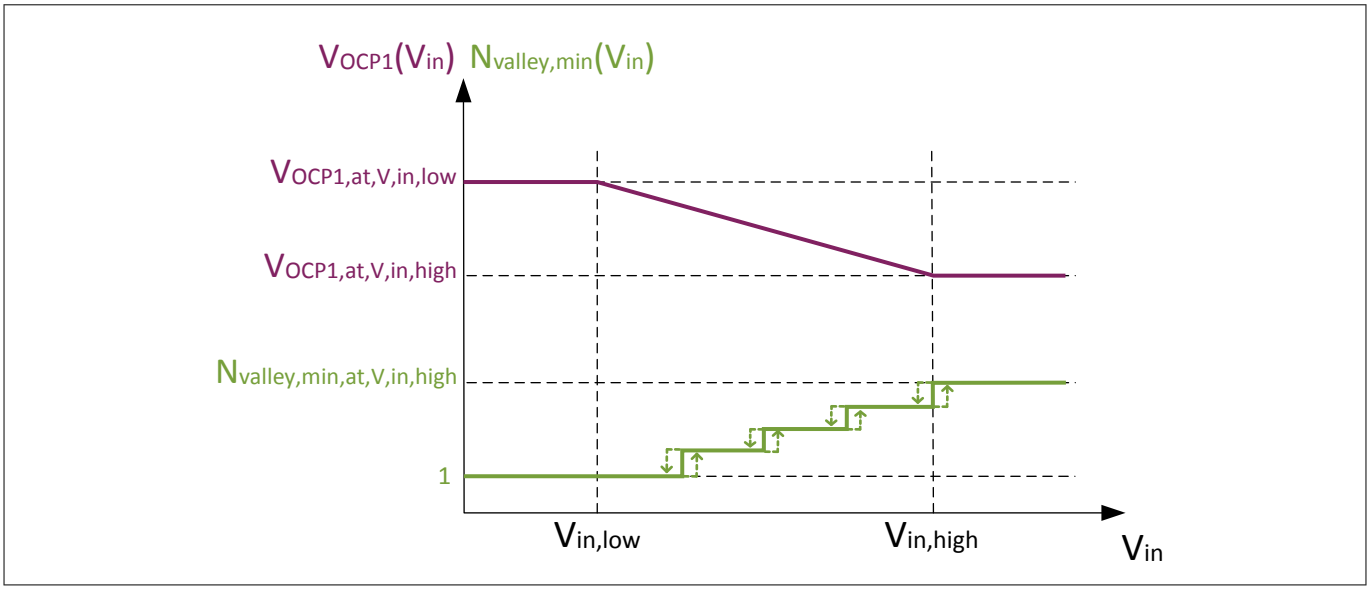


Figure 6 Regulated mode CS pin maximum voltage and minimum valley number limits adaptation based on estimated input voltage V_{in}

*Note: $V_{OCP1}(V_{in})$ and $N_{valley,min}(V_{in})$ are adapted once in every **Operation cycle**.*

On-time limits

The on-time limits in ***Figure 4*** are adaptive based on the estimated input voltage V_{in}.

- QRMn/DCM:

  To sense the output over-voltage level of V_{outOV} parameter, the device calculates a $t_{on,min,V,out,sense}(V_{in})$ variable, which is the estimated minimum on-time to achieve the desired minimum transformer demagnetization time of $t_{min,demag}$ parameter, at the peak of the estimated input voltage $V_{in,peak}$. The minimum on-time limit $t_{on,min}(V_{in})$ is based on the $t_{on,min}$ parameter or the $t_{on,min,V,out,sense}(V_{in})$ variable, whichever is higher, as shown in ***Figure 7***.

  For V_{in} between the lowest operational input voltage parameter $V_{in,low}$ and the input over-voltage protection level parameter V_{inOV}, the maximum on-time limit $t_{on,max}(V_{in})$ is scaled to compensate the influence of input voltage on feedback gain.

  For V_{in} from $V_{in,low}$ to the input under-voltage protection level parameter $V_{in,UV}$, $t_{on,max}(V_{in})$ can be linearly reduced from $t_{on,max,at,V,in,low}$ parameter to $t_{on,max,at,\ Vin,UV}$ parameter, to limit the maximum power during brown-out.

- ABM:

  For V_{in} decreased from $V_{in,high}$, the ABM minimum on-time limit $t_{on,min,ABM}(V_{in})$ is increased from $t_{on,min,ABM}$ parameter, to reduce the burst pulse number for a lower standby power at lower input voltage.

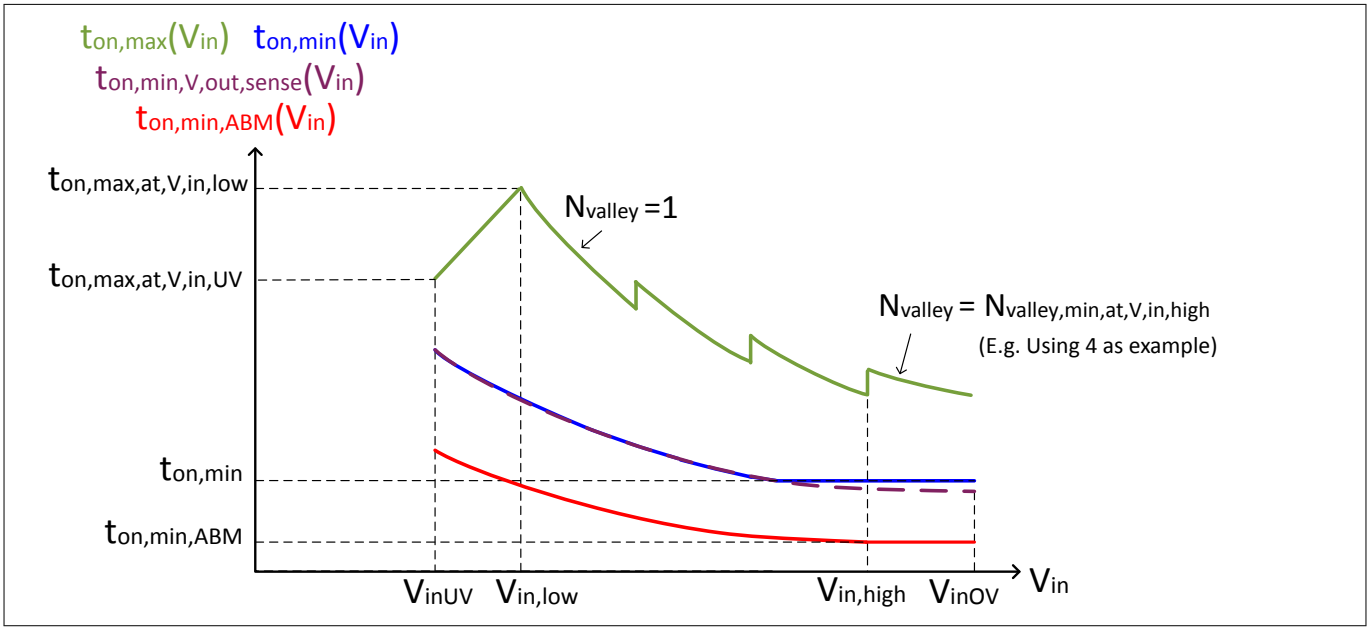


Figure 7 On-time limits adaptation based on estimated input voltage V_{in}

*Note: $t_{on,min}(V_{in})$, $t_{on,max}(V_{in})$, and $t_{on,min,ABM}(V_{in})$ are adapted once in every **Operation cycle**.*

Feedback voltage maximum limit

When the regulated mode is entered, the filtered feedback voltage maximum limit $V_{FB,filtered,max}$ is ramped up from $V_{FB,limit,start}$ (1.2 V typ.) to V_{REF} (2.428 V typ.), with an incremental voltage step of $V_{FB,limit,step}$ parameter after every $t_{FB,limit,step}$.

As shown in ***Figure 8***, when $V_{FB,filtered}$ is higher than $V_{FB,filtered,max}$ initially in the regulated mode entering, the feedback voltage mapping is based on $V_{FB,filtered,max}$ ramp, to prevent the excessive output voltage overshoot during output rise. When $V_{FB,filtered}$ gets lower than $V_{FB,filtered,max}$, the feedback voltage mapping then follows $V_{FB,filtered}$, for the steady-state output regulation.

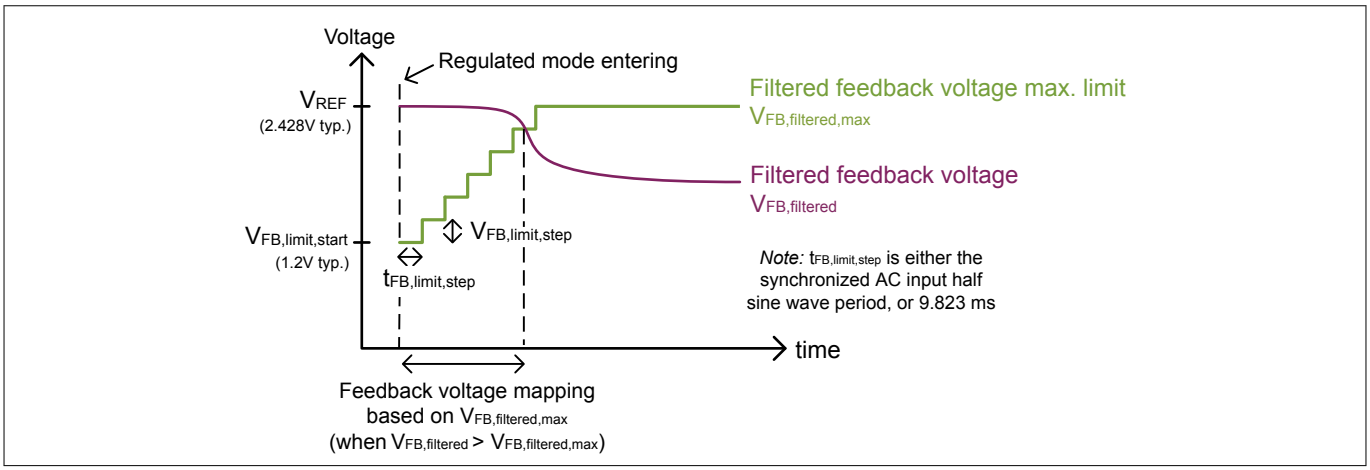


Figure 8 Feedback voltage maximum limit

3.3 Operation cycle

The period of every XDPL8219 operation cycle is 9.823 ms by default. When the *HV* pin ***line synchronization*** is enabled and properly in place with an AC input, it is approximately the half-sine-wave period of an AC input, else it follows the default value.

3.4 Line synchronization

Depending on the operation conditions, the XDPL8219 enables the line synchronization which senses the *HV* pin signal, to detect the input voltage type and the double-line-frequency of an AC input voltage.

If the *HV* pin line synchronization detected input voltage type is AC, the *HV* pin line synchronization is enabled in ***QRMn*** and ***DCM***, and disabled in ***ABM***. It takes some time for the initially enabled *HV* pin line synchronization to be properly in place with an AC input. When the *HV* pin line synchronization is properly in place with an AC input, the double-line-frequency or the half-sine-wave period detected by the controller is synchronized with the AC input, and the *HV* pin signal sensing duty cycle is lowered to reduce the *HV* pin series resistor power consumption.

If the *HV* pin line synchronization detected input voltage type is a constant DC, the *HV* pin line synchronization is disabled, and can only be re-enabled in QRMn and DCM, when an input voltage type change to AC is detected from the ***Input voltage estimation*** via *ZCD* pin and *CS* pin signals.

If the ***UART reporting*** feature is enabled and ABM is entered immediately upon start-up, the *HV* pin line synchronization is enabled initially for a short period of time to detect the initial line frequency.

Attention: ***To ensure the HV pin line synchronization can be established and properly in place with an AC input, the AC input should be a stable sinusoidal waveform with frequency between 45 Hz and 66 Hz. Additionally, the rectified AC input connected to the HV pin via external resistor also should not have excessive noise.***

3.5 Enhanced power quality

In ***QRMn*** and ***DCM***, the *HV* pin synchronized double-line-frequency of the AC input is used as the digital filter notch frequency, to suppress the double-line-frequency sine-wave component of the feedback voltage, to achieve good ***PFC*** and ***THD*** correction. In QRMn and DCM, by synchronizing the regulated mode ***Operation cycle*** with the AC input half-sine-wave period, the controller can also modulate the switching parameters depending on the phase angle, to enhance the PFC and THD correction.

Enhanced THD correction

By enabling the EN_{ETHDC} parameter, the controller compensates the input current distortion caused by the changing QRMn duty cycle over the AC input half-sine-wave period.

Enhanced power factor correction

For better PFC, the patented enhanced PFC (EPFC) feature can be enabled by configuring C_{EMI} parameter value above zero and fine-tuning the value, to compensate the input current displacement effect which is mainly caused by the DC link filter capacitor $C_{DC,filter}$ and the line filter.

3.6 Switching frequency dithering for constant DC input voltage

To lower the ***EMI*** while operating with a constant DC input voltage, the switching frequency dithering feature can be enabled by configuring c_{dither} parameter above zero. Based on the modulation gain parameter c_{dither}, t_{on} and $t_{sw,min}$ are modulated in ***QRMn*** and ***DCM***, while $t_{sw,min}$ is modulated in ***ABM***, to dither the switching frequency.

3.7 Configurable gate voltage rising slope at GD pin

The typical gate drive peak voltage $V_{GD,pk}$ is 12 V. To achieve a good balance of switching loss and ***EMI***, the gate voltage rising slope which determines the MOSFET switching on speed can be controlled, by configuring the gate driver peak source current parameter $I_{GD,pk}$.

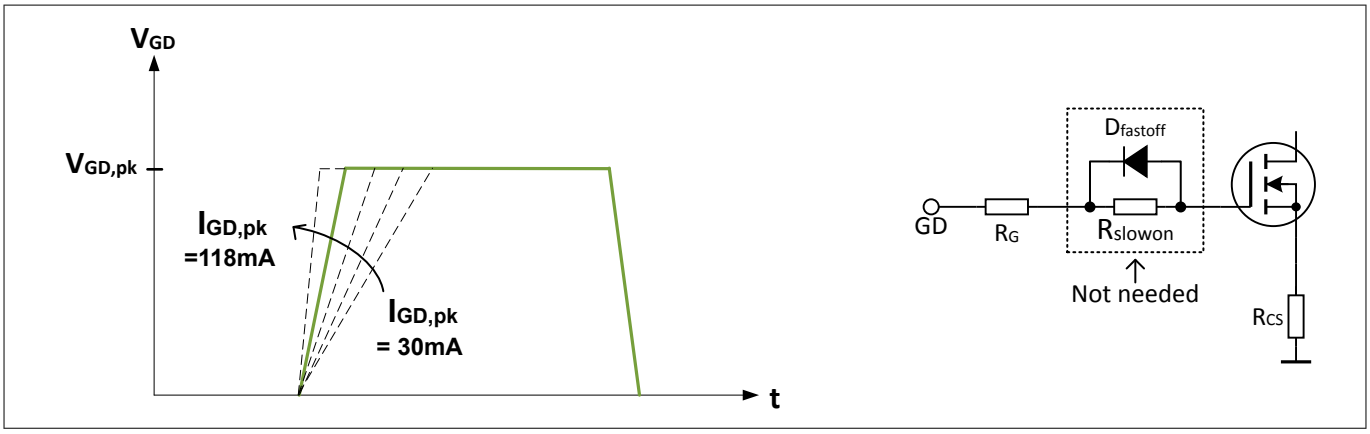


Figure 9 Configurable gate voltage rising slope and component saving

3.8 UART reporting

XDPL8219 ***UART*** reporting can be enabled to transmit data packet which contains the following data, at specific timings and conditions:

- Last estimated input voltage rms value V_{in}, based on the ***Input voltage estimation***
- Last detected line frequency or input voltage type, based on the *HV* pin ***Line synchronization***
- Last measured ***IC*** junction temperature, based on its internal sensor
- Indication of an input voltage loss, if the consecutive number of too low *ZCD* pin $-I_{IV}$ sampling value has exceeded the limit
- Error code of the last triggered protection before auto-restart

The UART reporting is based on the uni-directional UART communication with a fixed baud rate of 9600 bps.

3.9 Input voltage and output voltage estimation

XDPL8219 estimates the input voltage and output voltage based on the *ZCD* pin switching signal. As shown in the waveform example in ***Figure 10***, the transformer primary auxiliary winding voltage V_{AUX} contains information on the reflected input voltage and reflected output voltage, which can be measured at *ZCD* pin using a resistor divider.

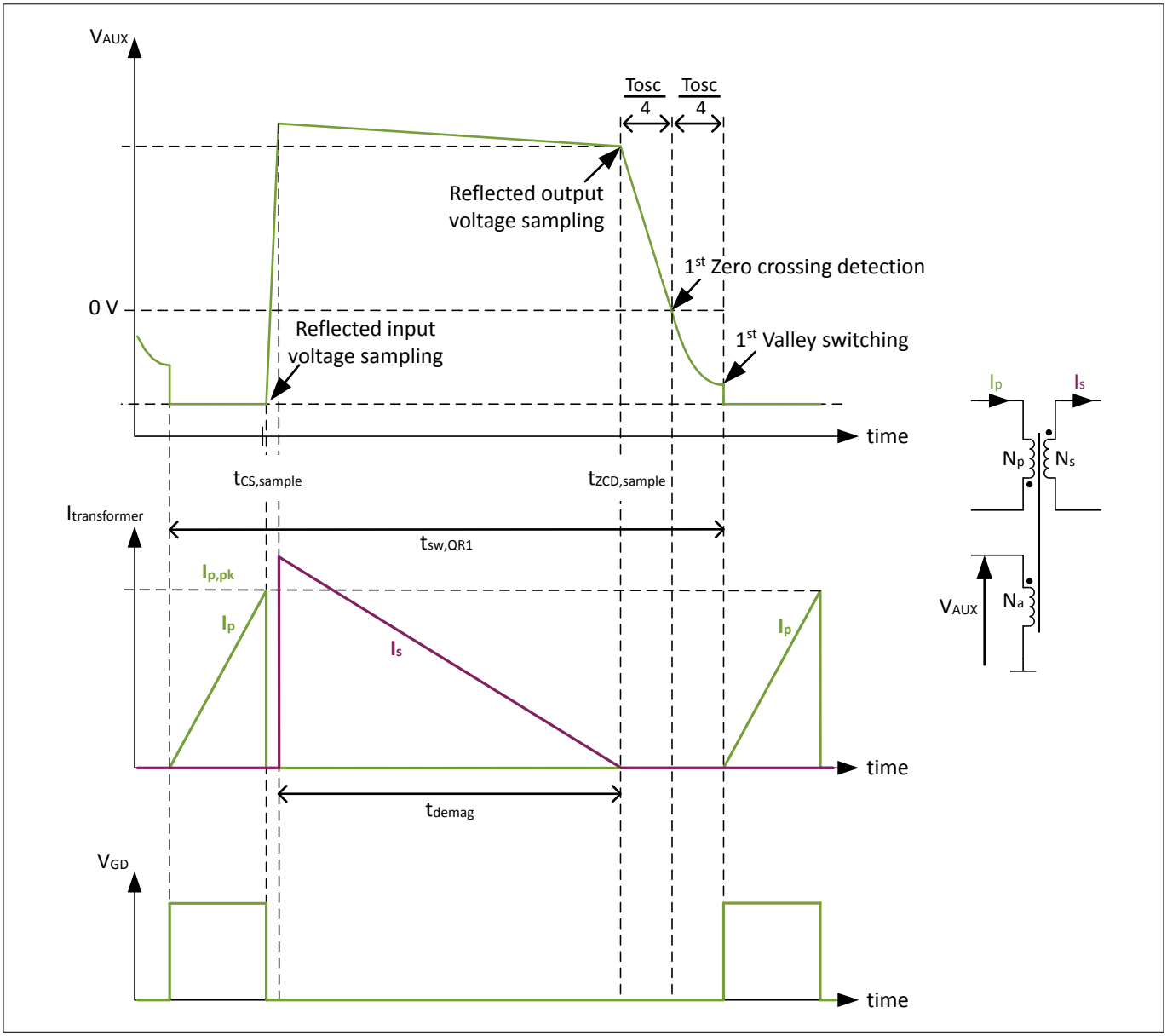


Figure 10 Flyback switching waveform example in QRM1

3.9.1 Output voltage estimation

The output voltage is estimated by sensing the reflected output voltage signal from the transformer primary auxiliary winding voltage V_{AUX}, when the MOSFET is switched off and near the end of transformer demagnetization. A resistor divider with $R_{ZCD,1}$ and $R_{ZCD,2}$ adapts the voltage at *ZCD* pin based on its operational range, while a *ZCD* pin filter capacitor C_{ZCD} is needed for noise filtering, as shown in ***Figure 11***.

Based on the sampled *ZCD* pin voltage $V_{ZCD,SH}$ at the timing of $t_{ZCD,sample}$ shown in ***Figure 10***, which is approximately a quarter of oscillation period (T_{osc}/4) before the 1st zero crossing of V_{AUX}, a ratio of the reflected output voltage signal from V_{AUX} is sensed. In ***QRMn*** and ***DCM***,the typical interval of each $V_{ZCD,SH}$ sampling is

approximately 1/64 of the regulated mode ***Operation cycle***, while the oscillation period T_{osc} is measured once during startup and updated every 7th regulated mode ***Operation cycle***.

Note: *As V_{AUX} zero crossing can only be detected by the **IC** via ZCD pin upon its internal analog delay plus external delay caused by C_{ZCD}, t_{ZCDPD} parameter fine-tuning is needed to compensate such delays, to have the proper timing of $t_{ZCD,sample}$ for output voltage estimation.*

Attention: ***Please note that the transformer demagnetization time t_{demag} has to be at least 2.0 µs at the peak of input voltage, to ensure that the reflected output voltage can be sensed properly at the ZCD pin.***

The estimated output voltage V_{out} is based on:

$$V_{out} = V_{ZCD,SH} \cdot \frac{R_{ZCD,1} + R_{ZCD,2}}{R_{ZCD,2}} \cdot \frac{N_s}{N_a} - V_d$$

Equation 1

Where N_s is the transformer secondary main winding turns, N_a is the transformer primary auxiliary winding turns and V_d is the secondary main output diode forward voltage (assumed by the controller as 0.7 V).

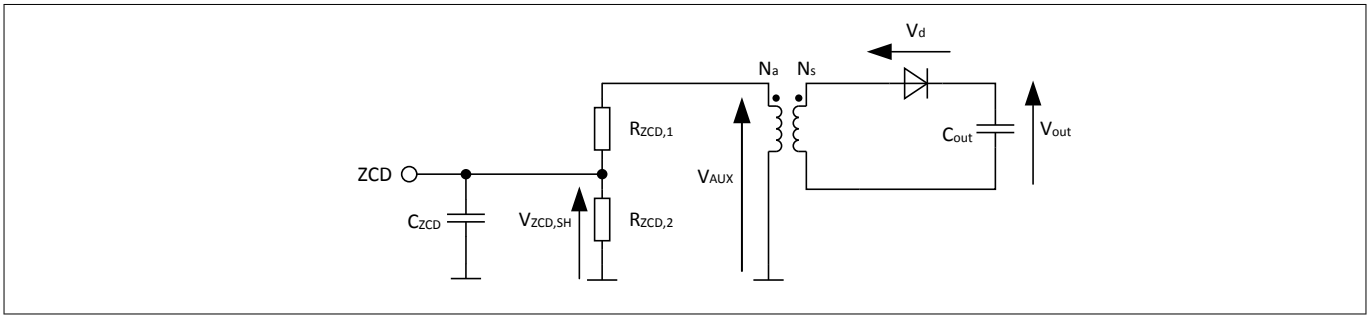


Figure 11 Output voltage estimation based on $V_{ZCD,SH}$

The estimated output voltage V_{out} is used for output voltage protections, so it is important to ensure that IC parameters $R_{ZCD,1}$, $R_{ZCD,2}$, N_s and N_a are configured as per the actual system hardware dimensioning.

3.9.2 Input voltage estimation

The input voltage is estimated by sensing the reflected input voltage signal from the transformer primary auxiliary winding voltage V_{AUX}, when the MOSFET is switched on. As the reflected input voltage signal is a negative voltage which cannot be sensed directly, the voltage at *ZCD* pin is clamped to a negative voltage of V_{INPCLN}. A resistor divider with $R_{ZCD,1}$ and $R_{ZCD,2}$ adapts $-I_{IV}$ which is the clamping current flowing out of *ZCD* pin, based on its operational range, while a *ZCD* pin filter capacitor C_{ZCD} is needed for noise filtering, as shown in ***Figure 12***.

Based on the sampled clamping current $-I_{IV}$ at the timing of $t_{CS,sample}$ shown in ***Figure 10***, which is at the end of on-time, the reflected input voltage signal from V_{AUX} is sensed. The typical interval of each $-I_{IV}$ sample is approximately 1/64 of the regulated mode ***Operation cycle***, when the XDPL8219 is awake and gate driver output is switching.

The estimated peak input voltage $V_{in,peak}$ over every regulated mode ***Operation cycle*** is based on:

$$V_{in,peak} = \max\left\{\frac{N_p}{N_a} \cdot \left[\left(-I_{IV} - \frac{V_{INPCLN}}{R_{ZCD,2}}\right) \cdot R_{ZCD,1} - V_{INPCLN}\right] + \frac{R_{in}}{R_{CS}} \cdot V_{CS,peak}\right\}$$

Equation 2

Where N_p is the primary main winding turns, N_a is the primary auxiliary winding turns, R_{CS} is the *CS* pin shunt resistor value, $V_{CS,peak}$ is the peak *CS* pin voltage, and R_{in} is the fine-tuning parameter for input voltage sensing accuracy improvement by compensating the switching frequency voltage ripple on $C_{DC,filter}$.

Regardless of the input voltage type is AC or a constant DC, the estimated input voltage V_{in} in rms value is assumed by the controller as 0.707 of $V_{in,peak}$ based on a filtered value over a few regulated mode operation cycles. The update rate of V_{in} is once per regulated mode operation cycle.

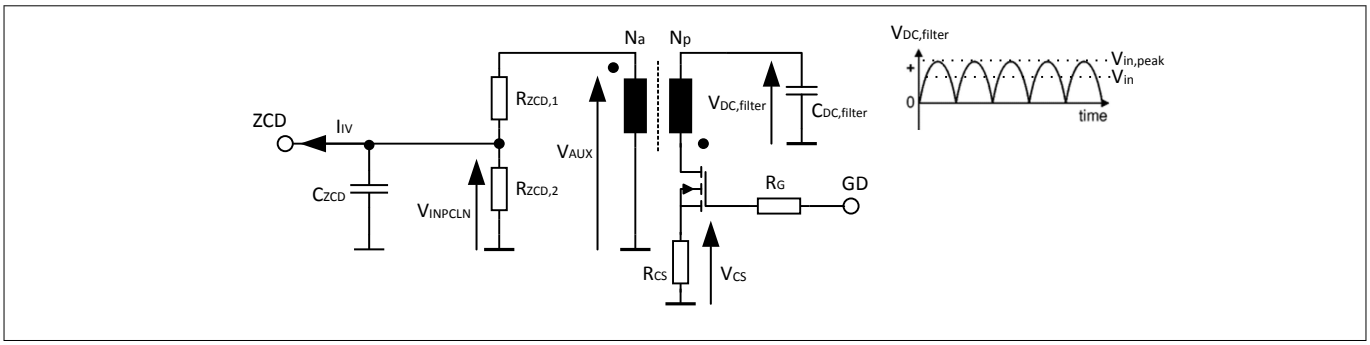


Figure 12 Input voltage estimation based on $-I_{IV}$

The estimated input voltage V_{in} is used for input voltage protections, so it is important to ensure that ***IC*** parameters $R_{ZCD,1}$, $R_{ZCD,2}$, N_p, N_a and R_{CS} are configured as per the actual system hardware dimensioning.

3.10 Protection features

Protections ensure the operation of the controller under restricted conditions. The protection monitoring signal(s) sampling rate, protection triggering condition(s) and protection reaction are described in this section.

Attention**: **The sampled protection monitoring signal accuracy is subjective to the digital quantization, tolerances of components (including IC) and estimations with indirect sensing (e.g. input and output voltage estimations based on ZCD, CS pin signals), while the protection level triggering accuracy is subjective to the sampled signal accuracy, sampling delay, indirect sensing delay (e.g. reflected output voltage signal cannot be sensed by ZCD pin near AC input phase angle of 0° and 180°) and blanking time.

3.10.1 Primary MOSFET overcurrent protection

V_{OCP2} denotes the *CS* pin voltage level 2 for primary MOSFET overcurrent protection. Under the single fault condition of shorted primary main winding, the primary MOSFET overcurrent protection is triggered when the *CS* pin voltage exceeds V_{OCP2} for longer than a blanking time based on t_{CSOCP2} parameter. The level of V_{OCP2} is automatically selected based on ***Table 2***.

Table 2 V_{OCP2} level selection depending on $V_{OCP1,at,V,in,low}$ parameter value

$V_{OCP1,at,V,in,low}$ (V)	V_{OCP2} (V)
0.34 to 0.36	0.6
0.37 to 0.54	0.8
0.55 to 0.72	1.2
0.73 to 1.08	1.6

The reaction of primary MOSFET overcurrent protection is fixed as auto-restart.

3.10.2 Output undervoltage protection

In case of a short or an overload on the output, the output voltage may drop to a low level. The output undervoltage protection can be triggered, if the condition is met by monitoring the estimated output voltage V_{out} based on the *ZCD* pin switching signal (see ***Output voltage estimation*** for details).

$EN_{UVP,Vout}$ parameter refers to the enable switch for the regulated mode output undervoltage protection. In regulated mode, if $EN_{UVP,Vout}$ parameter is enabled and the estimated output voltage V_{out} is lower than V_{outUV}

parameter for longer than a blanking time of $t_{VoutUV,blank}$ parameter, the regulated mode output undervoltage protection is triggered. The reaction of regulated mode output undervoltage protection is configurable to either auto-restart or latch mode based on *Reaction*$_{UVP,Vout}$ parameter.

Attention**: **Regulated mode output undervoltage protection is not available while the controller operates in ABM.

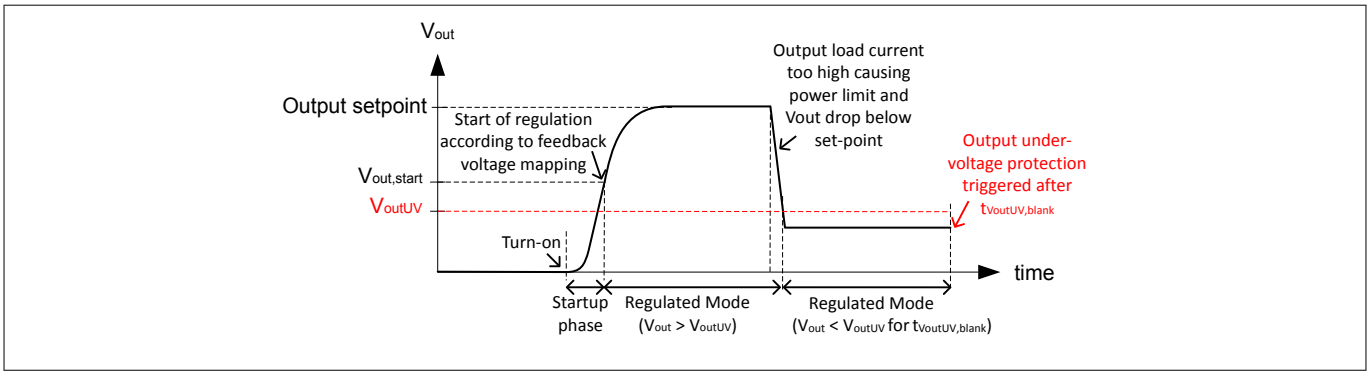


Figure 13 Regulated mode output undervoltage protection triggering waveform example

In startup phase, if the estimated output voltage V_{out} is lower than the $V_{out,start}$ parameter level after a timeout period of $t_{start,max}$ parameter, the startup output undervoltage protection is triggered. $t_{start,max}$ parameter refers to the maximum allowable duration of the startup phase, which consists of soft-start phase and output charging phase. It can be indirectly configured with *VCC* capacitance parameter C_{VCC}.

The reaction of startup output undervoltage protection is fixed as auto-restart.

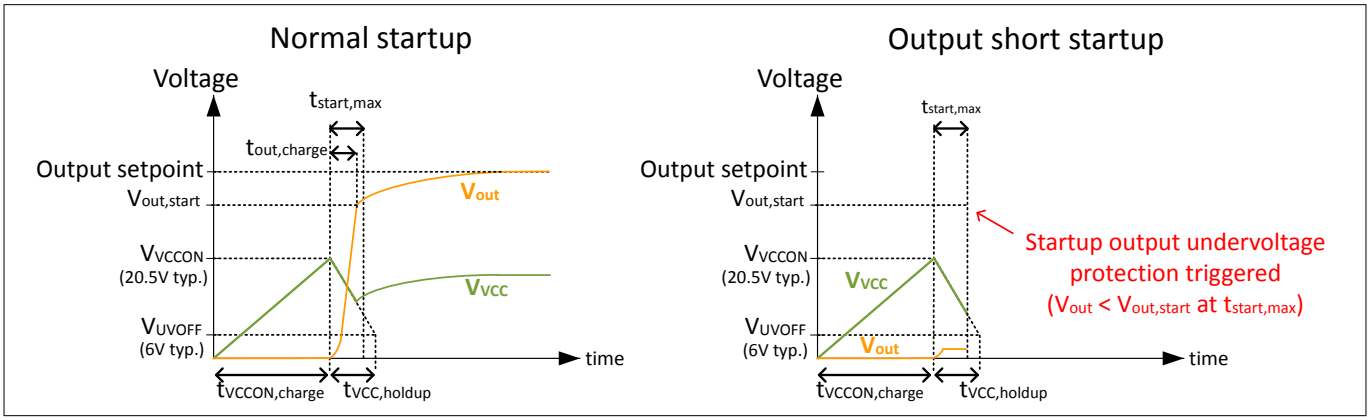


Figure 14 Normal startup and startup output undervoltage (short) protection waveform example

3.10.3 Output overvoltage protection

In case of *FB* pin open, the output voltage may rise to a high level. The output overvoltage protection can be triggered, if the condition is met by monitoring the estimated output voltage V_{out} based on the *ZCD* pin switching signal (see ***Output voltage estimation*** for details).

If the estimated output voltage V_{out} is higher than V_{outOV} for longer than a blanking time, the output overvoltage protection is triggered. The output overvoltage protection blanking time is typically a quarter of the ***Operation cycle***. The reaction of the output overvoltage protection is configurable to auto-restart or latch-mode based on *Reaction*$_{OVP,Vout}$ parameter.

Attention**: **Output overvoltage protection is not available while the controller operates in ABM.

Attention**: **It is mandatory to ensure that V_{outOV} is configured well below the actual output capacitor voltage rating $V_{out,cap,rating}$,while the $V_{out,cap,rating}$ is not exceeded in actual testing with all the necessary test conditions. The protection level triggering accuracy is subjective to the sampled

signal accuracy, sampling delay, indirect sensing delay (e.g. reflected output voltage signal cannot be sensed by ZCD pin near AC input phase angle of 0° and 180°) and blanking time.

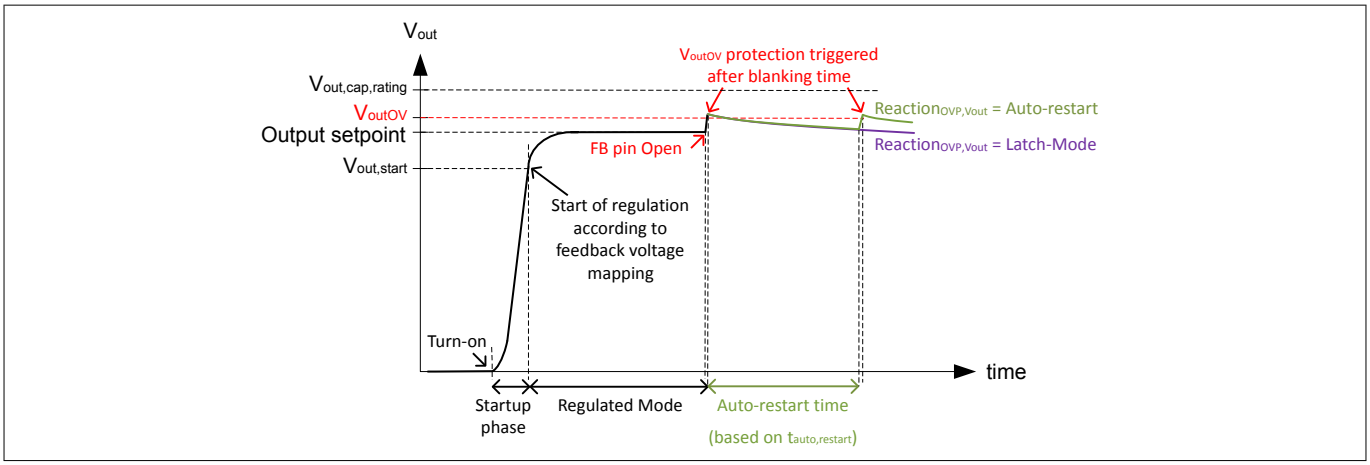


Figure 15 Output overvoltage protection

3.10.4 Transformer demagnetization time shortage protection

In case of insufficient transformer demagnetization time, the reflected output voltage signal cannot be properly sensed via the *ZCD* pin. If such condition presents for longer than 50% of the regulated mode operation cycle, the protection will be triggered. The reaction of this protection is fixed as auto-restart.

Attention**: **Transformer demagnetization time shortage protection is not available while the controller operates in ABM.

3.10.5 Minimum input voltage startup check and input undervoltage protection

By monitoring the estimated input voltage V_{in} mainly based on the *ZCD* pin switching signal (see ***Input voltage estimation*** for details), the minimum input voltage startup check can be performed, and the input undervoltage protection can be triggered if the condition is met.

$EN_{UVP,In}$ parameter refers to the enable switch for the minimum input voltage startup check (based on $V_{in,start,min}$) and input undervoltage protection (based on V_{inUV}).

Note: $V_{in,start,min}$ parameter refers to the minimum input voltage level for startup, while V_{inUV} parameter refers to the input undervoltage protection level.

During pre-startup check, if $EN_{UVP,In}$ parameter is enabled and the estimated input voltage V_{in} is lower than $V_{in,start,min}$, the startup phase will not be entered and the protection reaction of auto-restart will be performed.

Upon startup and in the regulated mode, the input undervoltage protection triggering condition depends on the operating mode:

- ***QRMn*/*DCM***:

  If $EN_{UVP,In}$ parameter is enabled and the estimated input voltage V_{in} is lower than V_{inUV} for longer than a blanking time $t_{VinUV,blank}$, the input undervoltage protection will be triggered. $t_{VinUV,blank}$ is typically 10 times of the regulated mode ***Operation cycle***.

- ***ABM***:

  If $EN_{UVP,In}$ parameter is enabled, $EN_{VIN,ABM}$ parameter is enabled and the estimated input voltage V_{in} is lower than V_{inUV} for longer than a blanking time, the input undervoltage protection will be triggered. The blanking time of the input undervoltage protection may deviate from the blanking time in other modes due to a integer rounding to a number of bursts.

Note: *$EN_{VIN,ABM}$ refers to the enable switch for input voltage protections in Active Burst Mode (ABM).*

The reaction of the input undervoltage protection is fixed as auto-restart.

3.10.6 Maximum input voltage startup check and input overvoltage protection

By monitoring the estimated input voltage V_{in} mainly based on the *ZCD* pin switching signal (see ***Input voltage estimation*** for details), the maximum input voltage startup check can be performed, and the input overvoltage protection can be triggered if the condition is met.

$EN_{OVP,In}$ parameter refers to the enable switch for the maximum input voltage startup check (based on $V_{in,start,max}$) and input overvoltage protection (based on V_{inOV}).

Note: *$V_{in,start,max}$ parameter refers to the maximum input voltage level for startup, while V_{inOV} parameter refers to the input overvoltage protection level.*

During pre-startup check, if $EN_{OVP,In}$ parameter is enabled and the estimated input voltage V_{in} is higher than $V_{in,start,max}$, the startup phase will not be entered and the protection reaction of auto-restart will be performed.

Upon startup and in the regulated mode, the input overvoltage protection triggering condition depends on the operating mode:

- ***QRMn***/***DCM***:

  If $EN_{OVP,In}$ parameter is enabled and the estimated input voltage V_{in} is higher than V_{inOV} for longer than a blanking time $t_{VinOV,blank}$, the input overvoltage protection will be triggered. $t_{VinOV,blank}$ is typically 1 regulated mode ***Operation cycle***.

- ***ABM***:

  If $EN_{OVP,In}$ parameter is enabled, $EN_{VIN,ABM}$ parameter is enabled and the estimated input voltage V_{in} is higher than V_{inOV} for longer than a blanking time, the input overvoltage protection will be triggered. The blanking time of the input overvoltage protection may deviate from the blanking time in other modes due to a integer rounding to a number of bursts.

  Note: *$EN_{VIN,ABM}$ refers to the enable switch for input voltage protections in Active Burst Mode (ABM)*

The reaction of the input overvoltage protection is fixed as auto-restart.

3.10.7 VCC undervoltage lockout

The ***Undervoltage Lockout (UVLO)*** is implemented in the hardware. It ensures the enabling and disabling of the ***IC*** operation based on the defined thresholds of the operating supply voltage V_{VCC} at the *VCC* pin.

The UVLO contains a hysteresis with the voltage thresholds V_{VCCon} for enabling the controller and V_{UVOFF} for disabling the controller. Once the mains input voltage is applied, current flows through an external resistor into the *HV* pin via the integrated depletion cell and diode to the *VCC* pin. The controller is enabled once V_{VCC} exceeds the V_{VCCon} threshold and V_{VCC} will then start to drop. For normal startup, V_{VCC} supply should be taken over by either external supply or the self-supply via the auxiliary winding before V_{VCC} drops to V_{UVOFF}.

3.10.8 VCC undervoltage protection

The *VCC* voltage sampling interval is approximately 1/64 of the regulated mode ***Operation cycle***, when the XDPL8219 is awake and the gate driver output is switching. In regulated mode, if $EN_{VCC,UVP}$ parameter is enabled and the filtered value out of the *VCC* sampling is lower than the *VCC* undervoltage protection level $V_{VCC,min}$ for longer than a blanking time, the *VCC* undervoltage protection will be triggered. The *VCC* undervoltage protection reaction is fixed as auto-restart.

3.10.9 VCC overvoltage protection

The *VCC* voltage sampling interval is approximately 1/64 of the ***Operation cycle***, when the XDPL8219 is awake and the gate driver output is switching. If the filtered value out of the *VCC* voltage sampling data is higher than the *VCC* overvoltage protection level $V_{VCC,max}$, the *VCC* overvoltage protection will be triggered. The *VCC* overvoltage protection reaction is configurable to auto-restart or latch-mode based on $Reaction_{VCC,OVP}$ parameter.

3.10.10 IC overtemperature protection

The ***IC*** junction temperature T_j is sampled 1 time every regulated mode ***Operation cycle***. If the sampled IC junction temperature T_j is higher than $T_{critical}$ parameter, the IC overtemperature protection will be triggered. The protection reaction is fixed as auto-restart, while the maximum junction temperature for startup and restart $T_{start,max}$ is fixed as 4°C below $T_{critical}$.
If $T_{critical}$ is configured above 119°C, the maximum switching frequency parameter $f_{sw,max}$ cannot be configured above 186.4 kHz. If $T_{critical}$ is 119°C or below, the maximum configurable $f_{sw,max}$ value is 247.2 kHz.

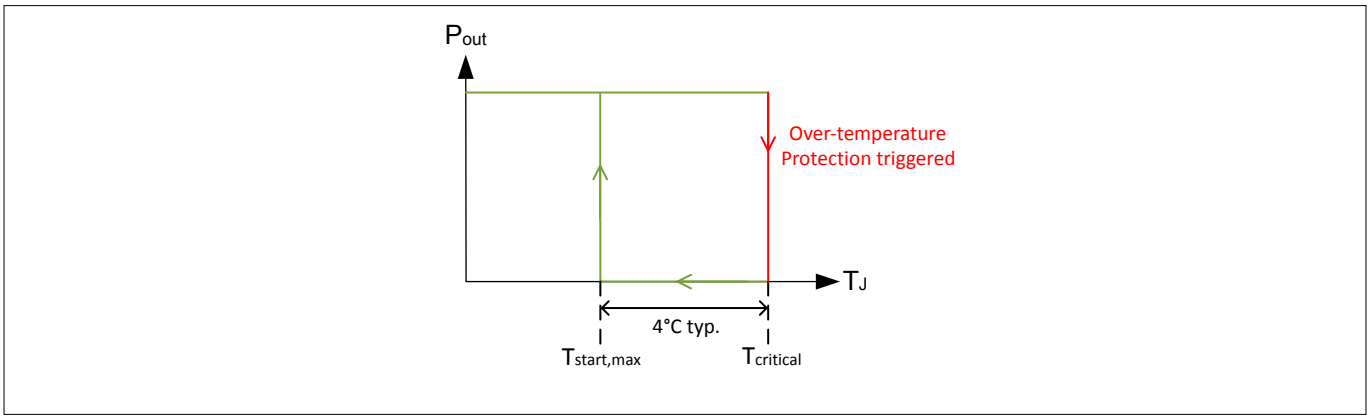


Figure 16 IC overtemperature protection

3.10.11 Other protections

- A hardware weak pull-up protects against an open *CS* pin. The reaction of this protection reaction is auto-restart.
- A firmware watchdog triggers a protection if the ADC hardware cannot provide all necessary information within a defined time period. This may occur if timing requirements for the ADC are exceeded. The reaction of this protection is fast auto-restart.
- A hardware watchdog checks correct execution of firmware. A protection is triggered in the event that the firmware does not service the watchdog within a defined period. The reaction of this protection is auto-restart.
- A hardware ***Random Access Memory*** parity check triggers a protection if a bit in the memory changes unintentionally. The reaction of this protection is auto-restart.
- A firmware ***Cyclic Redundancy Check*** at each startup verifies the integrity of firmware and parameters. The reaction of this protection is stop mode.
- A firmware task execution watchdog triggers a protection if the firmware tasks are not executed as expected. The reaction of this protection is auto-restart.
- A protection is triggered if the configurable parameter values are empty at startup. The reaction of this protection is stop mode.
- A protection is triggered if no reflected input voltage signal sensed from the *ZCD* pin at startup. The reaction of this protection is stop mode.

3.10.12 Protection reactions

The sequence of a protection reaction (not including hardware restart reaction) is as follows:

1. Upon triggering a protection, the gate driver is disabled within a maximum time, which is 1/512 of the regulated mode operation cycle.
2. The reaction depends on the triggered protection:
   - In case of latch mode, the application will enter latch mode at this time. No further sequence is done until *VCC* voltage drops below V_{UVOFF}.
   - In case of auto-restart reaction, the controller will enter power saving mode PSMD2 with the auto-restart time based on $t_{auto,restart}$.
   - In case of fast auto-restart reaction, the controller will enter power saving mode PSMD2 with the fast auto-restart time of 0.4 s typically.

   Note: For latch mode, auto-restart and fast auto-restart reactions, the internal HV startup cell is automatically enabled and disabled during this sequence, in order to keep the VCC voltage between the V_{UVLO} and V_{OVLO} thresholds.

   Note: For stop mode, if there is no external voltage supply for the VCC, the VCC voltage will drain to V_{UVOFF} and a hardware restart will be performed.
3. After the (fast) auto-restart time is expired, the controller executes a single discharge pulse of duration t_{pw}. This pulse partially discharges the capacitance after the bridge rectifier to improve accuracy of the next pre-startup input voltage check.
4. Any auto restart may include a new *VCC* charging cycle. The recharging time of *VCC* via *HV* pin current depends on the input voltage level and *VCC* level at the time when the (fast) auto-restart time is expired.
5. The power stage will enable its gate driver for pre-startup check. If the conditions for pre-startup check are within limits, the startup phase is entered and followed by the regulated mode. During this time, if any protection is triggered, the sequence of a protection reaction (not including hardware restart reaction) starts again from step number 1 above.

3.11 Debug mode

The $Debug_{Mode}$ parameter can be enabled to enter stop mode reaction upon the protection triggering (except for *VCC* undervoltage lockout), to read out the error code of the protection. For example in ***Figure 17***, the error code readout in the ***GUI*** shows a number of 0040_H (in red color), which indicates that the input undervoltage protection has been triggered.

Note: $Debug_{Mode}$ parameter should only be enabled for debugging purpose. For the final application, it has to be disabled.

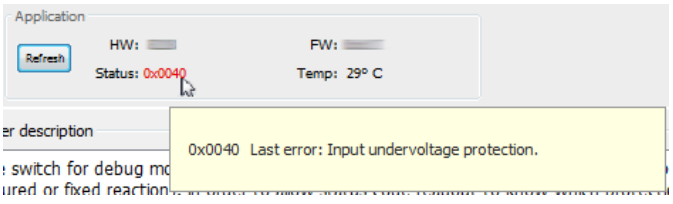


Figure 17 Error status code readout for debugging

4 List of Parameters

This list provides information about the configurable and fixed parameters.

This document uses symbols to ease the readability of formulas. As some tools do not support this format, the symbols are translated into plain text using underscores. For example, the parameter $f_{sw,max}$ translates to f_sw_max.

All parameter values are typical settings. The accuracy might vary due to digital quantization and tolerances.

Note: By default, the configurable parameters of a new XDPL8219 chip from Infineon are empty, so it is necessary to configure them digitally via UART pin before any application testing.

List of configurable parameters

Table 3 Configurable parameters for hardware configuration

Symbol	Basic description	Example	Minimum value	Maximum value
N_p	Transformer primary main winding turns	32	1	300
N_s	Transformer secondary main winding turns	10	1	300
N_a	Transformer primary auxiliary winding turns	3	1	300
L_p	Transformer nominal primary main winding inductance	0.544 mH	Refer GUI	3 mH
R_{CS}	Current sense resistor value	0.2 Ω	0.1 Ω	3 Ω
$R_{ZCD,1}$	*ZCD* series resistor value	27 kΩ	Refer GUI	Refer GUI
$R_{ZCD,2}$	*ZCD* shunt resistor value	3.9 kΩ	Refer GUI	Refer GUI
C_{VCC}	*VCC* capacitor value	22 µF	21.94 µF	100 µF
$V_{out,cap,rating}$	Main output capacitor voltage rating	80 V	10 V	450 V
R_{HV}	*HV* series resistor value	52 kΩ	Refer GUI	255 kΩ
$I_{GD,pk}$	Gate driver peak source current	30 mA	30 mA	108 mA

Table 4 Configurable parameters for startup

Symbol	Basic description	Example	Minimum value	Maximum value
n_{ss}	Number of soft start steps	3	1	Refer GUI
$V_{out,start}$	Output charging phase output voltage set-point	33 V	Refer GUI	V_{outOV}
$V_{start,OCP1}$	Output charging phase *CS* pin maximum voltage limit	0.52 V	Refer GUI	$V_{OCP1,at,V,in,low}$
$V_{OCP1,init}$	Initial *CS* pin maximum voltage limit for the input voltage measurement pulse before startup	0.3 V	Refer GUI	$V_{start,OCP1}$

Table 5 Configurable parameters for protections

Symbol	Basic description	Example	Minimum value	Maximum value
$t_{auto,restart}$	Auto-restart time	1.2 s	0.4 s	4 s
$V_{OCP1,at,V,in,low}$	Regulated mode *CS* pin maximum voltage limit at lowest operational input voltage ($V_{in,low}$)	0.52 V	Refer GUI	1.08 V

Table 5 Configurable parameters for protections (continued)

Symbol	Basic description	Example	Minimum value	Maximum value
$V_{OCP1,at,V,in,high}$	Regulated mode *CS* pin maximum voltage limit at highest operational input voltage ($V_{in,high}$)	0.40 V	Refer GUI	$V_{OCP1,at,V,in,low}$
$V_{in,low}$	Lowest operational input voltage (rms in case of AC input)	82 V	V_{inUV}	$V_{in,high}$
$V_{in,high}$	Highest operational input voltage (rms in case of AC input)	326 V	$V_{in,low}$	V_{inOV}
t_{CSOCP2}	MOSFET overcurrent protection blanking time	240 ns	100 ns	Refer GUI
$Reaction_{OVP,Vout}$	Output overvoltage protection reaction	Auto-Restart	Auto-Restart	Latch-Mode
V_{outOV}	Output overvoltage protection threshold	65 V	$V_{out,start}$	Refer GUI
$EN_{UVP,Vout}$	Enable switch for regulated mode output undervoltage protection	Enabled	Enabled	Disabled
$Reaction_{UVP,Vout}$	Regulated mode output undervoltage protection reaction	Auto-Restart	Auto-Restart	Latch-Mode
V_{outUV}	Regulated mode output undervoltage protection threshold	33 V	Refer GUI	Refer GUI
$t_{VoutUV,blank}$	Blanking time for regulated mode output undervoltage protection	500 ms	5 ms	1000 ms
$EN_{OVP,In}$	Enable switch for maximum input voltage startup check and input overvoltage protection	Enabled	Enabled	Disabled
$EN_{UVP,In}$	Enable switch for minimum input voltage startup check and input undervoltage protection	Enabled	Enabled	Disabled
$EN_{VIN,ABM}$	Enable switch for ***ABM*** input voltage protections	Enabled	Enabled	Disabled
V_{inOV}	Input overvoltage protection threshold (rms in case of AC input)	350 V	$V_{in,start,max}$	Refer GUI
$V_{in,start,max}$	Maximum input voltage for startup (rms in case of AC input)	325 V	$V_{in,start,min}$	V_{inOV}
$V_{in,start,min}$	Minimum input voltage at startup (rms in case of AC input)	82 V	V_{inUV}	$V_{in,start,max}$
V_{inUV}	Input undervoltage protection threshold (rms in case of AC input)	70 V	Refer GUI	$V_{in,start,min}$
$t_{on,max,at,V,in,UV}$	Maximum on-time at input undervoltage protection threshold	13 µs	Refer GUI	$t_{on,max,at,V,in,low}$
$Reaction_{VCC,OVP}$	*VCC* overvoltage protection reaction	Latch-Mode	Auto-Restart	Latch-Mode
$V_{VCC,max}$	*VCC* overvoltage protection threshold	23 V	23 V	24.9 V
$EN_{VCC,UVP}$	Enable switch for regulated mode *VCC* undervoltage protection	Enabled	Enabled	Disabled
$V_{VCC,min}$	Regulated mode *VCC* undervoltage protection threshold	7.5 V	7.5 V	11 V
$T_{critical}$	Temperature threshold for IC overtemperature protection	119°C	Refer GUI	143°C

Table 5 Configurable parameters for protections (continued)

Symbol	Basic description	Example	Minimum value	Maximum value
$Debug_{Mode}$	Enable switch for debug mode	Disabled	Enabled	Disabled

Table 6 Configurable parameters for multimode

Symbol	Basic description	Example	Minimum value	Maximum value
$R_{FB,pull,up}$	*FB* pin internal pull-up resistor value	5.5 kohm	2.25 kohm	7.5 kohm
$N_{quality}$	Quality factor of the notch filter	1.6	0	2.0
$n_{notch,blank}$	Number of operation cycles as a timeout between the line synchronization being established and the notch filter output being applied as the filtered feedback voltage. [1)]	2	1	10
$f_{sw,max}$	Maximum switching frequency when $V_{FB,filtered}$ is $V_{FB,sw}$ or more	247.2 kHz	26.9 kHz	Refer GUI
$t_{on,min}$	Minimum on-time $t_{on,min}(V_{in})$ value when $t_{on,min,V,out,sense}(V_{in})$ is lower than $t_{on,min}$	1.38 µs	Refer GUI	$t_{on,max,at,V,in,low}$
$t_{min,demag}$	Minimum transformer demagnetizing time value used for $t_{on,min,V,out,sense}(V_{in})$ variable calculation internally	2.0 µs	2.0 µs	5.0 µs
$t_{on,max,at,V,in,low}$	Maximum on-time when V_{in} is $V_{in,low}$	15 µs	Refer GUI	30 µs
$EN_{Burst,Exit,Filter,Feedback}$	Enable switch for ABM burst exit based on the filtered feedback voltage	Enabled	Enabled	Disabled
f_{burst}	ABM burst frequency	130 Hz	130 Hz	1000 Hz
$n_{ABM,min}$	Minimum number of pulses per burst in ABM	3	3	Refer GUI
$t_{on,min,ABM}$	Minimum on-time in ABM	1 µs	Refer GUI	$t_{on,min}$
$t_{ABM,blank}$	Timeout for ABM entrance	6.5 ms	0 ms	Refer GUI
n_{wakeup}	Number of scheduler intervals between wakeup and start of the burst	1	1	20
$N_{valley,max}$	Maximum valley number	14	3	14
$N_{valley,fast}$	Valley number difference which triggers the fast valley adaptation	9	1	$N_{valley,max}$ - 1
$N_{valley,min,at,V,in,high}$	Minimum valley number at highest operational input voltage ($V_{in,high}$)	4	1	$N_{valley,max}$ - 1
$c_{valley,comp}$	On time compensation factor for every valley change	3.00	0.01	5.00
$V_{FB,valley,1}$	Feedback voltage for the end of the valley mapping (valley 1)	1.5 V	Refer GUI	$V_{FB,max,map}$
$V_{FB,max,map}$	$V_{FB,filtered}$ threshold which represents the maximum power transfer of the system	2.0 V	Refer GUI	2.403 V

1 It is essential for the notch filter to have line synchronization in order to work properly. This timeout enables the notch filter to converge. During this timeout, a low pass filter is used as the feedback voltage filtration.

Table 6 Configurable parameters for multimode (continued)

Symbol	Basic description	Example	Minimum value	Maximum value
$V_{FB,sw}$	$V_{FB,filtered}$ threshold for the end of the maximum switching frequency ramp up	2.0 V	0.8 V	2.2 V
$V_{FB,min}$	$V_{FB,filtered}$ threshold which represents the minimum power transfer of the system	0.3 V	0.2 V	0.5 V
$V_{FB,limit,step}$	Voltage step size of filtered feedback voltage max. limit $V_{FB,filtered,max}$ ramp	800 mV	Refer GUI	Refer GUI

Table 7 Configurable parameters for power factor correction

Symbol	Basic description	Default	Minimum value	Maximum value
C_{EMI}	Input current displacement compensation gain parameter for enhanced PFC	0.16 µF	0 µF	1 µF
$V_{EPFC,on}$	$V_{FB,filtered}$ threshold for C_{EMI} gain reduction towards $V_{FB,filtered}$ = 0.8 V	1.0 V	0.8 V	2.403 V

Table 8 Configurable parameters for UART reporting

Symbol	Basic description	Default	Minimum value	Maximum value
$EN_{UART,REPORTING}$	Enable switch for UART reporting	Enabled	Enabled	Disabled
$EN_{SEND,LAST,ERROR,CODE}$	Enable switch for error code signal transmission	Enabled	Enabled	Disabled
$EN_{SEND,V,IN,LOSS}$	Enable switch for input voltage loss signal transmission	Enabled	Enabled	Disabled
$UART_{POLARITY}$	Idle level of the UART reporting bus	Low	Low	High

Table 9 Configurable parameters for fine tuning

Symbol	Basic description	Default	Minimum value	Maximum value
t_{ZCDPD}	*ZCD* pin propagation delay compensation parameter	370 ns	0 ns	1000 ns
R_{in}	DC link filter capacitor voltage ripple compensation parameter to improve input voltage estimation accuracy	10.5 Ω	0 Ω	30 Ω
EN_{ETHDC}	Enable switch for Enhanced THD correction	Enabled	Enabled	Disabled
c_{dither}	Percentage of switching parameter modulation for switching frequency dithering with a constant DC input voltage	10%	0%	20%

Table 10 Configurable parameters for user ID

Symbol	Basic description	Default	Minimum value	Maximum value
$User_{ID,A}$	User ID A	0	-	-

4 List of Parameters

List of Fixed Parameters

Table 11 Fixed parameters for hardware configuration

Symbol	Basic description	Default	Minimum value	Maximum value
$V_{}$	Secondary main output diode forward voltage assumption for output voltage estimation	0.7 V	-	-
V_{GD}	*GD* pin peak voltage	12 V	-	-

Table 12 Fixed parameters for protections

Symbol	Basic description	Default	Minimum value	Maximum value
$t_{start,max}$	Maximum allowable duration for startup phase	967 * C_{VCC}	-	-
$T_{start,max}$	Maximum IC junction temperature for startup	$T_{critical}$ - 4°C	-	-

Table 13 Fixed parameters for startup

Symbol	Basic description	Default	Minimum value	Maximum value
t_{ss}	Soft start time step	0.5 ms	-	-
$V_{FB,limit,start}$	Start voltage for filtered feedback voltage max. limit $V_{FB,filtered,max}$ ramp	1.2 V	-	-

Table 14 Fixed parameters for multimode

Symbol	Basic description	Default	Minimum value	Maximum value
$V_{FB,ABM}$	$V_{FB,filtered}$ threshold for the ABM/***DCM*** transition	0.8 V	-	-
$V_{FB,on}$	$V_{FB,filtered}$ threshold for the start of the on-time ramp up	0.8 V	-	-
$f_{sw,min}$	Minimum switching frequency	26.9 kHz	-	-

Table 15 Fixed parameters for power factor correction

Symbol	Basic description	Default	Minimum value	Maximum value
$t_{on,min,EPFC}$	Minimum on time for enhanced ***PFC*** modulation	$t_{CS,LEB}$ + $24/f_{MCLK}$	-	-
$t_{on,max,EPFC}$	Maximum on time for enhanced PFC modulation	$t_{on,max,at,V,in,low}$	-	-

Table 16 Other fixed parameters

Symbol	Basic description	Default	Minimum value	Maximum value
$t_{CS,LEB}$	*CS* leading edge blanking time	480 ns	-	-
$t_{ZCD,ring}$	*ZCD* ringing suppression	1.2 µs	-	-
t_{pw}	Discharge pulse duration	1.5 µs	-	-

Table 16 Other fixed parameters (continued)

Symbol	Basic description	Default	Minimum value	Maximum value
$n_{OSC,ZCD}$	Selection of zero-crossings for the oscillation period measurement at pre-startup	Second and Third zero-crossings	-	-
$T_{OSC,max}$	Maximum limit of the measured oscillation period (If exceeded at pre-startup, $T_{OSC,preset}$ is used; If exceeded after startup, the last valid measured oscillation period is used)	6.6 µs	-	-
$T_{OSC,preset}$	Oscillation period used by the controller if the measured oscillation period at pre-startup exceeds $T_{OSC,max}$	3.3 µs	-	-

5 Electrical Characteristics and Parameters

All signals are measured with respect to the ground pin, GND. The voltage levels are valid provided other ratings are not violated.

5.1 Package Characteristics

Table 17 Package Characteristics

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Thermal resistance for PG-DSO-8-58	R_{thJA}	—	178	K/W	JEDEC 1s0p for 140 mW power dissipation

5.2 Absolute Maximum Ratings

Attention: ***Stresses above the values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. These values are not tested during production test.***

Table 18 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Voltage externally supplied to pin VCC	V_{VCCEXT}	–0.5	26	V	voltage that can be applied to pin VCC by an external voltage source
Voltage at pin GDx	V_{GDx}	–0.5	V_{VCC} + 0.3	V	if gate driver is not configured for digital I/O
Junction temperature	T_J	–40	125	°C	$f_{sw,max} \leq 247.2$ kHz
Junction temperature	T_J	–40	150	°C	[2] $f_{sw,max} \leq 186.4$ kHz
Storage temperature	T_S	–55	150	°C	
Soldering temperature	T_{SOLD}	—	260	°C	Wave Soldering [3]
Latch-up capability	I_{LU}	—	150	mA	[4] Pin voltages acc. to abs. max. ratings
ESD capability HBM	V_{HBM}	—	1500	V	[5]
ESD capability CDM	V_{CDM}	—	500	V	[6]

2 The device guarantees general functionality between 125°C and 150°C. A degradation of performance may apply.
3 According to JESD22-A111 Rev A.
4 Latch-up capability according to JEDEC JESD78D, T_A= 85°C.
5 ESD-HBM according to ANSI/ESDA/JEDEC JS-001-2012.
6 ESD-CDM according to JESD22-C101F.

Table 18 Absolute Maximum Ratings (continued)

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Input Voltage Limit	V_{pin_DC}	-0.5	3.6	V	Voltage externally supplied to pins FB, CS, ZCD, UART (If not stated different)
Maximum permanent negative clamping current for ZCD and CS	$-I_{CLN\_DC}$	—	2.5	mA	RMS
Maximum transient negative clamping current for ZCD and CS	$-I_{CLN\_TR}$	—	10	mA	pulse < 500ns
Maximum negative transient input voltage for ZCD	$-V_{IN\_ZCD}$	—	1.5	V	pulse < 500ns
Maximum negative transient input voltage for CS	$-V_{IN\_CS}$	—	3.0	V	pulse < 500ns
Maximum permanent positive clamping current for CS	I_{CLP_DC}	—	2.5	mA	RMS
Maximum transient positive clamping current for CS	I_{CLP_TR}	—	10	mA	pulse < 500ns
Maximum current into pin VIN	I_{AC}	—	10	mA	for charging operation
Maximum sum of input clamping high currents for digital input stages of device	I_{CLH_sum}	—	300	µA	limits for each individual digital input stage have to be respected
Voltage at HV pin	V_{HV}	-0.5	600	V	

5.3 Operating Conditions

The recommended operating conditions are shown for which the DC Electrical Characteristics are valid.

Table 19 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Ambient temperature	T_A	–40	85	°C	
Junction Temperature	T_J	–40	125	°C	max. 66 MHz f_{MCLK}
Lower VCC limit	V_{VCC}	V_{UVOFF}	—	V	device is held in reset when $V_{VCC} < V_{UVOFF}$
Voltage externally supplied to VCC pin	V_{VCCEXT}	—	24	V	maximum voltage that can be applied to pin VCC by an external voltage source
Gate driver pin voltage	V_{GD}	–0.5	V_{VCC} + 0.3	V	
Line frequency	f_{in}	45	66	Hz	

5.4 DC Electrical characteristics

The electrical characteristics provide the spread of values applicable within the specified supply voltage and junction temperature range, T_J from -40 °C to +150 °C. Any necessary differentiation in value between $T_j \leq 125$ °C and $T_j > 125$ °C is explicitly shown.

Values have been verified either with simulation models up to $T_j = 150$ °C or by device characterization up to 140 °C.

Typical values represent the median values related to $T_A = 25$ °C. All voltages refer to GND, and the assumed supply voltage is $V_{VCC} = 18$ V if not otherwise specified.

Note: Not all values given in the tables are tested during production testing. Values not tested are explicitly marked.

Table 20 Power supply characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VCC_ON threshold	V_{VCCon}	—	V_{SELF}	—	V	Self-powered startup (default)
VCC_ON_SELF threshold	V_{SELF}	19	20.5	22	V	$dV_{VCC}/dt = 0.2$ V/ms
VCC_ON_SELF delay	t_{SELF}	—	—	2.1	µs	Reaction time of V_{VCC} monitor
VCC_UVOFF current	$I_{VCCUVOFF}$	5	20	40	µA	$V_{VCC} < V_{SELF}$(min) - 0.3 V or $V_{VCC} < V_{EXT}$(min) - 0.3 V[7)]
UVOFF threshold	V_{UVOFF}	—	6.0	—	V	SYS_CFG0.SELUVTHR = 0_B
UVOFF threshold tolerance	Δ_{UVOFF}	—	—	±5	%	This value defines the tolerance of V_{UVOFF}
UVOFF filter constant	t_{UVOFF}	600	—	—	ns	1V overdrive
UVLO (UVWAKE) threshold	V_{UVLO}	—	V_{UVOFF} · 1.25	—	V	
UVWAKE threshold tolerance	Δ_{UVLO}	—	—	±5	%	This value defines the tolerance of V_{UVLO}
UVLO (UVWAKE) filter constant	t_{UVLO}	0.6	—	2.2	µs	1 V overdrive
OVLO (OVWAKE) threshold	V_{OVLO}	—	V_{SELF}	—	V	
OVLO (OVWAKE) filter constant	t_{OVLO}	0.6	—	2.4	µs	1 V overdrive
VDDP voltage	V_{VDDP}	3.04	3.20	3.36	V	At PMD0/PSMD1. Some internal values refer to V_{VDDP} / V_{VDDA}

7 Tested at $V_{VCC} = 5.5$ V

Table 20 Power supply characteristics (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
						and V_{VDDPPS} / V_{VDDAPS} respectively.
VDDA voltage	V_{VDDA}	3.20	3.31	3.42	V	At PMD0/PSMD1. Some internal values refer to V_{VDDP} / V_{VDDA} and V_{VDDPPS} / V_{VDDAPS} respectively.
Nominal range 0% to 100%	V_{ADCVCC}	0	—	V_{REF}	V	$V_{ADCVCC} = 0.09 \cdot V_{VCC}$ [8]
Reduced VCC range for ADC measurement	R_{ADCVCC}	8	—	92	%	[9][10]
Maximum error for ADC measurement (8-bit result)	$TET0_{VCC}$	—	—	3.8	LSB_8	
Maximum error for ADC measurement (8-bit result)	$TET256_{VCC}$	—	—	5.2	LSB_8	
Gate driver current consumption excl. gate charge current	I_{VCCGD}	—	0.26	0.35	mA	$T_j \leq 125°C$
Gate driver current consumption excl. gate charge current	I_{VCCGD}	—	—	0.5	mA	$T_j > 125°C$
VCC quiescent current in PMD0	$I_{VCCPMD0}$	—	3.5	4.7	mA	All registers have reset values, clock is active, CPU is stopped
VCC quiescent current in PSMD2	$I_{VCCPSMD2}$	—	0.3	0.48	mA	$T_j \leq 85$ °CWU_PWD_CFG = $2C_H$
VCC quiescent current in PSMD2	$I_{VCCPSMD2}$	—	—	1.2	mA	$T_j \leq 125$ °CWU_PWD_CFG = $2C_H$
VCC quiescent current in PSMD2	$I_{VCCPSMD2}$	—	—	1.8	mA	$T_j > 125$ °CWU_PWD_CFG = $2C_H$
VCC quiescent current in power saving mode PSDM4 with standby logic active	$I_{VCCPSMD4}$	—	0.13	0.18	mA	$T_j \leq 125$ °C WU_PWD_CFG = 00_H

8 Theoretical minimum value, real minimum value is related to V_{UVOFF} threshold.
9 Operational values.
10 Note that the system is turned off if $V_{VCC} < V_{UFOFF}$.

Table 20 Power supply characteristics (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VCC quiescent current in power saving mode PSDM4 with standby logic active	$I_{VCCPSMD4}$	—	—	0.25	mA	T_j >125 °C WU_PWD_CFG = 00_H

Table 21 Electrical characteristics of the GD pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input clamping current, low	$-I_{CLL}$	—	—	100	µA	only digital input
Input clamping current, high	I_{CLH}	—	—	100	µA	only digital input
APD low voltage (active pull-down while device is not powered or gate driver is not enabled)	V_{APD}	—	—	1.6	V	I_{GD} = 5 mA
R_{PPD} value	R_{PPD}	—	600	—	kΩ	Permanent pull-down resistor inside gate driver
R_{PPD} tolerance	Δ_{PPD}	—	—	±25	%	Permanent pull-down resistor inside gate driver
Driver output low impedance	R_{GDL}	—	—	7.0	Ω	$T_J \leq 125$ °C, I_{GD} = 0.1 A
Driver output low impedance	R_{GDL}	—	—	7.5	Ω	T_J > 125 °C, = 0.1 A
Nominal output high voltage in PWM mode	V_{GDH}	—	12	—	V	GDx_CFG.VOL = 2, I_{GDH} = –1 mA
Output voltage tolerance	Δ_{VGDH}	—	—	±5	%	Tolerance of programming options if V_{GDH} > 10 V, I_{GDH} = –1 mA
Rail-to-rail output high voltage	V_{GDHRR}	V_{VCC}– 0.5	—	V_{VCC}	V	If V_{VCC} < programmed V_{GDH} and output at high state
Output high current in PWM mode for GD0	$-I_{GDH}$	—	100	—	mA	GDx_CFG.CUR = 8
Output high current tolerance in PWM mode	Δ_{IGDH}	—		±15	%	Calibrated [11)]

11 referred to GDx_CFG.CUR = 16

Table 21 Electrical characteristics of the GD pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Discharge current for GD0	I_{GDDIS}	800	—	—	mA	V_{GD} = 4 V and driver at low state
Output low reverse current	$-I_{GDREVL}$	—	—	100	mA	Applies if V_{GD} < 0 V and driver at low state
Output high reverse current in PWM mode	I_{GDREVH}	—	1/6 of I_{GDH}	—		Applies if $V_{GD} > V_{GDH}$ + 0.5 V (typ) and driver at high state

Table 22 Electrical characteristics of the CS pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage operating range	V_{INP}	–0.5	—	3.0	V	
OCP2 comparator reference voltage, derived from V_{VDDA}, given values assuming $V_{VDDA} = V_{VDDA,typ}$	V_{OCP2}	—	1.6	—	V	SYS_CFG0.OCP2 = 00_B
OCP2 comparator reference voltage, derived from V_{VDDA}, given values assuming $V_{VDDA} = V_{VDDA,typ}$	V_{OCP2}	—	1.2	—	V	SYS_CFG0.OCP2 = 01_B
OCP2 comparator reference voltage, derived from V_{VDDA}, given values assuming $V_{VDDA} = V_{VDDA,typ}$	V_{OCP2}	—	0.8	—	V	SYS_CFG0.OCP2 = 10_B
OCP2 comparator reference voltage, derived from V_{VDDA}, given values assuming $V_{VDDA} = V_{VDDA,typ}$	V_{OCP2}	—	0.6	—	V	SYS_CFG0.OCP2 = 11_B
Threshold voltage tolerance	Δ_{VOCP2}	—	—	±5	%	Voltage divider tolerance
Comparator propagation delay	t_{OCP2PD}	15	—	35	ns	
Minimum comparator input pulse width	t_{OCP2PW}	—	—	30	ns	
OCP2F comparator propagation delay	$t_{OCP2FPD}$	70	—	170	ns	dV_{CS}/dt = 100 V/µs

Table 22 Electrical characteristics of the CS pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Delay from V_{CS} crossing V_{CSOCP2} to begin of GDx turn-off (I_{GD0} > 2mA)	$t_{CSGDxOCP2}$	125	135	190	ns	dV_{CS}/dt = 100 V/µs; f_{MCLK} = 66 MHz. GDx driven by QR_GATE FIL_OCP2.STABLE = 3
OCP1 operating range	V_{OCP1}	0	—	$V_{REF}/2$	V	RANGE =00_B
OCP1 threshold at full scale setting (CS_OCP1LVL=FF_H)	V_{OCP1FS}	1187	1209	1243	mV	RANGE =00_B
Delay from V_{CS} crossing V_{CSOCP1} to CS_OCP1 rising edge, 1.2 V range	t_{CSOCP1}	90	170	250	ns	Input signal slope dV_{CS}/dt = 150 mV/µs. This slope represents a use case of a switch-mode power supply with minimum input voltage.
Delay from CS_OCP1 rising edge to QR_GATE falling edge	$t_{OCP1GATE}$	—	—	130	ns	
Delay from QR_GATE falling edge to start of GDx turn-off	$t_{GATEGDx}$	1	3	5	ns	GDx driven by QR_GATE. Measured up to I_{GDx} > 2 mA
OCP1 comparator input single pulse width filter	t_{OCP1PW}	60	—	95	ns	Shorter pulses than min. are suppressed, longer pulses than max. are passed
Nominal S&H operating range 0% to 100%	V_{CSH}	0	—	$V_{REF}/2$	V	CS_ICR.RANGE =00_B
Reduced S&H operating range	RR_{CVSH}	8	—	92	%	CS_ICR.RANGE =00_B Operational values
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET0_{CS0S}$	—	—	4.7	LSB	CS_ICR.RANGE =00_B
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET256_{CS0S}$	—	—	6.0	LSB	CS_ICR.RANGE =00_B
Nominal S&H operating range 0% to 100%	V_{CSH}	0	—	$V_{REF}/6$	V	CS_ICR.RANGE =11_B
Reduced S&H operating range	RR_{CVSH}	20	—	80	%	CS_ICR.RANGE =11_B Operational values

Table 22 Electrical characteristics of the CS pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET0_{CS0S}$	—	—	8.0	LSB	CS_ICR.RANGE =11_B
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET256_{CS0S}$	—	—	8.7	LSB	CS_ICR.RANGE =11_B
S&H delay of input buffer	t_{CSHST}	—	—	510	ns	Referring to jump in input voltage. Limits the minimum gate driver T_{on} time.

Table 23 Electrical characteristics of the ZCD pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage operating range	V_{INP}	–0.5	—	3.3	V	
Input clamping current, high	I_{CLH}	—	—	100	µA	
Zero-crossing threshold	V_{ZCTHR}	15	40	70	mV	
Comparator propagation delay	t_{ZCPD}	30	50	70	ns	dV_{ZCD}/dt = 4 V/µs
Input voltage negative clamping level	$-V_{INPCLN}$	140	180	220	mV	Analog clamp activated
Nominal I/V-conversion operating range 0% to 100%	$-I_{IV}$	0	—	0.5	mA	CRNG =11_BGain = 4800 mV/mA
Nominal I/V-conversion operating range 0% to 100%	$-I_{IV}$	0	—	1	mA	CRNG =10_BGain = 2400 mV/mA
Nominal I/V-conversion operating range 0% to 100%	$-I_{IV}$	0	—	2	mA	CRNG =01_BGain = 1200 mV/mA
Nominal I/V-conversion operating range 0% to 100%	$-I_{IV}$	0	—	4	mA	CRNG =00_B Gain = 600 mV/mA
Reduced I/V-conversion operating range	RR_{IV}	5	—	80	%	

Table 23 Electrical characteristics of the ZCD pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Overall tolerance of the ZCD IV measurement	ΔI_{IV}	-4.7	—	4.7	%	T<125°C, $-I_{IV}$ >375 µA , by design, not ensured by production test
Maximum deviation between ZCD clamp voltage and trim result stored in OTP	E_{ZCDClp}	—	—	±5	%	$-I_{IV}$ > 0.25 mA
IV-conversion delay of input buffer	t_{IVST}	—	—	900	ns	Refers to jump in input current[12)]
Nominal S&H input voltage range 0% to 100%	V_{ZSH}	0	—	$2/3 \cdot V_{REF}$	V	SHRNG =0_B
Nominal S&H input voltage range 0% to 100%	V_{ZSH}	V_{REF} /2	—	$7/6 \cdot V_{REF}$	V	SHRNG =1_B
Reduced S&H input voltage range	RR_{ZVSH}	4	—	95	%	
Maximum error for corrected ADC measurement (8-bit result)	$TET0_{ZVS0}$	—	—	3.7	LSB_8	SHRNG =0_B
Maximum error for corrected ADC measurement (8-bit result)	$TET256_{ZVS0}$	—	—	4.9	LSB_8	SHRNG =0_B
Maximum error for corrected ADC measurement (8-bit result)	$TET0_{ZVS1}$	—	—	4.2	LSB_8	SHRNG =1_B
Maximum error for corrected ADC measurement (8-bit result)	$TET256_{ZVS1}$	—	—	5.8	LSB_8	SHRNG =1_B
S&H delay of input buffer referring to jump of input voltage	t_{ZSHST}	—	—	1.0	µs	SHRNG =0_B $T_j \leq$ 125 °C
S&H delay of input buffer referring to jump of input voltage	t_{ZSHST}	—	—	1.2	µs	SHRNG =0_B T_j > 125 °C

12 Limits the minimum gate driver T_{on} time.

Table 23 Electrical characteristics of the ZCD pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
S&H delay of input buffer referring to jump of input voltage	t_{ZSHST}	—	—	1.6	µs	SHRNG =1_B $T_j \leq 125$ °C
S&H delay of input buffer referring to jump of input voltage	t_{ZSHST}	—	—	1.8	µs	SHRNG =1_B $T_j > 125$ °C

Table 24 Electrical characteristics of the HV pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Current for V_{CC} cap charging	I_{LD}	3.0	5	7.5	mA	V_{HV} = 30 V; $V_{VCC} < V_{VCCon}$ – 0.3 V; $T_j \geq 0$°C
Current for V_{CC} cap charging	I_{LD}	2.4	5	7.5	mA	V_{HV} = 30 V; $V_{VCC} < V_{VCCon}$ – 0.3 V;-25°C < T_j < 0°C
Current for V_{CC} cap charging	I_{LD}	2.0	5	7.5	mA	V_{HV} = 30 V; $V_{VCC} < V_{VCCon}$ – 0.3 V;T_j < -25°C
Nominal current for measurement path 0% to 100%	I_{MEAS}	0	—	9.6	mA	CURRNG = 11_B
Nominal current for measurement path 0% to 100%	I_{MEAS}	0	—	4.8	mA	CURRNG = 10_B
Nominal current for measurement path 0% to 100%	I_{MEAS}	0	—	1.6	mA	CURRNG = 01_B
Comparator threshold (in % of full range of I_{MEAS})	THR_{COMP}	15	20	25	%	COMPTHR= 00_B
Comparator threshold (in % of full range of I_{MEAS})	THR_{COMP}	25	30	35	%	COMPTHR= 01_B
Comparator threshold (in % of full range of I_{MEAS})	THR_{COMP}	45	50	55	%	COMPTHR= 11_B

Table 25 Electrical characteristics of the FB pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
MFIO reference voltage	$V_{MFIOREF}$	—	V_{REF}	—	V	Selection = V_{REF}
Nominal range 0% to 100%	V_{MFIO}	0	—	V_{REF}	V	Gain = 1

Table 25 Electrical characteristics of the FB pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Reduced operating range	RR_{VMFIO}	4	—	96	%	Gain = 1. Operational values.
Maximum error for corrected measurement (8-bit result)	$TET0_{MFI0}$	—	—	4.0	LSB_8	Gain = 1
Maximum error for corrected measurement (8-bit result)	$TET256_{MFI0}$	—	—	4.8	LSB_8	Gain = 1
Delay of input buffer	t_{MFIOST}	—	—	2.7	µs	Refers to jump in input voltage 0% to 90%. Applicable for MFIO0 and MFIO1 only.
Pull-up resistor tolerance	Δ_{RPU}	—	—	±20	%	Overall tolerance

Table 26 Electrical characteristics of the UART pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input clamping current, low	$-I_{CLL}$	—	—	100	µA	only digital input
Input clamping current, high	I_{CLH}	—	—	100	µA	only digital input
Input capacitance	C_{INPUT}	—	—	25	pF	
Input low voltage	V_{IL}	—	—	1.0	V	
Input high voltage	V_{IH}	2.1	—	—	V	
Input low current with active weak pull-up WPU	$-I_{LPU}$	30	—	90	µA	Measured at max. V_{IL}
Max. input frequency	f_{INPUT}	15	—	—	MHz	
Output low voltage	V_{OL}	—	—	0.8	V	I_{OL} = 2 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –2 mA
Output sink current	I_{OL}	—	—	2	mA	
Output source current	$-I_{OH}$	—	—	2	mA	
Output rise time (0 → 1)	t_{RISE}	—	—	50	ns	20 pF load, push/pull output
Output fall time (1 → 0)	t_{FALL}	—	—	50	ns	20 pF load, push/pull or open-drain output
Max. output switching frequency	f_{SWITCH}	10	—	—	MHz	

Table 26 Electrical characteristics of the UART pin (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
UART baudrate for parameter configuration	f_{UART}	-10%	57600	+10%	baud	
UART baudrate for reporting	$f_{UART,report}$	-10%	9600	+10%	baud	

Table 27 Electrical characteristics of the A/D converter

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Integral non-linearity	INL	—	—	1	LSB_8	13)

Table 28 Electrical characteristics of the reference voltage

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Reference voltage	V_{REF}	—	2.428	—	V	
VREF overall tolerance	Δ_{VREF}	—	—	±1.5	%	Trimmed, $T_j \leq 125$ °C and aging
VREF overall tolerance	Δ_{VREF}	—	—	±2.0	%	Trimmed, full temperature range and aging

Table 29 Electrical characteristics of the OTP programming

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
OTP programming voltage at the VCC pin for range $C000_H$ to $CFFF_H$	V_{PP}	7.35	7.5	7.65	V	Operational values
OTP programming current	I_{PP}	—	1.6	—	mA	Programming of 4 bits in parallel

Table 30 Electrical characteristics of the clock oscillators

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Master clock oscillation period including all variations	t_{MCLK}	15.0	15.8	16.6	ns	In reference to 66 MHz f_{MCLK}

13 ADC capability measured via channel MFIO without errors due to switching of neighbouring pins, e.g. gate drivers, measured with STC = 5. MFIO buffer non-linearity masked out by taking ADC output values ≥ 30 only.

Table 30 Electrical characteristics of the clock oscillators (continued)

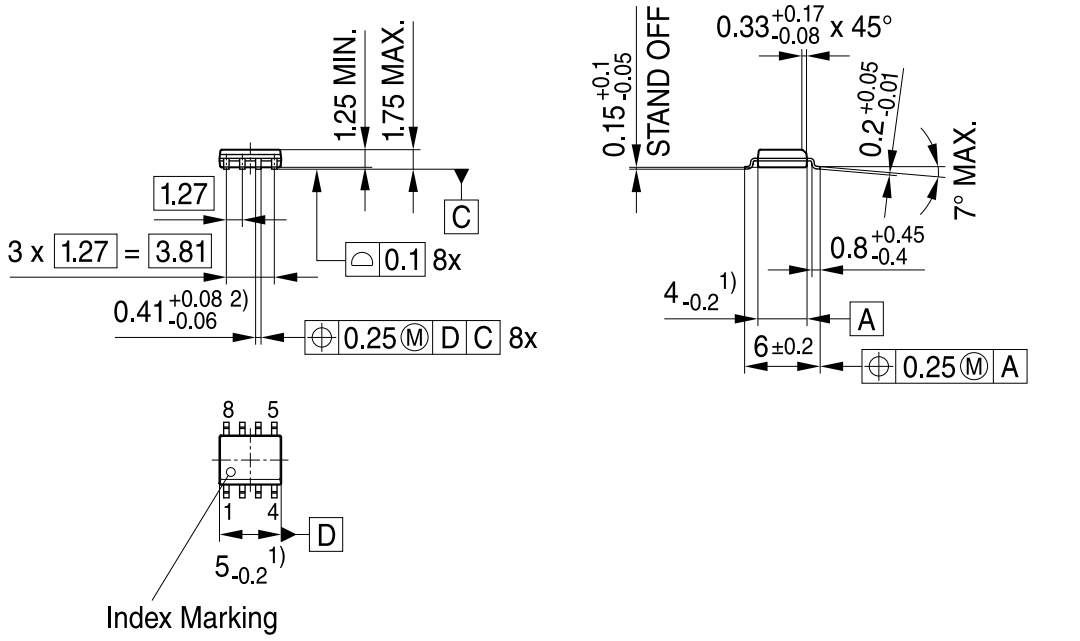
Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Main clock oscillator frequency variation of stored DPARAM frequency	Δ_{MCLK}	–3.2	—	+3.5	%	Temperature drift and aging only, 66 MHz f_{MCLK}
Standby clock oscillator frequency	f_{STBCLK}	96	100	104	kHz	Trimming tolerance at T_A = 25 °C
Standby clock oscillator frequency	f_{STBCLK}	90	100	110	kHz	Overall tolerance, $T_j \leq$ 125 °C
Standby clock oscillator frequency	f_{STBCLK}	85	100	110	kHz	Overall tolerance, T_j >125 °C

Table 31 Electrical characteristics of the temperature sensor

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Temperature sensor ADC output operating range	ADC_{TEMP}	0	—	190	LSB	ADC_{TEMP} = 40 + temperature / °C)
Temperature sensor tolerance	Δ_{TEMP}	—	—	±6	K	Incl. ADC conversion accuracy at 3 σ

6 Package Dimensions

The package dimensions of PG-DSO-8 are provided.



1) Does not include plastic or metal protrusion
2) Does not include dambar protrusion of 0.127 max. in excess of the lead width dimension

PG-DSO-8-41, -42, -51, -53, -58-PO V06

Figure 18 Package Dimensions for PG-DSO-8

Note: Dimensions in mm.

Note: You can find all of our packages, packing types and other package information on our Infineon Internet page “Products”: http://www.infineon.com/products.

7 References

1. Infineon: *XDPL8219 Design Guide*
2. Infineon: *XDPL8219 Reference Board Engineering Report*
3. Infineon: *CoolMOS P7 power MOSFETs*, ***http://www.infineon.com/P7***

8 Revision History

Major changes since previous revision

Revision History

Revision	Description
1.0	Initial version
1.1	***Figure 1***: Text improvement from "XDPL8219" to "Flyback Controller IC". ***Figure 4***: Correction of $t_{on,min}(V_{in})$ alignment with the reference point.

Glossary

ABM

Active Burst Mode (ABM)

Active Burst Mode is an operating mode of a switched-mode power supply for very light load conditions. The controller switches in bursts of pulses with a pause between bursts in which no switching is done.

ADC

Analog-to-Digital Converter (ADC)

An analog-to-digital converter is a device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.

BOM

Bill of Materials (BOM)

A bill of materials is a list of the raw materials, sub-assemblies, intermediate assemblies, sub-components, parts and the quantities of each needed to manufacture an end product.

CCM

Continuous Conduction Mode (CCM)

Continuous Conduction Mode is an operational mode of a switching power supply in which the current is continuously flowing and does not return to zero.

CRC

Cyclic Redundancy Check

A cyclic redundancy check is an error-detecting code commonly used to detect accidental changes to raw data.

CV

Constant Voltage (CV)

Constant Voltage is a mode of a power supply in which the output voltage is kept constant regardless of the load.

Glossary

DCM

Discontinuous Conduction Mode (DCM)

Discontinuous Conduction Mode is an operational mode of a switching power supply in which the current starts and returns to zero.

EMI

Electro-Magnetic Interference (EMI)

Also called Radio Frequency Interference (RFI), this is a (usually undesirable) disturbance that affects an electrical circuit due to electromagnetic radiation emitted from an external source. The disturbance may interrupt, obstruct, or otherwise degrade or limit the effective performance of the circuit.

FB

Flyback (FB)

A flyback converter is a power converter with the inductor split to form a transformer, so that the voltage ratios are multiplied with an additional advantage of galvanic isolation between the input and any outputs.

GUI

Graphic User Interface

A graphical user interface is a type of interface that allows users to interact with electronic devices through graphical icons and visual indicators.

HID

Human Interface Device (HID)

A Human Interface Device is a type of computer device that interacts directly with, and most often takes input from, humans and may deliver output to humans. The term HID most commonly refers to the USB-HID specification.

IC

Integrated Circuit (IC)

A miniaturized electronic circuit that has been manufactured in the surface of a thin substrate of semiconductor material. An IC may also be referred to as micro-circuit, microchip, silicon chip, or chip.

IIR

Infinite Impulse Response (IIR)

Infinite impulse response is a property applying to many linear time-invariant systems. Common examples of linear time-invariant systems are most electronic and digital filters. Systems with this property have an impulse response which does not become exactly zero past a certain point, but continues indefinitely.

OCP1

Overcurrent Protection Level 1 (OCP1)

The Overcurrent Protection Level 1 is limiting the current in a switched-mode power supply to limit the power delivered to the output of the power supply.

OTP

One-Time Programmable memory

A one-time programmable memory is a form of memory to which data can be written once. After writing, the data is stored permanently and cannot be further changed.

Glossary

PCB

Printed Circuit Board (PCB)

A Printed Circuit Board mechanically supports and electrically connects electronic components using conductive tracks, pads and other features etched from copper sheets laminated onto a non-conductive substrate.

PC

Personal Computer

A personal computer is a general-purpose computer whose size, capabilities, and original sale price make it useful for individuals, and which is intended to be operated directly by an end-user with no intervening computer time-sharing models that allowed larger, more expensive minicomputer and mainframe systems to be used by many people, usually at the same time.

PFC

Power Factor Correction (PFC)

Power factor correction increases the power factor of an AC power circuit closer to 1 which corresponds to minimizing the reactive power of the power circuit.

PF

Power Factor (PF)

Power factor is the ratio between the real power and the apparent power.

PWM

Pulse Width Modulation (PWM)

Pulse-width modulation is a technique to encode an analog value into the duty cycle of a pulsing signal with arbitrary amplitude.

QRM1

Quasi-Resonant Mode, switching in first valley (QRM1)

Quasi-Resonant Mode is an operating mode of a switched-mode power supply which maximizes efficiency. This is achieved by switching at the occurrence of the first valley of a signal which corresponds to a time when switching losses are low.

QRMn

Quasi-Resonant Mode, switching in valley n (QRMn)

Quasi-Resonant Mode is an operating mode of a switched-mode power supply which maximizes efficiency. This is achieved by switching at the occurence of an nth valley of a signal which corresponds to a time when switching losses are low.

RAM

Random Access Memory

Random-access memory is a form of computer data storage that allows data items to be read and written regardless of the order in which they are accessed.

SSR

Secondary Side Regulated (SSR)

A Secondary Side Regulated power supply is controls its operation based on feedback from the secondary side of an isolated power supply.

THD

Total Harmonic Distortion (THD)

The total harmonic distortion of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

UART

Universal Asynchronous Receiver Transmitter

A universal asynchronous receiver transmitter is used for serial communications over a peripheral device serial port by translating data between parallel and serial forms.

USB

Universal Serial Bus

Universal Serial Bus is an industry standard that defines cables, connectors and communications protocols used in a bus for connection, communication, and power supply between computers and electronic devices.

UVLO

Undervoltage Lockout (UVLO)

The Undervoltage-Lockout is an electronic circuit used to turn off the power of an electronic device in the event of the voltage dropping below the operational value.

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