i.MX6 SMART DEVICE SYSTEM

MCIMX6Q-SDB, MCIMX6Q-SDP, MCIMX6DL-SDP

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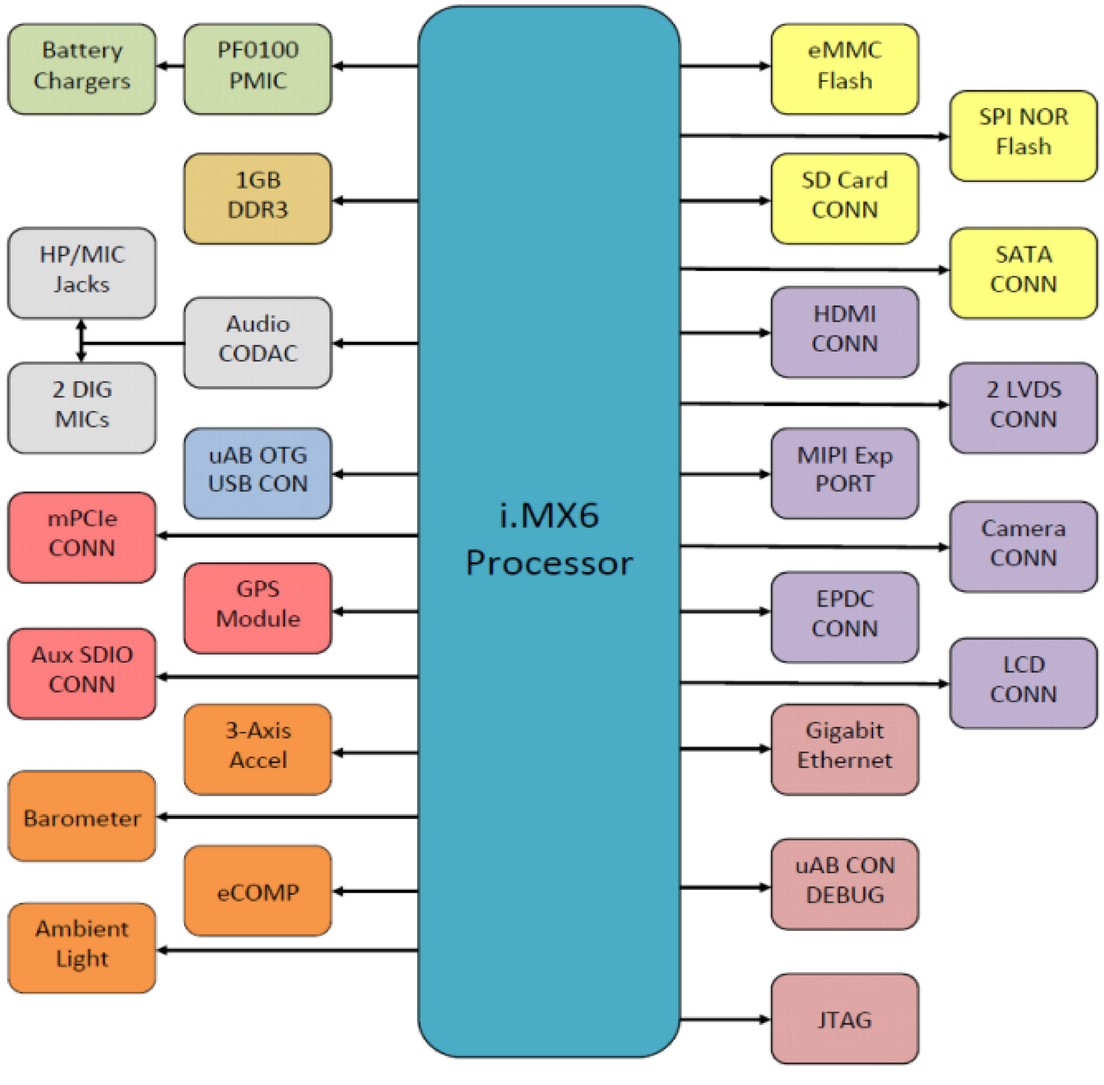
Smart Device System Block Diagram



GENERAL DESIGN NOTES

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/16 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are Tantalum
2. Critical compenents that require tolerances tighter than listed in Note 1are labeled with required tolerance on schematic. Non-critical components may be filled
3. Interrupted lines coded with the same letter or letter with tighter tolerance parts for BOM consolidation combinations are electrically connected. purposes, but may be changed to meet the general tolerances of Note 1 if desired.
4. Device type number is for reference only. The number varies with the manufacturer.
5. Special signal usage:
   _B or 'n' Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals
6. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

AC ADAPTER SPECIFICATIONS

DC Voltage Output: 5VDC
Current Output: ~ 5A (depending on application)
Polarity:
Inner Diameter: 2.1mm
Outer Diameter: 5.5mm

Revision History

Rev. Code	Date	Description

ICAP Classification FCP: ___ FIUO: ___ PUBI: X
Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM
Page Title: TITLE PAGE
Size: D | Document Number: SOURCE:SCH-27392 PDF:SPF-27392 | Rev: C3
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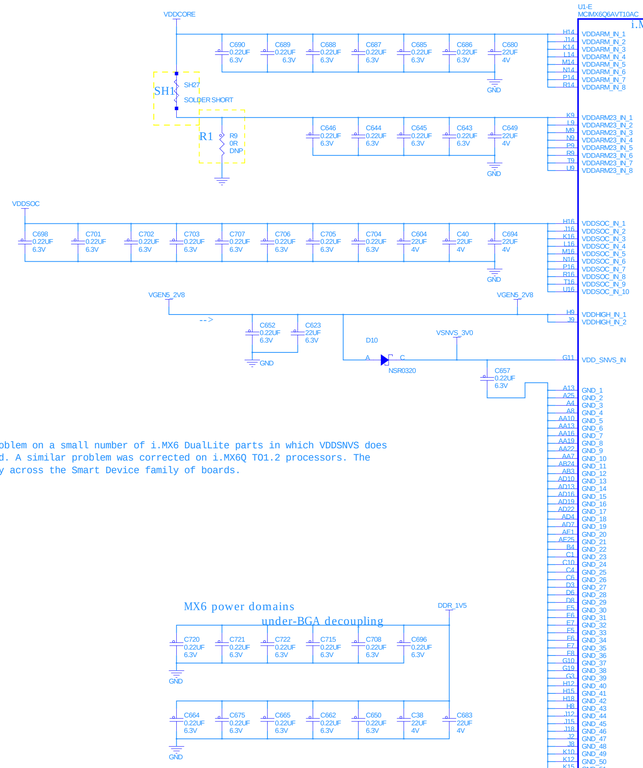
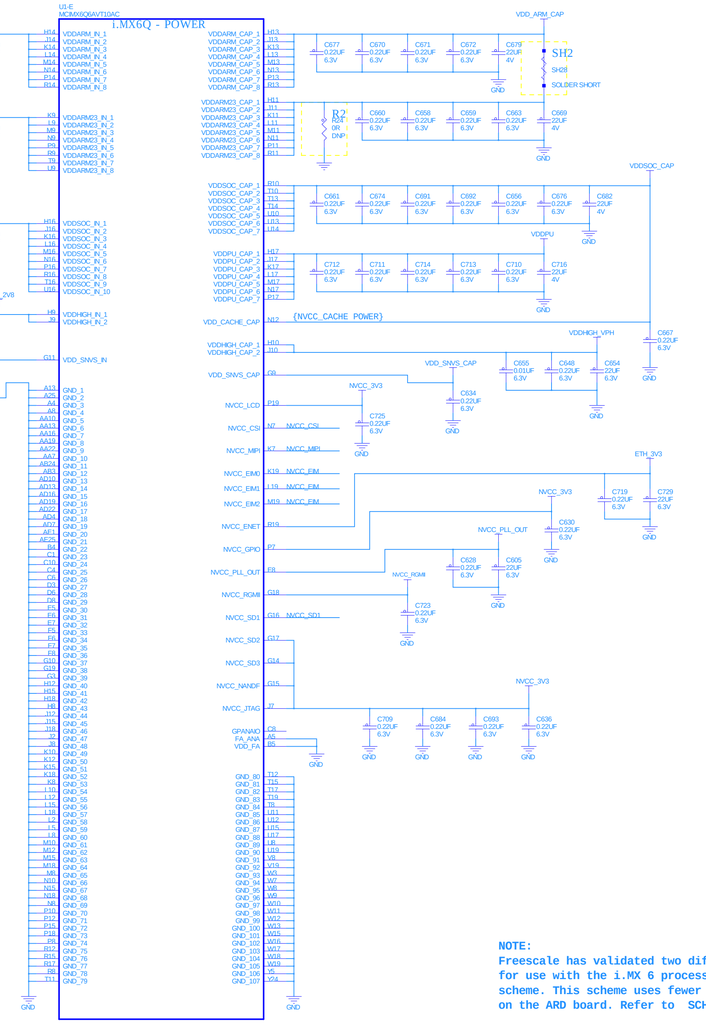
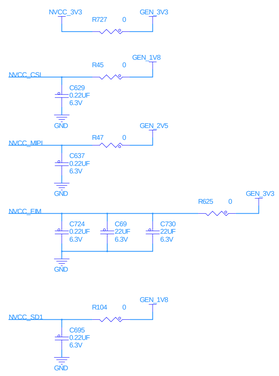






NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and DualLite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

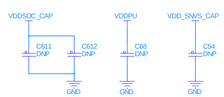
NOTE:
Diode D10 is required to correct a problem on a small number of i.MX6 DualLite parts in which VDDSNVS does not come up when VDDHIGH_IN is applied. A similar problem was corrected on i.MX6Q T01.2 processors. The diode is left populated for similarity across the Smart Device family of boards.

NOTE:
Freescale has validated two difference sets of decoupling capacitors and board layouts for use with the i.MX 6 processor. The customer is free to choose the desired decoupling scheme. This scheme uses fewer components. The alternate scheme can be found on the ARD board. Refer to SCH-27142 and LAY-27142.

Table 4. VDDARMxx_xx Power Connections

	i.MX 6Quad	i.MX 6Dual	i.MX 6DualLite	i.MX 6Solo
SH1	Shorted	Open	Shorted	Shorted
SH2	Shorted	Open	Shorted	Shorted
R1	Open	Shorted	Open	Open
R2	Open	Shorted	Open	Open

Extra Bulk Capacitors



NOTE:
In early designs of the Smart Device board, these bulk capacitors were used. After testing of the board, it was found that these capacitors could be removed with no effect. This reduces the capacitve loading on the internal processor LDOs. The coponents/footprints have been left in place in the event that future applications and/or software changes show that these capacitors are needed.

ICAP Classification: FCP: ___ FIUO: ___ PUBI: X
Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM
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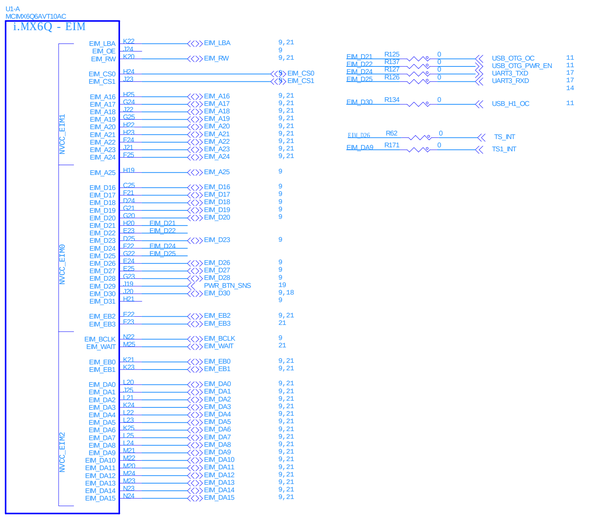

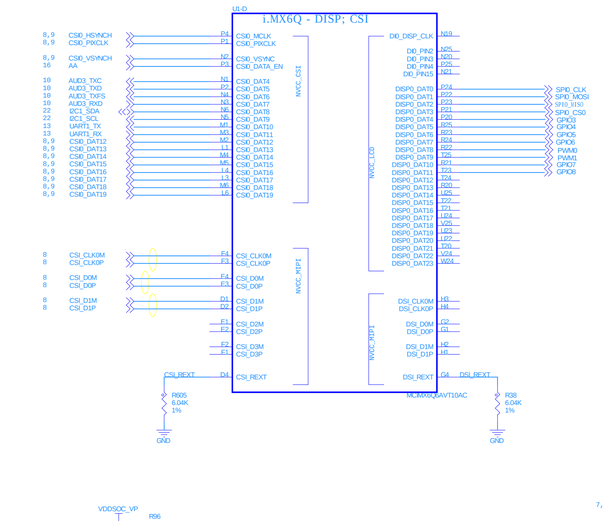

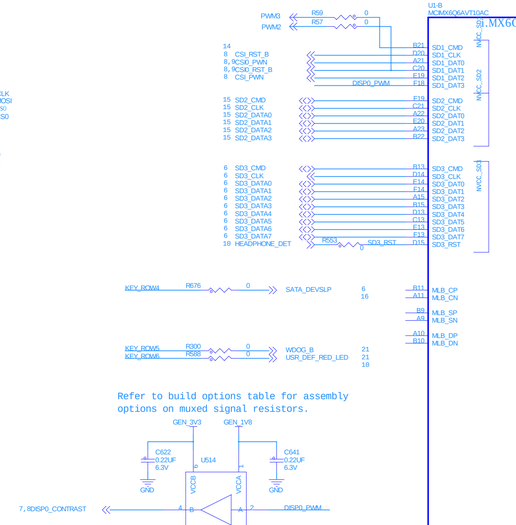

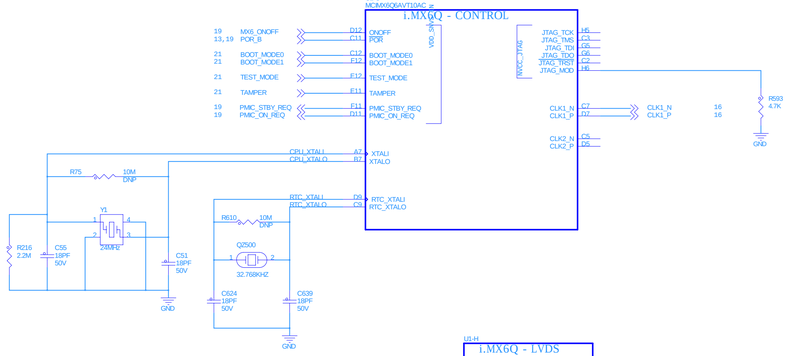

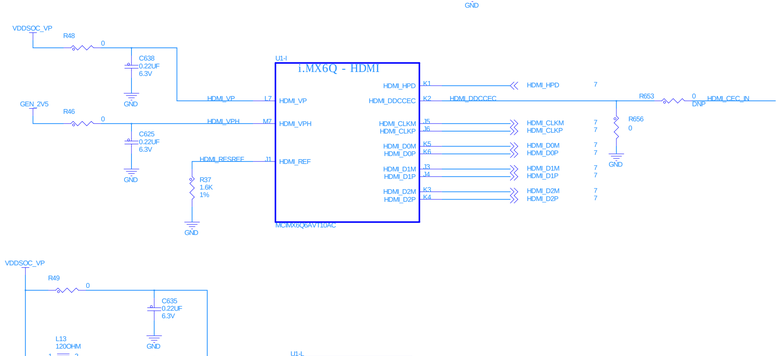

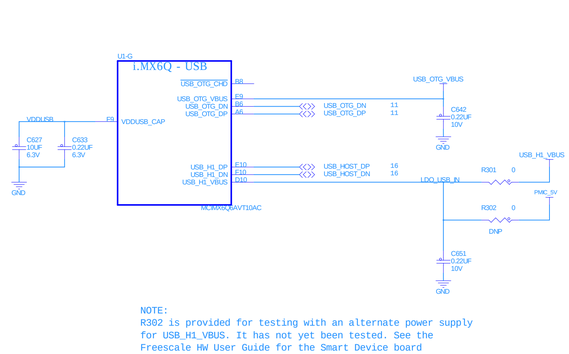

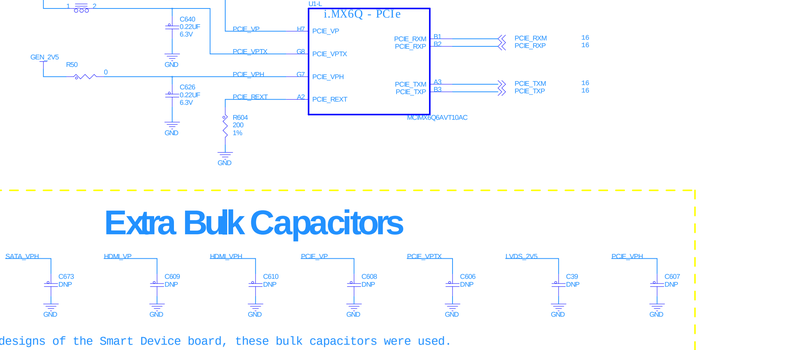

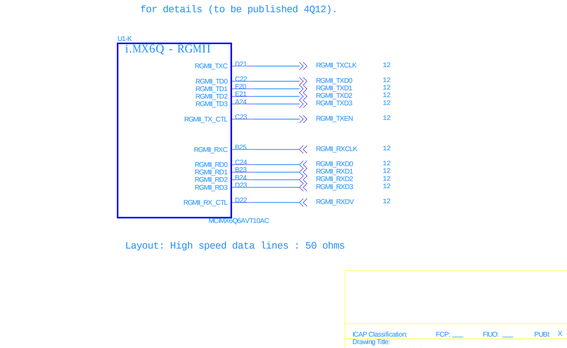

Note:

1) R216 is required to correct a known 24MHz slow starting issue present on some iMX 6 part. Please refer to the i.MX 6 Processor Errata, issue # ERR003745 for more details.

2) Per bulletin EB830, the i.MX6 processor may drive the 24 MHz crystal up to 250 uW. Freescale recommends following the guidelines contained in the bulletin.

The HW Developer Guide contains additional information.

NVCC_LVDS2P5 also powers on-chip DDR I/O predrivers, and must be powered whether LVDS is used or not.

Extra Bulk Capacitors

SATA_VP C681 DNP GND
SATA_VPH C673 DNP GND
HDMI_VP C609 DNP GND
HDMI_VPH C610 DNP GND
PCIE_VP C608 DNP GND
PCIE_VPTX C606 DNP GND
LVDS_2V5 C39 DNP GND
PCIE_VPH C607 DNP GND

NOTE:
In early designs of the Smart Device board, these bulk capacitors were used. After testing of the board, it was found that these capacitors could be removed with no effect. This reduces the capacitve loading on the internal processor LDOs. The coponents/footprints have been left in place in the event that future applications and/or software changes show that these capacitors are needed.

NOTE:
R302 is provided for testing with an alternate power supply for USB_H1_VBUS. It has not yet been tested. See the Freescale HW User Guide for the Smart Device board for details (to be published 4Q12).

Layout: High speed data lines : 50 ohms

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MCIMX6Q-SMART DEVICE PLATFORM
Page Title:
CPU SIGNAL
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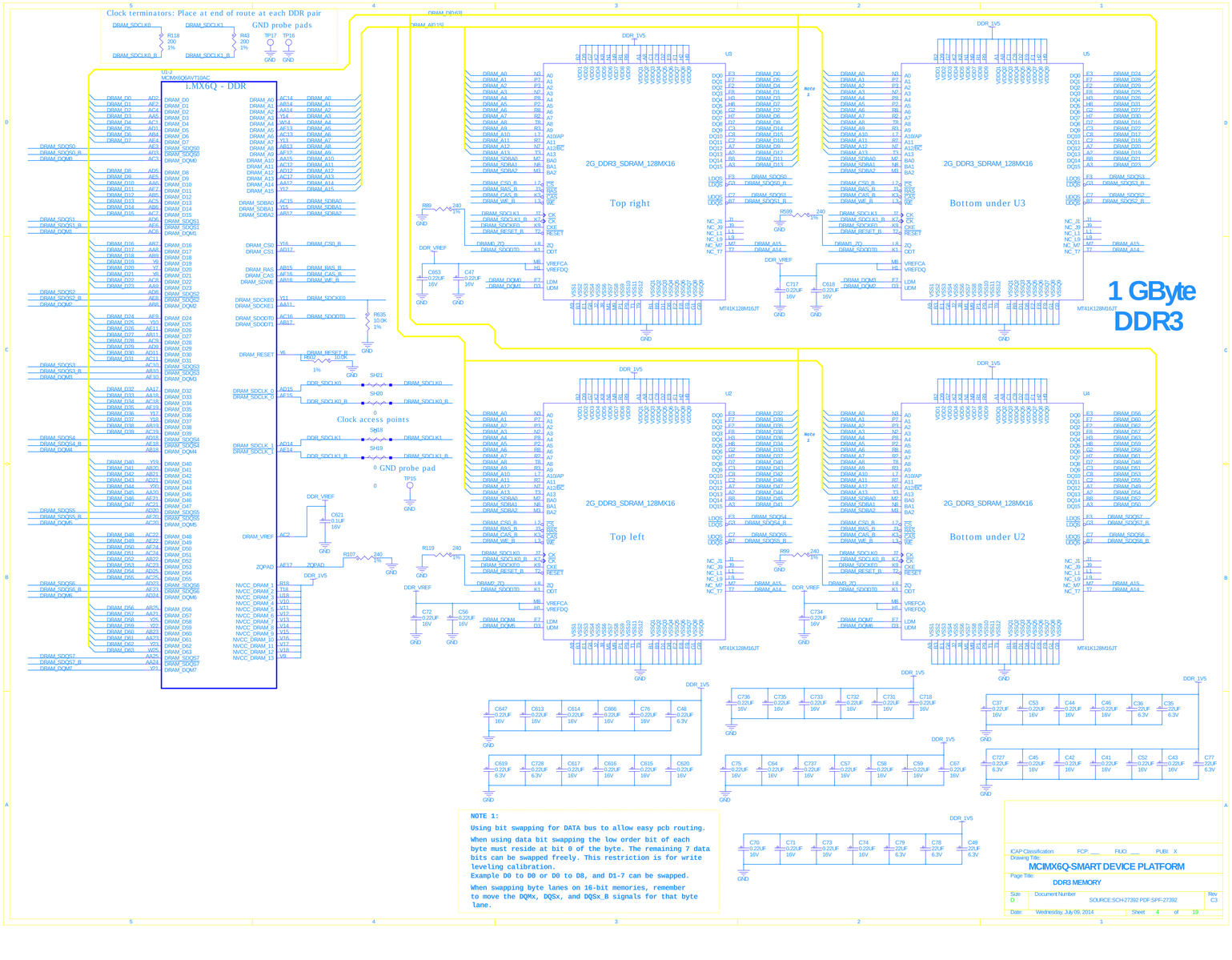
Clock terminators: Place at end of route at each DDR pair
DRAM_SDCLK0
DRAM_SDCLK1
GND probe pads
R118 200 1%
R43 200 1%
TP17
TP16
DRAM_SDCLK0_B
DRAM_SDCLK1_B
U1-J
MCIMX6Q4AVT10AC
i.MX6Q - DDR
DRAM_D0
DRAM_D1
DRAM_D2
DRAM_D3
DRAM_D4
DRAM_D5
DRAM_D6
DRAM_D7
DRAM_SDQS0
DRAM_SDQS0_B
DRAM_DQM0
DRAM_D8
DRAM_D9
DRAM_D10
DRAM_D11
DRAM_D12
DRAM_D13
DRAM_D14
DRAM_D15
DRAM_SDQS1
DRAM_SDQS1_B
DRAM_DQM1
DRAM_D16
DRAM_D17
DRAM_D18
DRAM_D19
DRAM_D20
DRAM_D21
DRAM_D22
DRAM_D23
DRAM_SDQS2
DRAM_SDQS2_B
DRAM_DQM2
DRAM_D24
DRAM_D25
DRAM_D26
DRAM_D27
DRAM_D28
DRAM_D29
DRAM_D30
DRAM_D31
DRAM_SDQS3
DRAM_SDQS3_B
DRAM_DQM3
DRAM_D32
DRAM_D33
DRAM_D34
DRAM_D35
DRAM_D36
DRAM_D37
DRAM_D38
DRAM_D39
DRAM_SDQS4
DRAM_SDQS4_B
DRAM_DQM4
DRAM_D40
DRAM_D41
DRAM_D42
DRAM_D43
DRAM_D44
DRAM_D45
DRAM_D46
DRAM_D47
DRAM_SDQS5
DRAM_SDQS5_B
DRAM_DQM5
DRAM_D48
DRAM_D49
DRAM_D50
DRAM_D51
DRAM_D52
DRAM_D53
DRAM_D54
DRAM_D55
DRAM_SDQS6
DRAM_SDQS6_B
DRAM_DQM6
DRAM_D56
DRAM_D57
DRAM_D58
DRAM_D59
DRAM_D60
DRAM_D61
DRAM_D62
DRAM_D63
DRAM_SDQS7
DRAM_SDQS7_B
DRAM_DQM7
DRAM_A0
DRAM_A1
DRAM_A2
DRAM_A3
DRAM_A4
DRAM_A5
DRAM_A6
DRAM_A7
DRAM_A8
DRAM_A9
DRAM_A10
DRAM_A11
DRAM_A12
DRAM_A13
DRAM_A14
DRAM_A15
DRAM_SDBA0
DRAM_SDBA1
DRAM_SDBA2
DRAM_CS0_B
DRAM_CAS_B
DRAM_RAS_B
DRAM_WE_B
DRAM_SDCKE0
DRAM_SDCKE1
DRAM_SDODT0
DRAM_SDODT1
DRAM_RESET
DRAM_RESET_B
R600 470R 1%
DDR_SDCLK0
DRAM_SDCLK0
DDR_SDCLK0_B
DRAM_SDCLK0_B
SH21
SH20
0
Clock access points
DDR_SDCLK1
DRAM_SDCLK1
DDR_SDCLK1_B
DRAM_SDCLK1_B
SH18
SH19
0 GND probe pad
TP15
DRAM_VREF
C621 0.1UF 16V
ZQPAD
R107 240 1%
DDR_1V5
NVCC_DRAM_1
NVCC_DRAM_2
NVCC_DRAM_3
NVCC_DRAM_4
NVCC_DRAM_5
NVCC_DRAM_6
NVCC_DRAM_7
NVCC_DRAM_8
NVCC_DRAM_9
NVCC_DRAM_10
NVCC_DRAM_11
NVCC_DRAM_12
NVCC_DRAM_13
R635 10.0K 1%
DRAM_DQ[63]
DRAM_A[15]
DDR_1V5
U3
2G_DDR3_SDRAM_128MX16
Top right
R89 240 1%
DDR_VREF
C653 0.22UF 16V
C47 0.22UF 16V
MT41K128M16JT
U5
Bottom under U3
R599 240 1%
C717 0.22UF 16V
C618 0.22UF 16V
U2
Top left
R119 240 1%
C72 0.22UF 16V
C56 0.22UF 16V
U4
Bottom under U2
R99 240 1%
C734 0.22UF 16V
Note 1
1 GByte DDR3
C647 0.22UF 16V
C613 0.22UF 16V
C614 0.22UF 16V
C666 0.22UF 16V
C76 0.22UF 16V
C46 0.22UF 6.3V
C619 0.22UF 6.3V
C728 0.22UF 6.3V
C617 0.22UF 16V
C616 0.22UF 16V
C615 0.22UF 16V
C620 0.22UF 16V
C736 0.22UF 16V
C735 0.22UF 16V
C733 0.22UF 16V
C732 0.22UF 16V
C731 0.22UF 16V
C718 0.22UF 16V
C75 0.22UF 16V
C64 0.22UF 16V
C737 0.22UF 16V
C57 0.22UF 16V
C58 0.22UF 16V
C59 0.22UF 16V
C67 0.22UF 16V
C37 0.22UF 16V
C53 0.22UF 16V
C44 0.22UF 16V
C46 0.22UF 16V
C36 0.22UF 6.3V
C35 0.22UF 6.3V
C727 0.22UF 6.3V
C45 0.22UF 16V
C42 0.22UF 16V
C41 0.22UF 16V
C52 0.22UF 16V
C43 0.22UF 16V
C77 0.22UF 6.3V
C70 0.22UF 16V
C71 0.22UF 16V
C73 0.22UF 16V
C74 0.22UF 16V
C79 22UF 6.3V
C78 22UF 6.3V
C49 22UF 6.3V
NOTE 1:
Using bit swapping for DATA bus to allow easy pcb routing.
When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration.
Example D0 to D0 or D0 to D8, and D1-7 can be swapped.
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.
ICAP Classification: FCP: ___ FIUO: ___ PUBI: X
Drawing Title:
MCIMX6Q-SMART DEVICE PLATFORM
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DDR3 MEMORY
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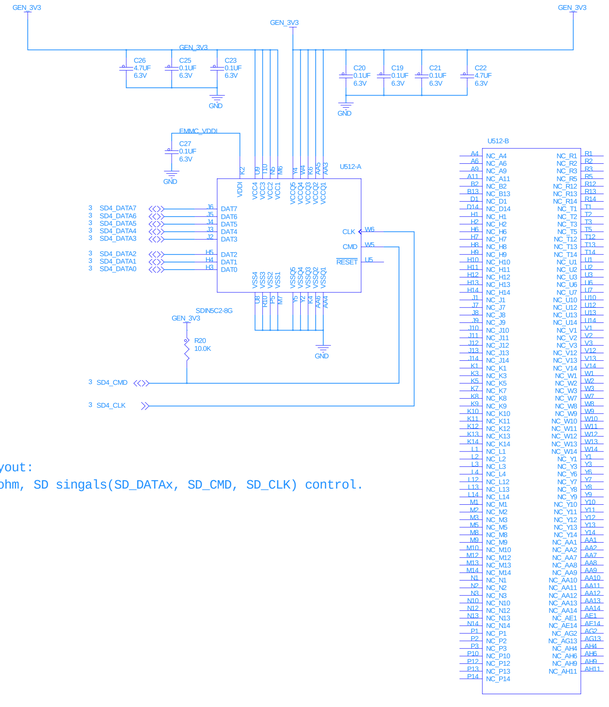
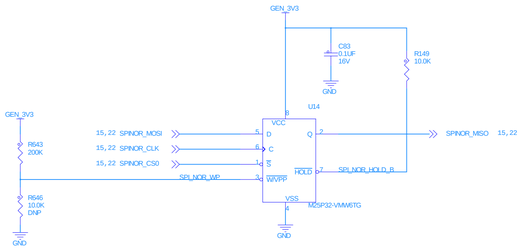
8GB eMMC MEMORY



Layout:
50ohm, SD singals(SD_DATAx, SD_CMD, SD_CLK) control.

4MB SPI NOR FLASH



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Page Title:	eMMC, SPI NOR FLASH
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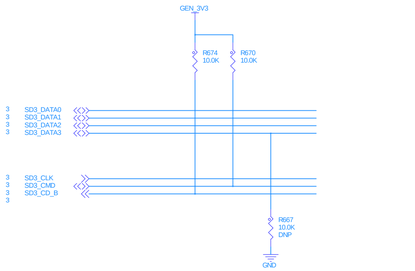
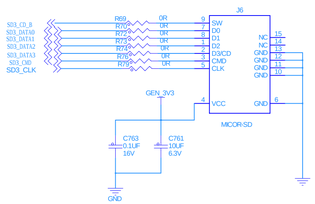
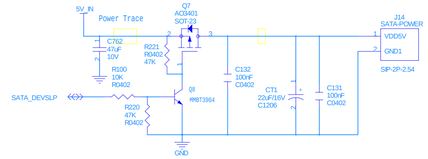
SD CARD SOCKET

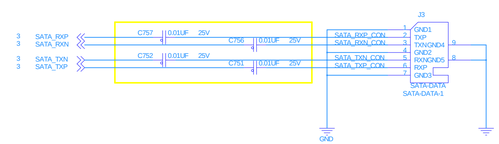




Layout:
50ohm, SD signals(SD_DATAx, SD_CMD, SD_CLK) length equal

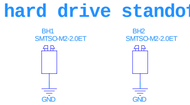
SATA CONNECTOR





Layout:
1. 100ohm diff pairs, length equal
2. Mount these capacitors very close to the connector J506.

hard drive standoff



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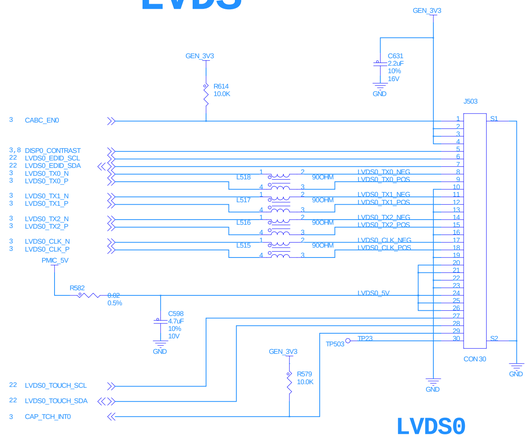
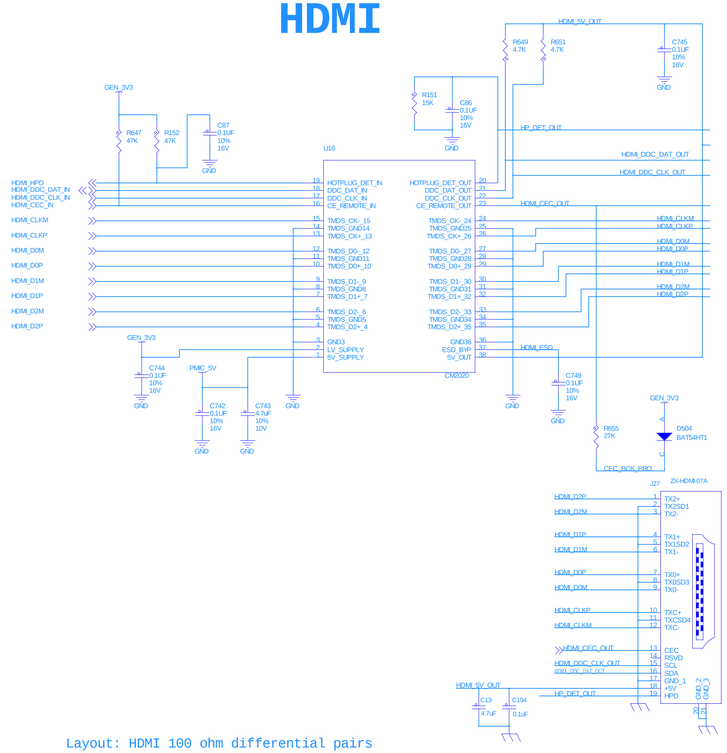
LVDS



LVDS0

Place L515, L516, L517 and L518
CMCs close to J403 connector.

HDMI



Layout: HDMI 100 ohm differential pairs

NOTE:
When using HDMI, I2C2 bus is limited to 100 kHz
to read EDID values due to HDMI standards.
I2C2 bus speed should be limited to 100 kHz whenever
Hot Plug Detect is high.

LVDS Connector notes:
Pin 1: This pin is the Display Enable pin. It is used to
Enable/Disable the HannStar display.
Pin 5: This pin is the Display Brightness control. It
provides a PWM signal to the display to increase/
decrease display brightness depending on PWM
duty cycle. This signal is shared by all displays, so all
displays will change brightness together.

22
22
3

ICAP Classification: FCP: ___ FIUO: ___ PUBS: X

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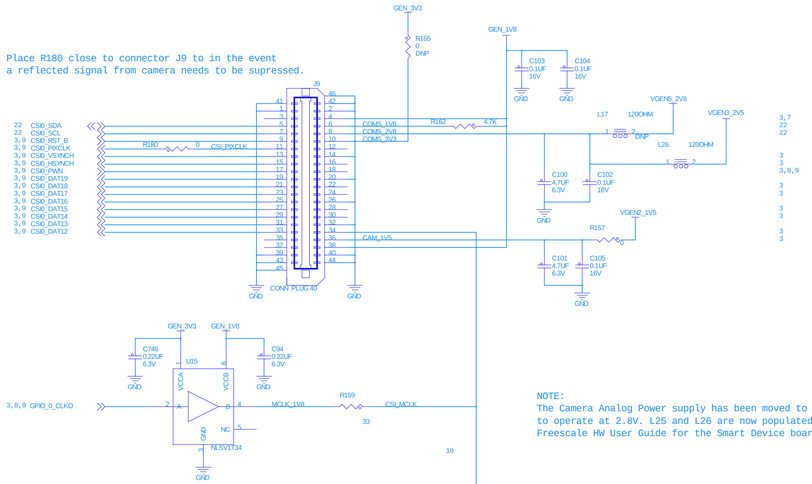
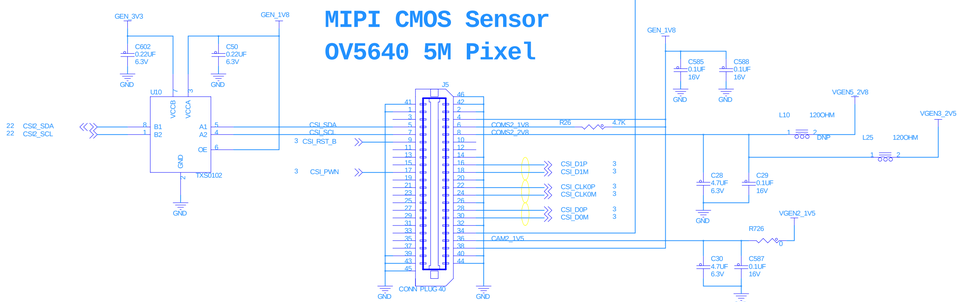
CSI CMOS Sensor
OV5642 5M Pixel



Place R158 and R159 near U15.
Acts as source termination.

NOTE:
The Camera Analog Power supply has been moved to VGEN3. Freescale SW will program VGEN3 to operate at 2.8V. L25 and L26 are now populated and L10 and L17 are depopulated. See the Freescale HW User Guide for the Smart Device board for details (to be published 4Q12).

MIPI CMOS Sensor
OV5640 5M Pixel



Layout: 100 ohm differential pairs

ICAP Classification: FCP: ____ FIUO: ____ PUBI: X
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MCIMX6Q-SMART DEVICE PLATFORM
Page Title:
CAMERA, EXP PORT
Size: D | Document Number: SOURCE:SCH-27392 PDF:SPF-27392 | Rev: C3
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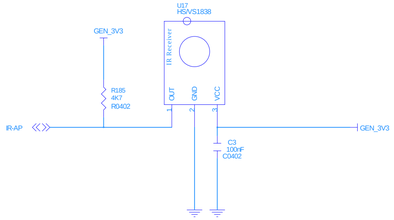

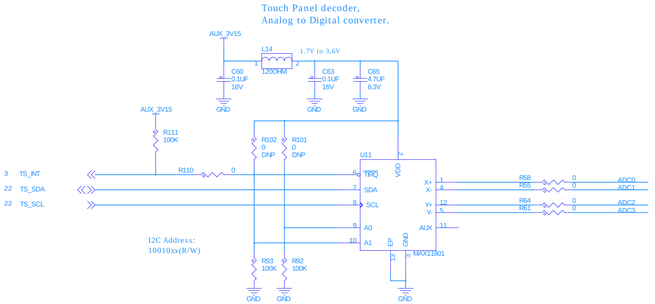

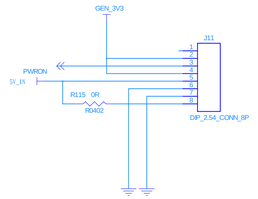

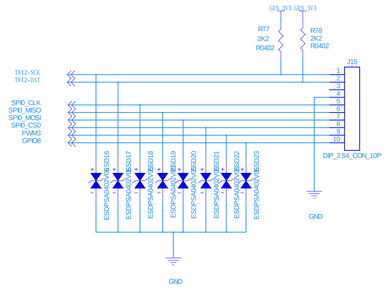

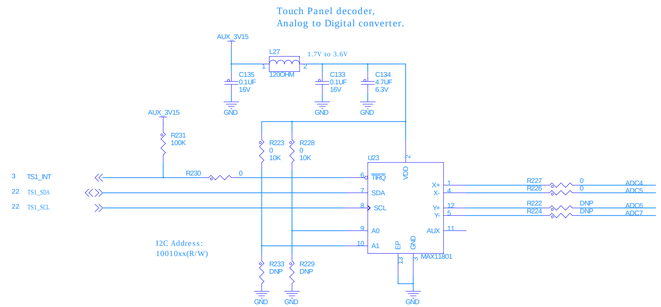

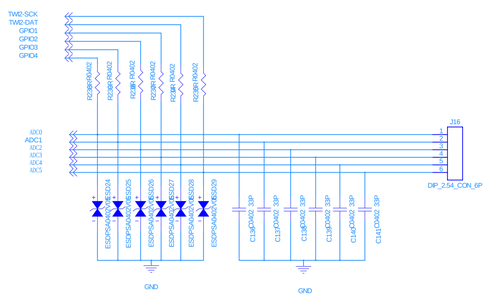

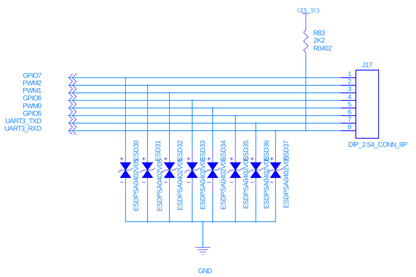

ICAP Classification:	FCP: ___	FIUO: ___	PUBI: X
Drawing Title:	MCIMX6Q-SMART DEVICE PLATFORM		
Page Title:	ArduinoSocket		
Size: D	Document Number: SOURCE:SCH-27392 PDF:SPF-27392		Rev: C3
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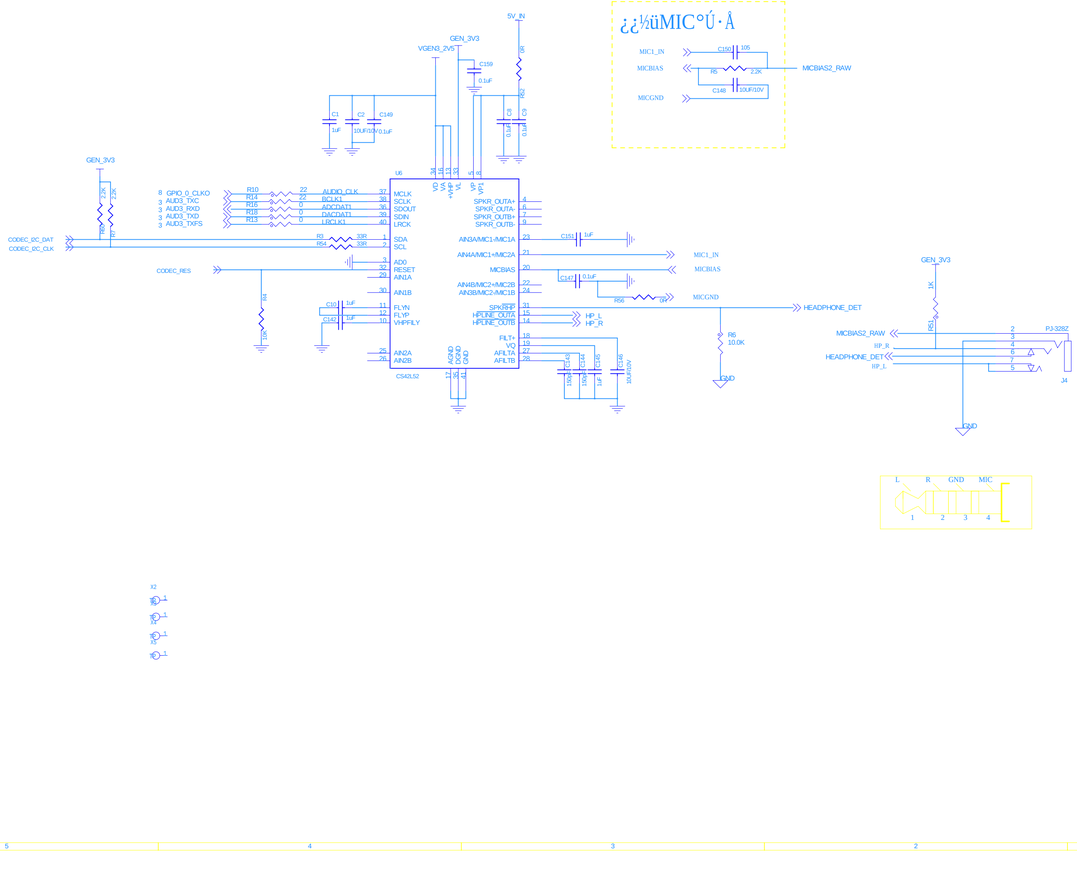
5 4 3 2 1



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Drawing Title:	MCIMX6Q-SMART DEVICE PLATFORM		
Page Title:	AUDIO		
Size: D	Document Number: SOURCE:SCH-27392 PDF:SPF-27392		Rev: C3
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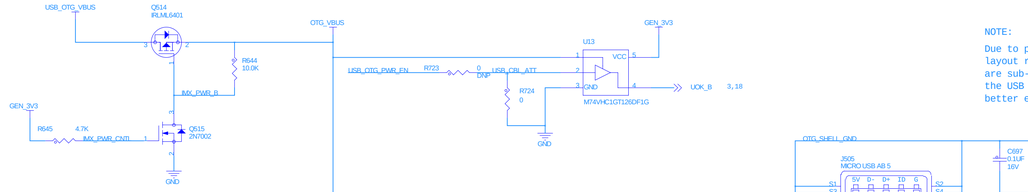
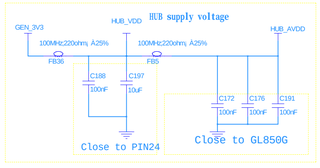
USB-OTG

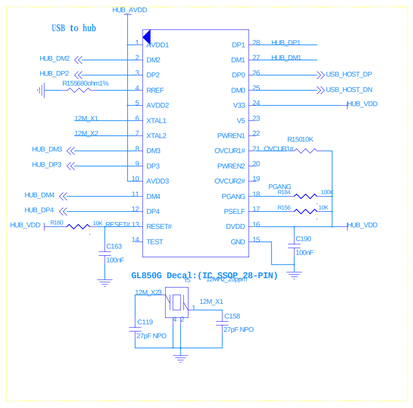


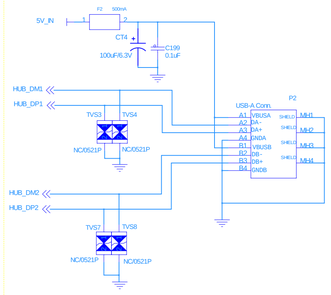
NOTE:

Due to placement requirements on the SABRE SD board set, layout routing for the USB_OTG_DP and USB_OTG_DN traces are sub-optimal. It is recommended that customers consider using the USB layout on the Freescale i.MX6 SABRE AI board as a better example of proper USB trace routing.

USB-HOST-HUB







ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title:

MCIMX6Q-SMART DEVICE PLATFORM

Page Title: USB

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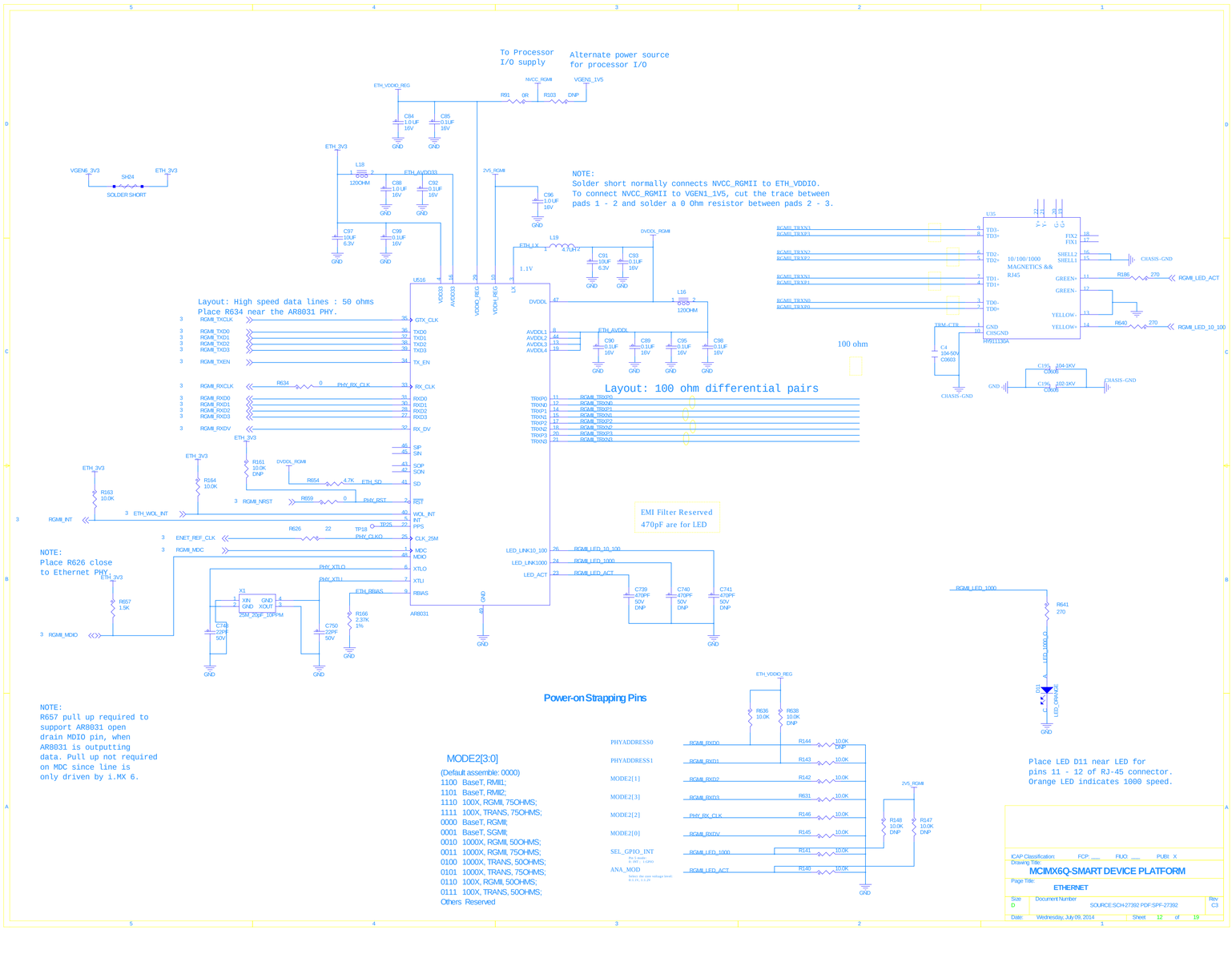
To Processor I/O supply
Alternate power source for processor I/O
ETH_VDDIO_REG
NVCC_RGMII
VGEN1_1V5
R91 0R
R103 DNP
C94 1.0UF 16V
C95 0.1UF 16V
ETH_3V3
L18 120OHM
ETH_AVDD33
C88 1.0UF 16V
C92 0.1UF 16V
2V5_RGMII
C96 1.0UF 16V
VGEN6_3V3
SH24
SOLDER SHORT
ETH_3V3
NOTE:
Solder short normally connects NVCC_RGMII to ETH_VDDIO.
To connect NVCC_RGMII to VGEN1_1V5, cut the trace between
pads 1 - 2 and solder a 0 Ohm resistor between pads 2 - 3.
C97 10UF 6.3V
C99 0.1UF 16V
ETH_LX
L19 4.7UH+2
DVDDL_RGMII
C91 10UF 6.3V
C93 0.1UF 16V
1.1V
U516
VDD33
AVDD33
VDDO_REG
VDDL_REG
LX
DVDDL
L16 120OHM
Layout: High speed data lines : 50 ohms
Place R634 near the AR8031 PHY.
RGMII_TXCLK
GTX_CLK
RGMII_TXD0
RGMII_TXD1
RGMII_TXD2
RGMII_TXD3
TXD0
TXD1
TXD2
TXD3
RGMII_TXEN
TX_EN
AVDDL1
AVDDL2
AVDDL3
AVDDL4
ETH_AVDDL
C90 0.1UF 16V
C89 0.1UF 16V
C95 0.1UF 16V
C98 0.1UF 16V
RGMII_RXCLK
R634 0
PHY_RX_CLK
RX_CLK
RGMII_RXD0
RGMII_RXD1
RGMII_RXD2
RGMII_RXD3
RXD0
RXD1
RXD2
RXD3
RGMII_RXDV
RX_DV
Layout: 100 ohm differential pairs
TRXP0
TRXN0
TRXP1
TRXN1
TRXP2
TRXN2
TRXP3
TRXN3
RGMII_TRXP0
RGMII_TRXN0
RGMII_TRXP1
RGMII_TRXN1
RGMII_TRXP2
RGMII_TRXN2
RGMII_TRXP3
RGMII_TRXN3
ETH_3V3
R161 10.0K DNP
DVDDL_RGMII
R654 4.7K
ETH_SD
SIP
SIN
SOP
SON
SD
ETH_3V3
R163 10.0K
R164 10.0K
RGMII_NRST
R659 0
PHY_RST
RST
RGMII_INT
ETH_WOL_INT
WOL_INT
INT
PPS
ENET_REF_CLK
R626 22
TP18
TP25
PHY_CLKO
CLK_25M
RGMII_MDC
MDC
MDIO
NOTE:
Place R626 close
to Ethernet PHY.
PHY_XTLO
XTLO
PHY_XTLI
XTLI
ETH_RBIAS
RBIAS
ETH_3V3
R657 1.5K
RGMII_MDIO
X1
XIN GND
GND XOUT
25M_20pF_10PPM
C748 22PF 50V
C750 22PF 50V
R166 2.37K 1%
AR8031
GND
LED_LINK10_100
LED_LINK1000
LED_ACT
RGMII_LED_10_100
RGMII_LED_1000
RGMII_LED_ACT
C739 470PF 50V DNP
C740 470PF 50V DNP
C741 470PF 50V DNP
EMI Filter Reserved
470pF are for LED
U35
RGMII_TRXN3
RGMII_TRXP3
RGMII_TRXN2
RGMII_TRXP2
RGMII_TRXN1
RGMII_TRXP1
RGMII_TRXN0
RGMII_TRXP0
TD3-
TD3+
TD2-
TD2+
TD1-
TD1+
TD0-
TD0+
10/100/1000
MAGNETICS &&
RJ45
FIX2
FIX1
SHELL2
SHELL1
CHASSIS-GND
GREEN+
GREEN-
YELLOW-
YELLOW+
R186 270
RGMII_LED_ACT
R640 270
RGMII_LED_10_100
TRM_CTR
GND
CHSGND
H911130A
C4 104-50V C0603
CHASSIS-GND
C195 .004-1KV C0603
C196 .002-1KV C0603
GND
CHASSIS-GND
100 ohm
RGMII_LED_1000
R641 270
LED_1000_O
D21
LED_ORANGE
GND
Power-on Strapping Pins
ETH_VDDIO_REG
R636 10.0K
R638 10.0K DNP
PHYADDRESS0
PHYADDRESS1
MODE2[1]
MODE2[3]
MODE2[2]
MODE2[0]
SEL_GPIO_INT
ANA_MOD
RGMII_RXD0
RGMII_RXD1
RGMII_RXD2
RGMII_RXD3
PHY_RX_CLK
RGMII_RXDV
RGMII_LED_1000
RGMII_LED_ACT
R144 10.0K DNP
R143 10.0K DNP
R142 10.0K DNP
R631 10.0K DNP
R146 10.0K DNP
R145 10.0K DNP
R141 10.0K DNP
R140 10.0K DNP
2V5_RGMII
R148 10.0K DNP
R147 10.0K DNP
GND
MODE2[3:0]
(Default assemble: 0000)
1100 BaseT, RMII1;
1101 BaseT, RMII2;
1110 100X, RGMII, 75OHMS;
1111 100X, TRANS, 75OHMS;
0000 BaseT, RGMII;
0001 BaseT, SGMII;
0010 1000X, RGMII, 50OHMS;
0011 1000X, RGMII, 75OHMS;
0100 1000X, TRANS, 50OHMS;
0101 1000X, TRANS, 75OHMS;
0110 100X, RGMII, 50OHMS;
0111 100X, TRANS, 50OHMS;
Others Reserved
NOTE:
R657 pull up required to
support AR8031 open
drain MDIO pin, when
AR8031 is outputting
data. Pull up not required
on MDC since line is
only driven by i.MX 6.
Place LED D11 near LED for
pins 11 - 12 of RJ-45 connector.
Orange LED indicates 1000 speed.
ICAP Classification: FCP: ___ FIUO: ___ PUBI: X
Drawing Title:
MCIMX6Q-SMART DEVICE PLATFORM
Page Title:
ETHERNET
Size: D
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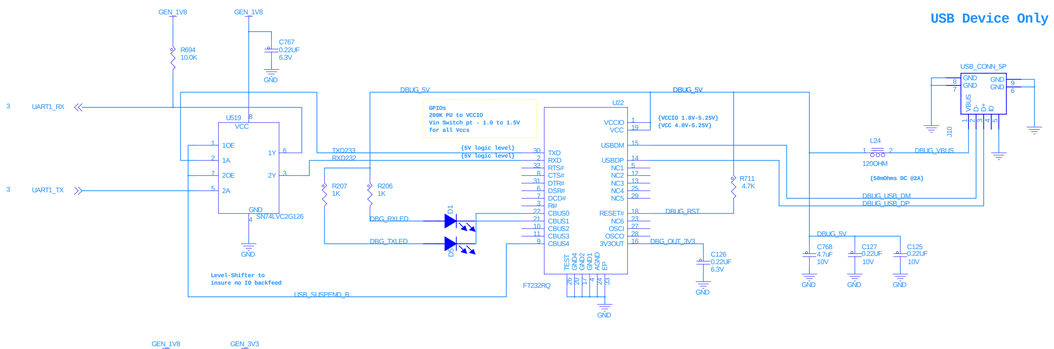
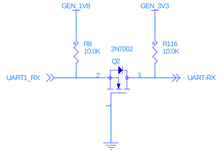
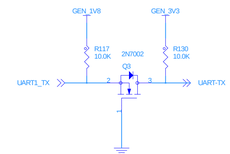
DEBUG UART TO USB CONVERSION

Library Revision - A

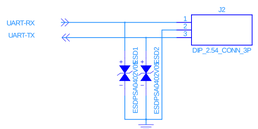
USB Device Only







Drivers located at:
http://www.ftdichip.com/Products/ICs/FT232R.htm



ICAP Classification: FCP: ____ FIUO: ____ PUBI: X

Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM

Page Title: JTAG, DEBUG

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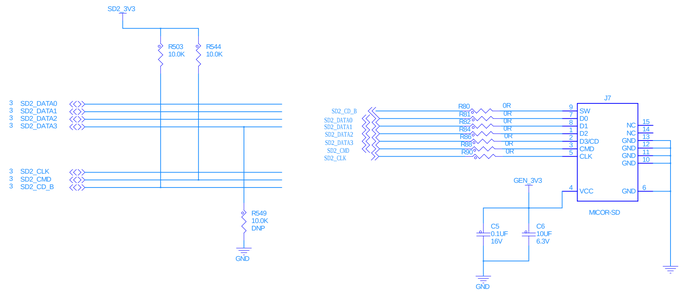
AUX SDIO CARD SOCKET



Layout:
50ohm, SD signals(SD_DATAx, SD_CMD, SD_CLK) length equal

NOTE:
The AUX SDIO CARD SOCKET and the
BLUETOOTH CABLE CONNECTOR
have been designed and tested
specifically for use with the WIFI/BT
combo card SX-SDCAN-2830BT
Developed and sold by
Silex Technolgy. The developer
may need to consult the datasheet
of other WIFI solutions for compatibility
with this card socket.

ICAP Classification: FCP: ____ FUO: ____ PUBI: X
Drawing Title:
MCIMX6Q-SMART DEVICE PLATFORM
Page Title:
AUX SDIO CONN, CAN
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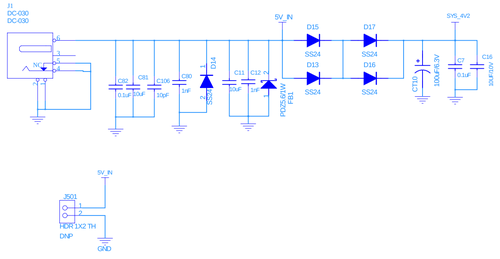
External
Power
5 Vdc



NOTE:
R728 is provided for testing a means to suspend battery charging so that an acurate voltage reading can be taken during the battery charge cycle. It has not yet been tested. When populating R728, R134 should be depopulated. See the Freescale HW User Guide for the Smart Device board for details (to be published 4Q12).

Note: Populate either
Option #1 for the Smart Device Board, or
Option #2 for the Smart Device Platform

ICAP Classification: FCP: ____ FIUO: ____ PUBI: X

Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM

Page Title: BATTERY CHARGER

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PMIC LDO Outputs

PMIC Switched Outputs

PMIC Powered-ON LED indicator

PMIC Control

POWER

Note:
Bulk capacitors on VGEN1-6 are all 4.7uF for BOM consolidation purposes. Freescale recommended guidance for minimum capacitance on VGEN1, VGEN3, VGEN5, VGEN6 is 2.2uF.

NOTE:
R632 is provided for testing an alternate gating source for PMIC_5V power. The circuit has not yet been tested. See the Freescale HW User Guide for the Smart Device board for details (to be published 2Q13).

VDDOTP -

Connect TP14 to 8 volts to program PMIC OTP fuses

OPTIONAL:
PMIC Power On Circuit

Note:
To turn off board "AUTO ON" feature, depopulate R30 and R31, and populate U509. This feature has not yet been tested. See the Freescale HW User Guide for the Smart Device board for details (to be published 2Q13).

Note:
PMPF0100 Pass1.0 through Pass1.2 are subject to boot issues if power is removed from the board and reapplied within ~ 2 minutes.
PMPF0100 Pass2.0 will correct this issue. For more details, see the PMPF0100 ERRATA, Issue #ER19

ICAP Classification:	FCP: ___ FIUO: ___ PUBI: X
Drawing Title:	MCIMX6Q-SMART DEVICE PLATFORM
Page Title:	PF0100 PMIC
Size: D	Document Number: SOURCE:SCH-27392 PDF:SPF-27392 Rev: C3
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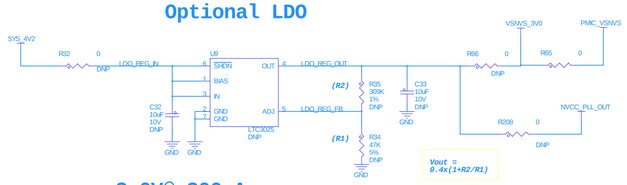
Optional LDO



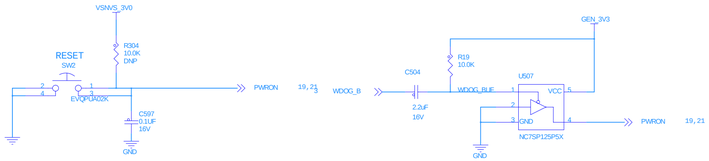
3.0V@ 300mA max

NOTE FOR VDDHIGH_IN LOADING ON VGEN5:
VDDHIGH was placed on VGEN5 early in the design as a compromise solution for a board designed primarily for software development. Validation of the i.MX6 processor has shown that operations at elevated temperatures may cause VDDHIGH_IN to require much more current than VGEN5 can supply. It is recommended for robust designs potentially operating at more extreme temperatures for VDDHIGH to be supplied from a power rail that can supply 250 mA or more.
This allows for datasheet maximum of 125 mA for internal VDDHIGH_IN loads plus 125 mA for external PHY IO loads.

The optional LDO U9 shown on this page could be reconfigured to supply both VDDHIGH_IN and VDD_SNVS_IN loads to meet the additional current requirments

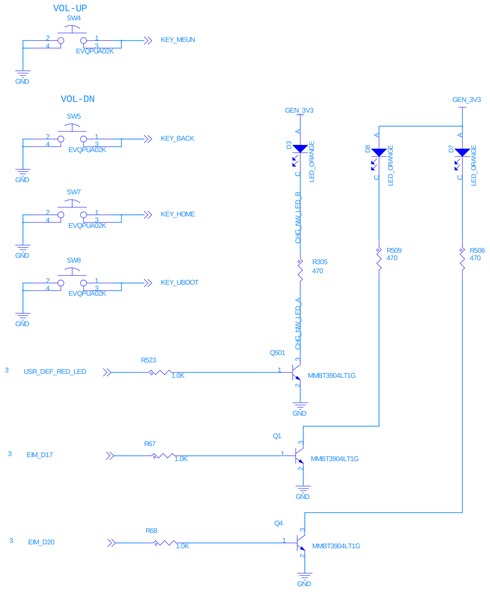
U9 is no longer required for PF0100 VSNVS issue, but may be desired for NVCC_PLL_VOUT.
It is being left in a depopulated condition. If the LDO is needed, R34 and R35 should be populated as follows:
For VSNVS (3.0V): R34 = 47K, R35 = 309K
For NVCC_PLL_OUT (1.1V): R34 = 47K, R35 = 82.5K

ICAP Classification: FCP: ____ FIUO: ____ PUBI: X
Drawing Title:
MCIMX6Q-SMART DEVICE PLATFORM
Page Title:
AUX VOLT REG
Size: D | Document Number: SOURCE:SCH-27392 PDF:SPF-27392 | Rev: C3
Date: Wednesday, July 09, 2014 | Sheet 17 of 19

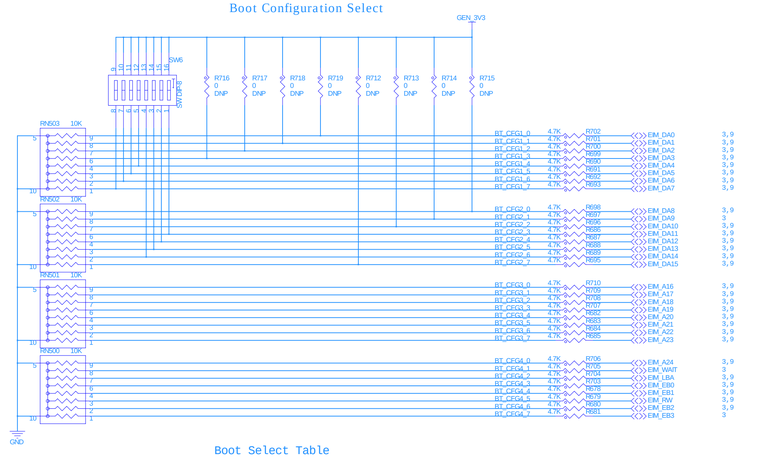


NOTE:
On Rev B4 and later designs, the RESET button is connected directly to the PWRON input of the PMIC. This will cause a complete board reset (Processor & PMIC) when the RESET button is pressed.

U/I KEY

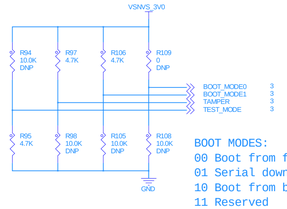


Boot Configuration Select



Boot Select Table

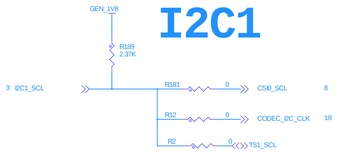
NOTE:
Place series resistors so as to minimize EIM portion of trace length. Two layout possibilites include:
1) As close to processor as possbile.
2) Close to other componets using EIM signals.

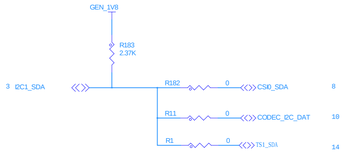


BOOT MODES:
00 Boot from fuses
01 Serial downloader
10 Boot from board settings
11 Reserved

ICAP Classification: FCP: ____ FIUO: ____ PUBI: X
Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM
Page Title: BOOT SELECT
Size: D | Document Number: SOURCE:SCH-27392 PDF:SPF-27392 | Rev: C3
Date: Wednesday, July 09, 2014 | Sheet 18 of 19

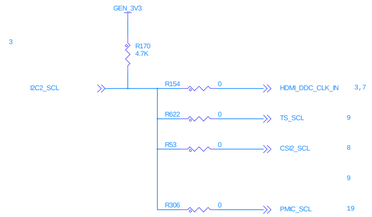
I2C1

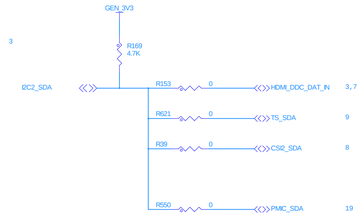




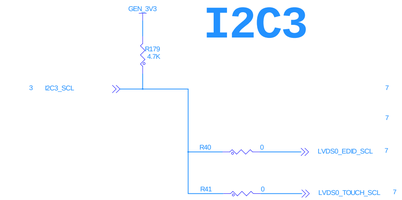
NOTE:
R183 and R189 were changed to bring I2C rise time from LOW >> HIGH within electric specification. If using a CODEC other than the one used in this design, it may be possbile to switch pull up resistors back to 4.7K.

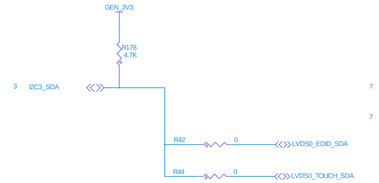
I2C2





I2C3





CSPI1

NOTE:
On all three pad resistor options, resistors are to be initially populated on pads 1 - 2 (Option A). Users may move resistors from their default locations as needed.

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