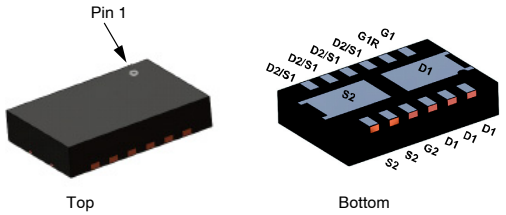
MOSFET – Dual N-Channel, POWERTRENCH®

100 V, 25 A, 19 mΩ

FDMD82100

V_{DS}	$r_{DS(ON)}$ MAX	I_D MAX
100 V	19 mΩ @ 10 V	25 A
	33 mΩ @ 6 V	



Power 3.3 x 5

PQFN12 3.3X5, 0.65P
CASE 483BN

General Description

This device includes two 100 V N−Channel MOSFETs in a dual Power (3.3 mm X 5 mm) package. HS source and LS Drain internally connected for half/full bridge, low source inductance package, low $r_{DS(on)}$/Qg FOM silicon.

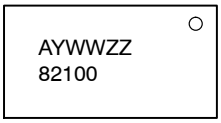
Features

- Max $r_{DS(on)}$ = 19 mΩ at V_{GS} = 10 V, I_D = 7 A
- Max $r_{DS(on)}$ = 33 mΩ at V_{GS} = 6 V, I_D = 5.5 A
- Ideal for Flexible Layout in Primary Side of Bridge Topology
- 100% UIL Tested
- Kelvin High Side MOSFET Drive Pin−out Capability
- This Device is Pb−Free, Halide Free and RoHS Compliant

Applications

- Synchronous Buck : Primary Switch of Half/Full bridge converter for telecom
- Motor Bridge: Primary Switch of Half/Full bridge converter for BLDC motor
- MV POL: 48 V Synchronous Buck Switch

MARKING DIAGRAM



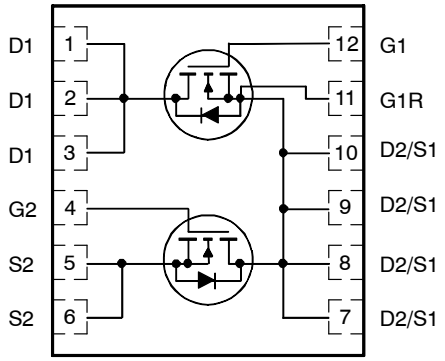
A	= Assembly Plant Code
YWW	= Date Code (Year & Week)
ZZ	= Lot Code
82100	= Specific Device Code

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter			Rating	Unit
V_{DS}	Drain to Source Voltage			100	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current	Continuous	T_C = 25°C	25	A
		Continuous (Note 1a)	T_A = 25°C	7	
		Pulsed (Note 4)		80	
E_{AS}	Single Pulse Avalanche Energy (Note 3)			121	mJ
P_D	Power Dissipation (Note 1a)		T_A = 25°C	2.1	W
	Power Dissipation (Note 1b)		T_A = 25°C	1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter		Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	3.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	60	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	130	

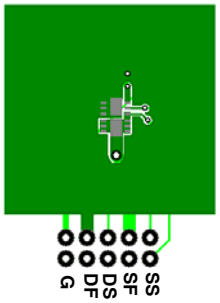
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	70	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	3.3	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	–9	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 7 A	–	15	19	mΩ
		V_{GS} = 6 V, I_D = 5.5 A	–	23	33	
		V_{GS} = 10 V, I_D = 7 A, T_J = 125°C	–	27	35	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 7 A	–	18	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	–	805	1070	pF
C_{oss}	Output Capacitance		–	176	235	pF
C_{rss}	Reverse Transfer Capacitance		–	8	15	pF
R_g	Gate Resistance		0.1	1.8	3.6	Ω
SWITCHING CHARACTERISTICS						
$td_{(on)}$	Turn−On Delay Time	V_{DD} = 50 V, I_D = 7 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	9.4	19	ns
t_r	Rise Time		–	3.2	10	
$t_{d(off)}$	Turn−Off Delay Time		–	15	27	
t_f	Fall Time		–	3.3	10	
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_D = 7 A	–	12	17	nC
		V_{GS} = 0 V to 6 V, V_{DD} = 50 V, I_D = 7 A	–	8	11	
Q_{gs}	Gate to Source Charge	V_{DD} = 50 V, I_D = 7 A	–	3.9	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	2.7	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 7 A (Note 2)	–	0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 7 A, di/dt = 100 A/μs	–	46	74	ns
Q_{rr}	Reverse Recovery Charge		–	48	77	nC

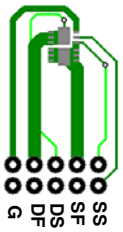
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 60°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 130°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 121 mJ is based on starting T_J = 25°C, L = 3 mH, I_{AS} = 9 A, V_{DD} = 100 V, V_{GS} = 10 V, 100% tested at L = 0.1 mH, I_{AS} = 30 A.
4. Pulse Id refers to Figure 11. Forward Bias Safe Operation Area.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

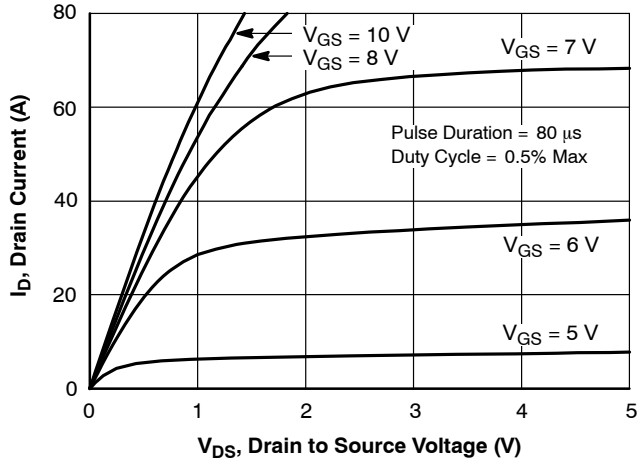


Figure 1. On Region Characteristics

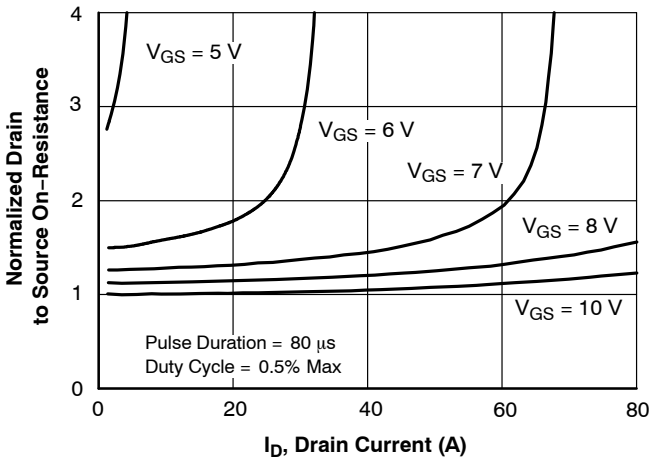


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

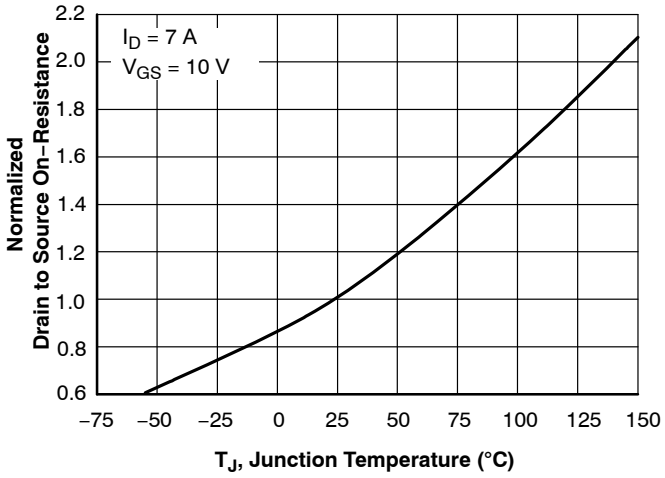


Figure 3. Normalized On Resistance vs. Junction Temperature

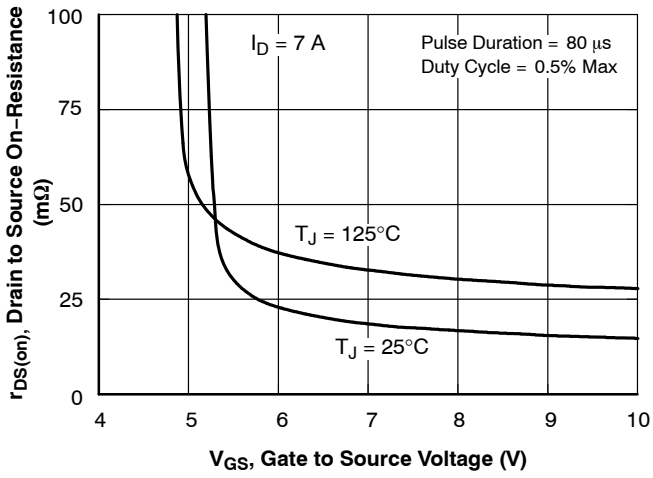


Figure 4. On−Resistance vs. Gate to Source Voltage

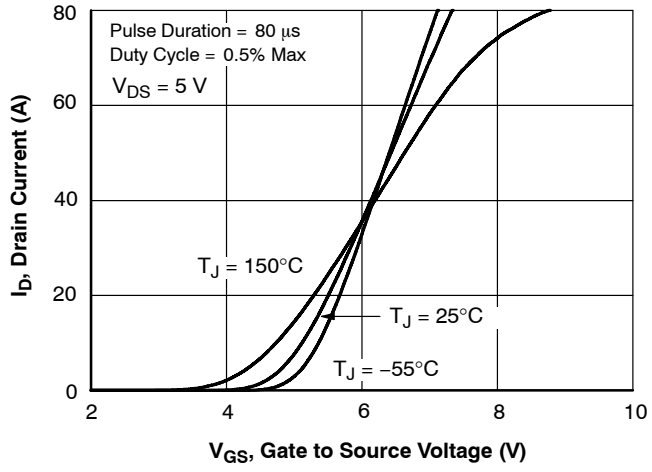


Figure 5. Transfer Characteristics

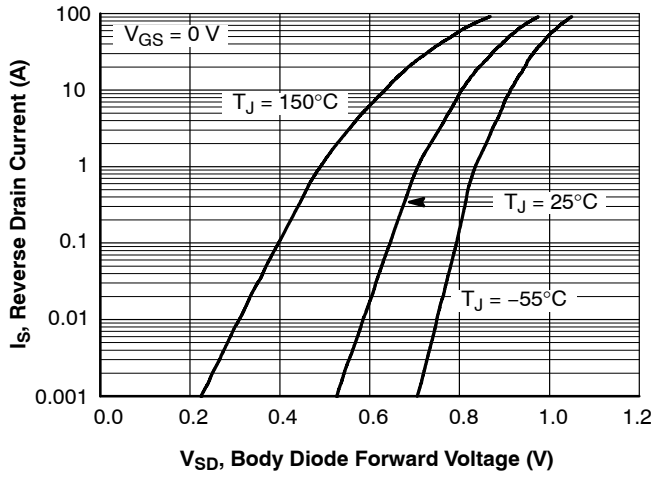


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

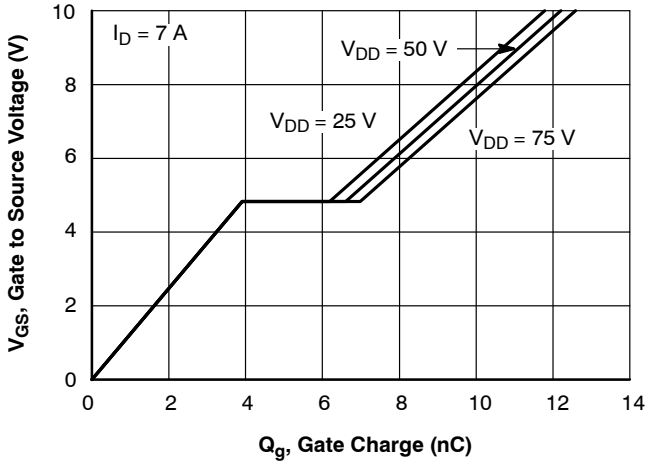


Figure 7. Gate Charge Characteristics

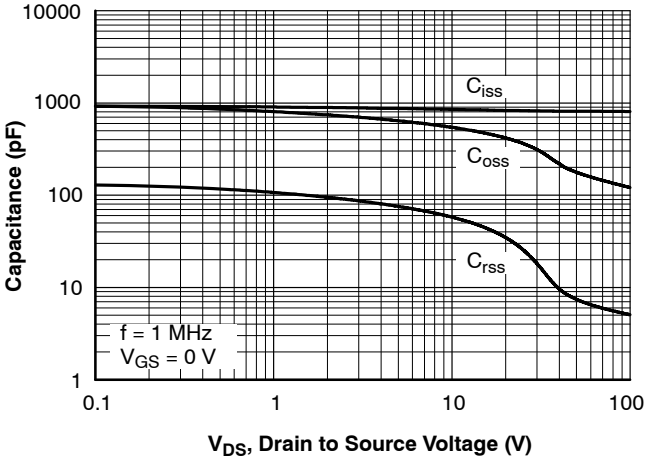


Figure 8. Capacitance vs. Drain to Source Voltage

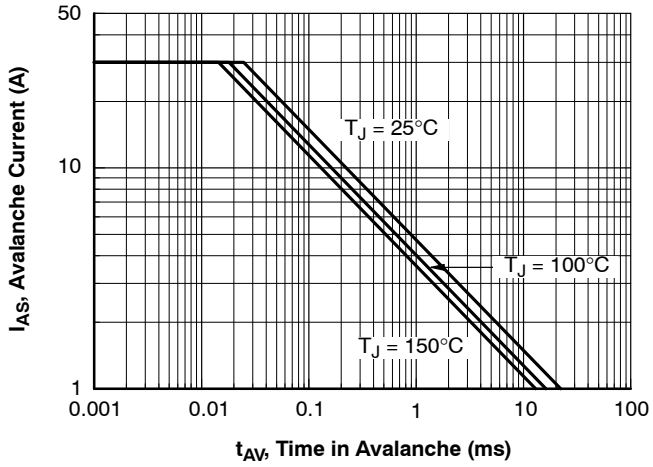


Figure 9. Unclamped Inductive Switching Capability

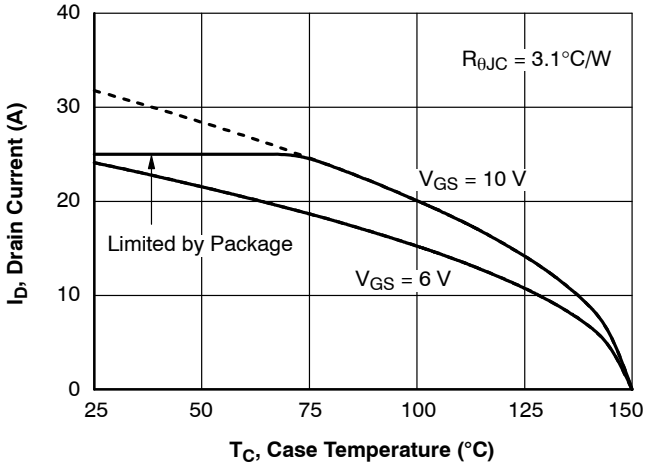


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

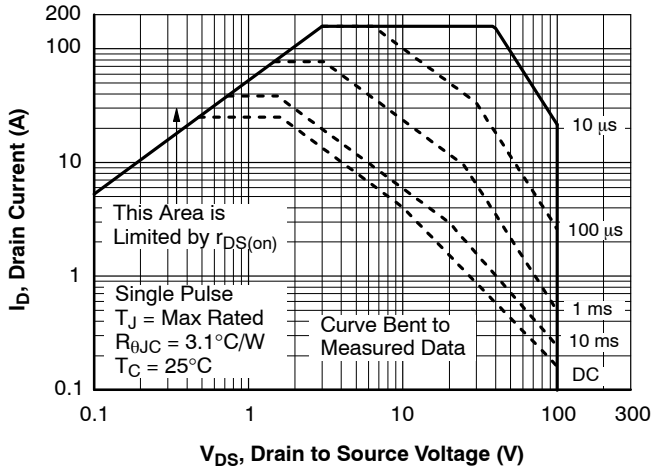


Figure 11. Forward Bias Safe Operating Area

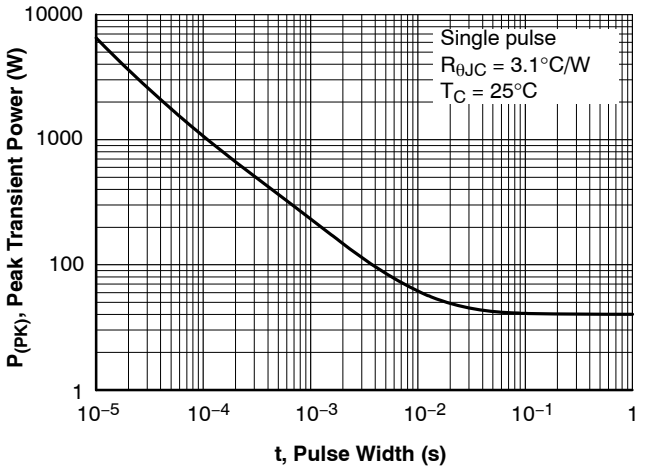


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C UNLESS OTHERWISE NOTED) (CONTINUED)

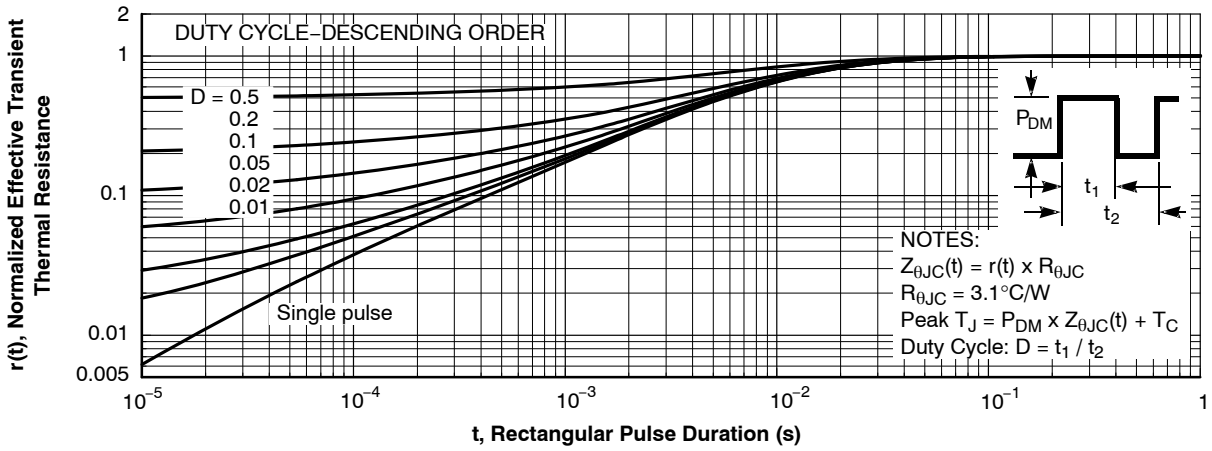


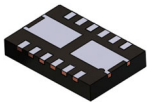
Figure 13. Junction−to−Case Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
FDMD82100	82100	PQFN12 3.3x5, 0.65P (Power 3.3 x 5) (Pb−Free, Halide Free)	13”	12 mm	3000 Units

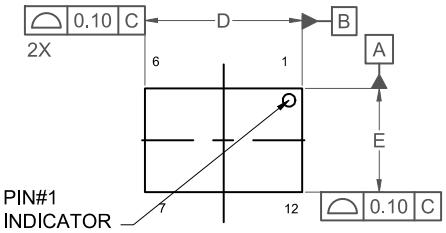
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

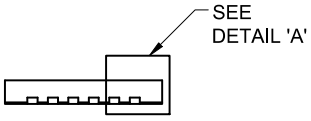


PQFN12 3.3X5, 0.65P
CASE 483BN
ISSUE A

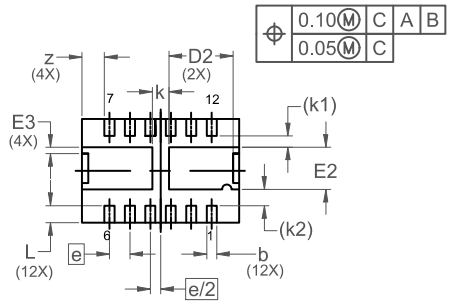
DATE 26 AUG 2021



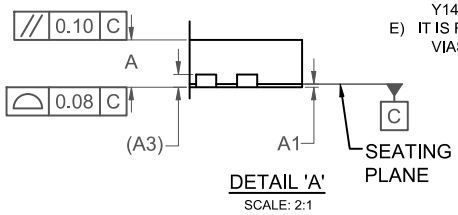
TOP VIEW



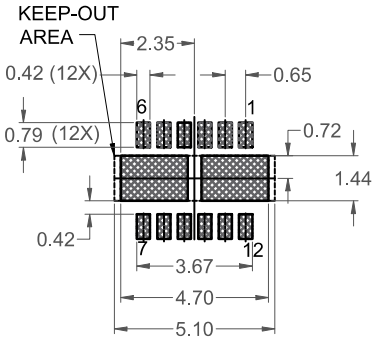
FRONT VIEW



BOTTOM VIEW



DETAIL 'A'
SCALE: 2:1



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC MO-240, VARIATION BA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	4.90	5.00	5.10
D2	1.92	2.04	2.14
E	3.20	3.30	3.40
E2	1.24	1.34	1.44
E3	0.10	0.20	0.30
e	0.65 BSC		
e/2	0.325 BSC		
k	0.53 REF		
k1	0.36 REF		
k2	0.52 REF		
L	0.44	0.54	0.64
z	0.72 REF		

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DESCRIPTION:	**PQFN12 3.3X5, 0.65P**		**PAGE 1 OF 1**

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